MX98745

XRC II
100 BASE-TX/FX
Repeater Controller

1.0 FEATURES

* IEEE 802.3u D5 repeater and management compatible
* Support 7 TX/FX ports and 1 universal port (TX or MII port selectable)
* Support 8-scale utilization and collision rate LED display
* Asynchronous Expansion port clock supported for easily stackable application
* Separate jabber and partition state machines for each port
* On-chip elasticity buffer for PHY signal re-timing to the MX98745 clock source
* Contents of internal register loaded from EEPROM
* PCS/MAC type MII interface selectable
* CMOS device features high integration and low power with a signle +5V supply

2.0 GENERAL DESCRIPTION

The MX98745, Second generation 100 Mb/s TX/FX Hub Controller (XRC II), is designed specifically to meet the needs of today's high speed Fast Ethernet networking systems. The MX98745 is fully IEEE 802.3u D5 clause 27 repeater compatible.

Difference from MX98741, which provides 8 dedicated TX/FX ports and 3 MII ports, MX98745 support 7 dedicated TX/FX ports and one programmble TX/FX/MII port. Whenever MII port is programmed, MX98745 also supports the flexibility to make user can easily select PCS or MAC type MII for system application. With this programmable MII interface, user can easily connect MX98745 to MX98742 (Bridge), or T4 transceiver. Or user can use this programmable MII interface to connect to either MAC or PCS type data transceiver.

All contents of internal registers are loaded from EEPROM in MX98745. If system application prefers default setting instead of using contents from EEPROM, EEPROM operation can be disabled by setting EECONF to low. This feature faciliates system modulization application.

8 scale of utilization LED is also provided by MX98745. They are 1%, 3%, 5%, 10%, 20%, 40%, 60% and 80+%. The defination for utiliztion is Mbs Received/100 Mb within one second sampling period. Meanwhile, RX/LINK, Partition, Isolation and Collision status are also provided through LED display.

A great improvement in MX98745 (compared to MX98741) is that it also provides "asynchronous expansion port data transfer mode" to make stackable design more easier.

3.0 BLOCK DIAGRAMS

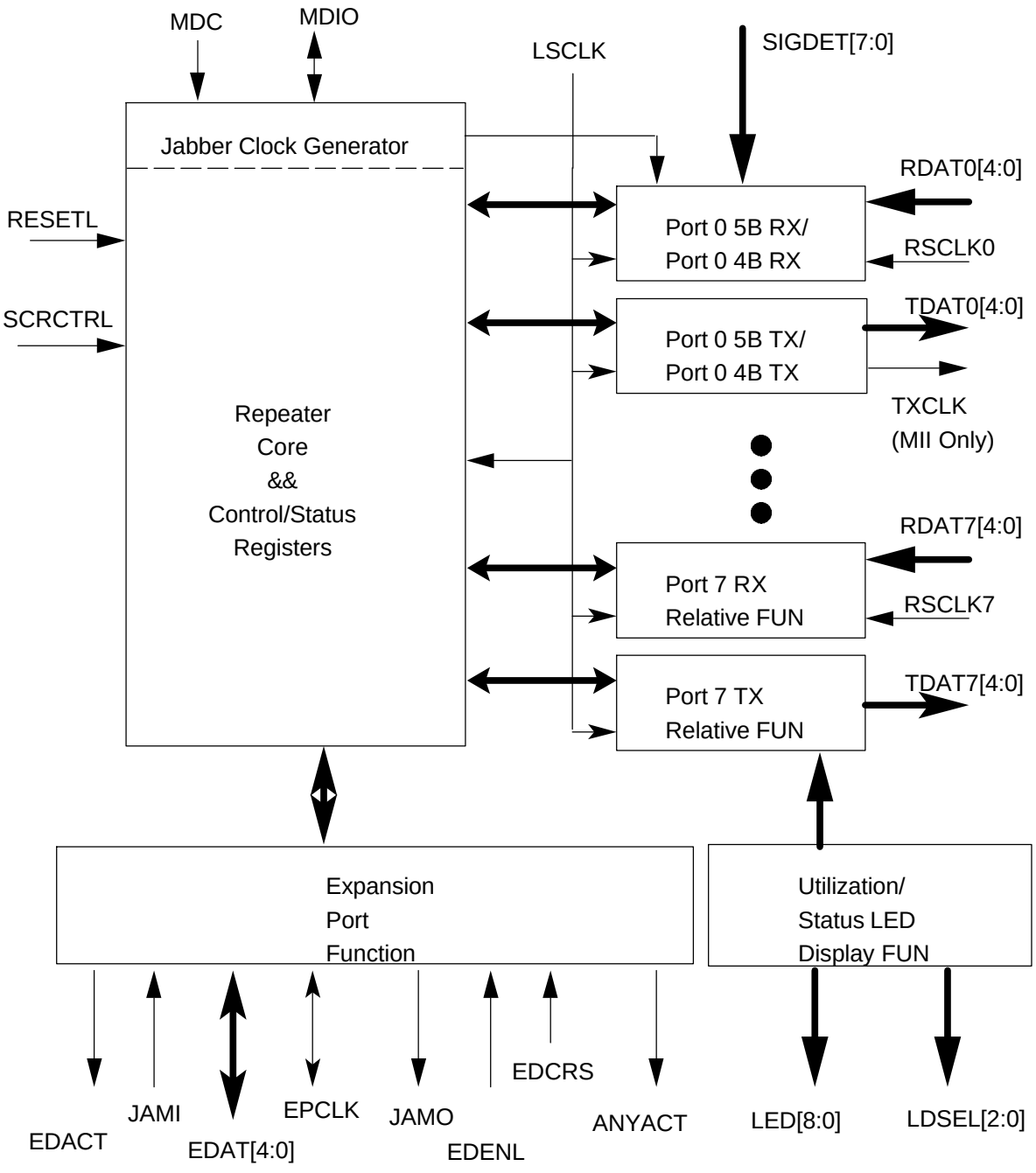

Figure 3-1 Block Diagram for XRC+

4.0 PIN CONFIGURATION

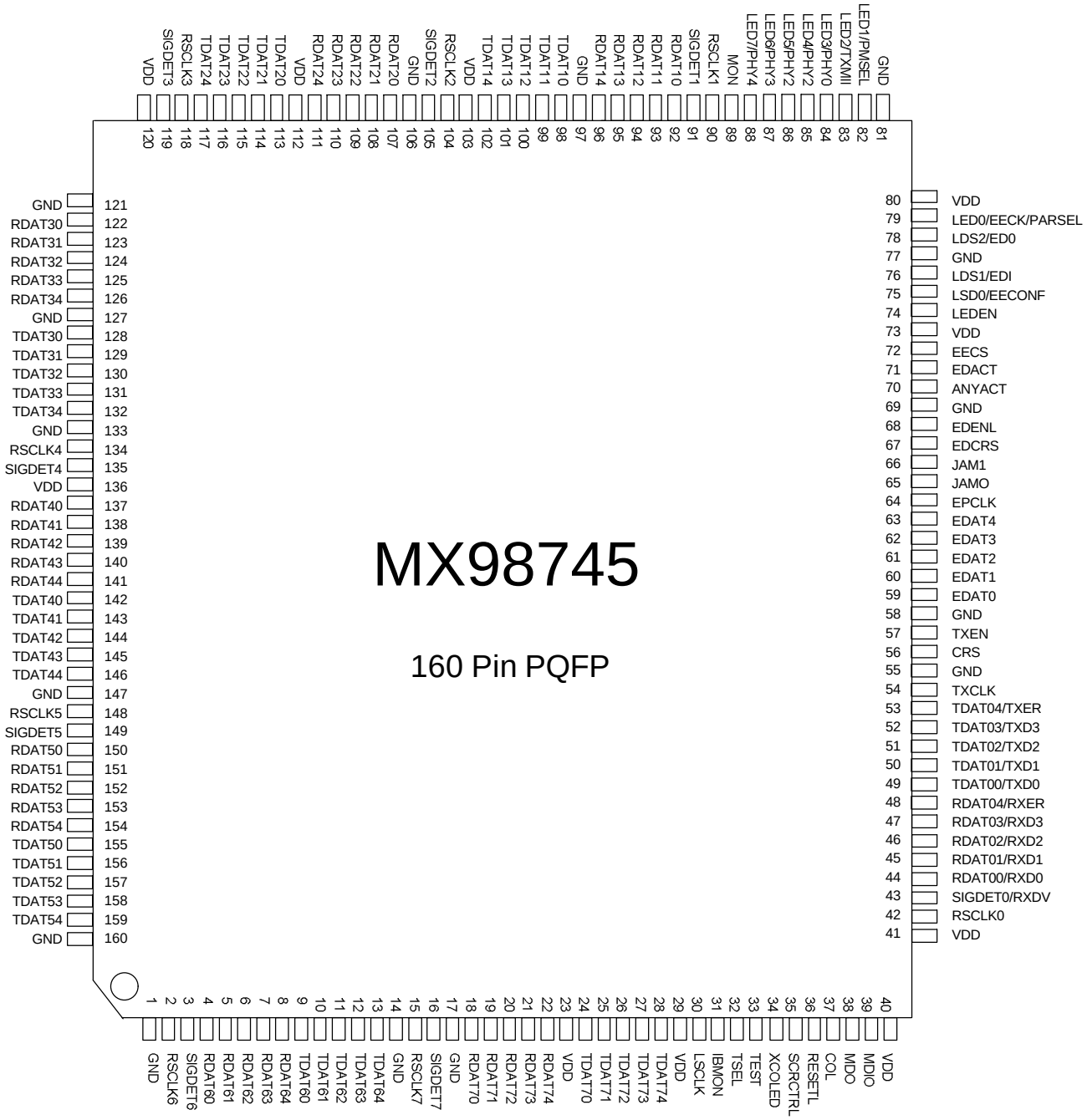

Figure 4-1 Pin Configuration for XRCII

5.0 PIN DESCRIPTION

A. MX Data Transceiver (Am78965/Am78966 or MC68836), 98 pins			
PAD #	**Name**	**I/O**	**Description**
24-28 9-13 155-159 142-146 128-132 113-117 98-102	TDAT[7:1][0:4]	O, TTL	**Transmit Data**. These five outputs are 5B encoded transmit data symbols, driven at the rising edge of LSCLK. TDAT4 is the Most Significant Bit.
30	LSCLK	I, TTL	**Local Synchrnous Clock**. This pin supplies the frequency reference to the MX98745 within same HUB. It should be driven by a crystal-controlled 25M clock source.
18-22 4-8 150-154 137-141 122-126 107-111 92-96	RDAT[7:1][0:4]	I, TTL	**Receive Data**. These 5 bit parallel data symbol from transceiver are latched by the rising edge of RSCLK of each port. RDAT4 is the Most Significant Bit.
15,2 148,134 118,104 90,42	RSCLK[7:0]	I, TTL	**Recovered Symbol Clock**. This is a 25 MHz clock, which is derived from the clock synchroniztion PLL circuit.
16,3, 149,135, 119,105, 91	SIGDET[7:1]	I, TTL	**Signal Detect**. This signal indicates that the received signal is above the detection threshold and will be used for the link test state machine.
31	Monitor	I, TTL	**Monitor Mode**. Internal Pulldown. When this pin is set to one, LED display pins LED[9:0] will be changed to monitor mode.

Table 5-1 Pin Description for XRCII

B. Expansion Port, 12 pins			
PAD #	**Name**	**I/O**	**Description**
65	JAMO	O, CMOS	**Forced Jam Out**. Active High. The OR'd forced jam signals controlled by Carrier Integrity Monitor of each port. If collision occurs inside the XRC II (exclude JAMI), this pin is also asserted.
66	JAMI	I, TTL	**Forced Jam Input**. Active High. Asserted by external arbitor, and XRCII will generate JAM patterns to all its ports whenever this signal is validate more than 40 ns. This signal is filtered by LSCLK for 40ns internally.
68	EDENL	I, Sche	**Enable Expansion Data**. Active Low. Asserted by an external arbitor. XRC II will not drive data onto EDAT until this pin is asserted. Assertion time less than 40ns will not be recognized by XRC II.
63-59	EDAT[4:0]	I/O, TTL	**Expansion Data**. Bidirectional 5 bit-wide data. By default, EDAT is an input. An external arbitor coordinates multiple devices on EDAT.
64	EPCLK	I/O, TTL	**Expansion port Data Clock**. This clock will be outputed by XRCII along with the EDAT[4:0]. Another module of XRCII should use this signal as expansion port data input clock.
70	ANYACT	O, CMOS	**Any Activity**. Active High. When XRCII tries to release data onto EDAT, this pin will be asserted by XRC II.
67	EDCRS	I, Sche	**Expansion Data Carrier Sense**. When this pin is asserted, XRC II will recognize that there is activity on expansion port data bus EDAT and perform corresponding activity within XRCII itself.
71	EDACT	O, CMOS	**Expansion Data Activity**. When XRCII detects that EDENL is asserted by external arbitor, it will assert EDACT high. System application can use this signal to control the data bus flow of EDAT.

Table 5-1 Pin Description for XRC II (Continued)

C. Universal Port (UP), 14 pins			
PAD #	**Name**	**I/O**	**Description**
43	SIGDET0/ RXDV	I, TTL	**Signal Detect/Receive Data Valid**. When TXMII (pin 84) is detected high during power on reset, This pin works as Signal detect in 5B data mode. When TXMII is low, this pin is output and works as RXDV in MII mode. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter
44-47	RDAT0[0:3]/ RXD[0:3]	I, TTL	**Receive Data[3:0]**. No matter TXMII's value is, these four pins work as the receive data both in TX mode and MII mode. Receive data is synchronous to RSCLK0's rising edge.
48	RDAT04/ RXER	I, TTL	**Receive Data Bit 4/Receive Data Error**. When TXMII is detected as 1, this pin works as the MSB of RDAT0[4:0]. When MII mode is selected, this pin is RXER and synchronous to RSCLK0's rising edge.
56	CRS	I/O, TTL	**Carrier Sense**. In PCS Mode, synchronous to TXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. In MAC mode (PMSEL is low), this pin is input.
57	TXEN	O, CMOS	**Transmit Enable**. This pin is output and synchronous to the TXCLK's rising edge whenever valid data is presented on TXD[3:0]
49-52	TDAT[0:3]/ TXD[0:3]	O, CMOS	**Transmit Data**. No matter TXMII's value is, these four pins work as the transmit data both in TX mode and MII mode. In TX mode, TDAT is synchronous to LSCLK rising edge. In MII mode, TXD[0:3] is synchronous to TXCLK rising edge.

Table 5-1 Pin Description for XRCII (Continued)

C. Universal Ports (UP) (Continued)			
PAD #	**Name**	**I/O**	**Description**
53	TDAT04/ TXER	O, CMOS	**Transmit Data Bit 4/Transmit ERROR**. When TXMII is set to one, this pin work as the MSB of TDAT of port 0. When TXMII is low, This pin acts as TXEN and is synchronous to the TXCLK's rising edge. When TXER is asserted for one or more than one TXCLK period while TXEN is also asserted, one or more "HALT" symbols will present at TXD[3:0].
37	COL	I/O, CMOS	**Collision**. This signal is asserted if both the receiving media and TXEN are active. When PCS type MII is selected, this pin is output from XRCII and indicates that there is collision within the XRCII. When PMSEL is 0, COL is input to XRCII and indicates that there is collision on the receiving port.
54	TXCLK	I/O, CMOS	**Transmit Clock**. 25M Hz clock. TXD[3:0], TXEN, TXER are synchronous to this clock's rising edge. In PCS type MII (PMSEL is 1), CRS and COL are also synchronous to this clock's rising edge.
D. Management, 2 pins			
38	MDC	I, TTL	**Management Data Clock**. The timing reference for MDIO. The minumum high and low times are 200 ns each.
39	MDIO	I/O, TTL	**Management Data Input/Output**. A bi-directional signal. The selection of input/output direction is based on IEEE 802.3u management functions (Section 22.2.4).
E. Test/Miscellaneous, 5 pins			
33	TEST	I	**Test**. Industrial test pin. Set to 0 for normal operation. When programmed to logic 1, XRC II is in test mode.
32	TSEL	I	**Test Select**. Used by industrial test. Internal Pulldown. Set to 0 for normal operation.

Table 5-1 Pin Description for XRC II (Continued)

E. Test/Miscellaneous (Continued)			
PAD #	**Name**	**I/O**	**Description**
34	XCOLED	O, LED	**Collision LED**. Active low. When there is collision within the XRC II, XCOLED will be on for 80ms and off for 20ms.
35	SCRCTRL	I, TTL	**Scrambler Control**. Active High. When this pin is set to 0, All TX port will be set to descramble mode, i.e. contents of register #17 will be disabled. When this pin is set to 1, Each port's scrambler/descrambler is controller by corresponding bit in register #17. Internally pullup.
36	RESETL	I, Sche	**Reset**. Active Low. Will be filtered by LSCLK within the MX98745.
31	IBMON	I, TTL	**Internal Bus Monitor**. In house debugging usage. Internally pull down.
F. LED Display/EEPROM Interface, 14 pins			
74	LEDEN	O, CMOS	**Led Output Enable**. When LEDEN is asserted high, it means that varuous internal status is shown on LED[7:0] according to the value on LDS[2:0]
78, 76, 75	LDS2/EDO, LDS1/EDI, LDS0/EECONF	I/O, TTL	**LED Output Select**. LDS0 is internally pulldown and value on LDS0 will be latched internally by MX98745 at the rising edge of RESETL as the value of EECONF. Value on LDS1 will act as EEPROM Data Input signal during EEPROM loading operation (after power on reset and EECONF is set to 1) and LDS2 will be data output from EEPROM. When EECONF is low, EEPROM operation will be disabled. After power on reset, LDS[2:0] work as the select pins of LED[7:0] output. The following are corresponding definition LDS2 LDS1 LDS0 0 0 1 Link/Receive 0 1 0 Isolation 0 1 1 Partition 1 0 0 Utilization 1 0 1 Collision Rate

Table 5-1 Pin Description for XRC II (Continued)