MX98743

FEM
100 Base Fast Ethernet
Management Chip

1.0 FEATURES

* Support IEEE 802.3 MIBs
* Support RMON etherStatsEnty and etherStats History group
* 8/12/32 bit microprocessor interface
* Linear mapped registers for easy programming
* Embedded MAC for low-cost management functions implementation

2.0 GENERAL DESCRIPTION

The Fast Ethernet Management (FEM) chip works with XRC to support the following Repeater Management functions:

IEEE 802.3u Port Management Attributes:
- PortAdminState (from XRC, 8 port state)
- AutoParitionState (from XRC, 8 port state)
- ReadableFrame (32-bit Counter)
- ReadableOctets (32-bit Counter)
- FramesCheckSequenceError (32-bit Counter)
- AlignmentErrors (32-bit Counter)
- FramesTooLong (32-bit Counter)
- ShortEvents (32-bit Counter)
- Runts (32-bit Counter)
- Collision (32-bit Counter)
- LateEvents (32-bit Counter)
- VeryLongEvents (32-bit Counter)
- DataRateMismatches (32-bit Counter)
- Auto Partitions (32-bit Counter)
- Isolates (32-bit Counter)
- SymbolErrorDuringPacket (32-bit Counter)
- LastSourceAddress (32-bit Counter)
- SourceAddressChange (32-bit Counter)

IEEE 802.3u MAU Management Attributes:
- FalseCarriers (32-bit Counter)

RMON MIB Statistics Group
- etherStatsDropEvents (32-bit Counter)
- etherStatsOctets (32-bit Counter, same as ReadableOctets)
- etherStatsPkts (32-bit Counter, same as ReadableFrames)
- etherStatsBroadcastPks (32-bit Counter)
- etherStatsMulticastPks (32-bit Counter)
- etherStatsCRCSlignErrors (32-bit Counter, sum of FrameCheckSequenceErrors and AlignmentErrors)
- etherStatsUndersizedPks (32-bit Counter, same as ShortEvent)
- etherStatsOversizedPks (32-bit Counter, same as FrameTooLong)
- etherStatsFragments (32-bit Counter, same as Runts)
- etherStatsJabbers (32-bit Counter)
- etherStatsCollision (32-bit Counter, same as Collision)
- etherStatsPks64Octets (32-bit Counter)
- etherStatsPkts65to127Octs (32-bit Counter)
- etherStatsPkts128to255Octets (32-bit Counter)
- etherStatsPks236to511Octets (32-bit Counter)
- etherStatsPkts512to1023Octets (32-bit Counter)
- etherStatsPkts1024to1518Octets (32-bit Counter)

RMON MIB History Group
The same period is programmable from 1 second to 65536 seconds.
- etherHistoryDropEvents (32-bit Counter)
- etherHistoryOctets (32-bit Counter, same as ReadableOctets)
- etherHistoryPkts (32-bit Counter, same as ReadableFrames)
- etherHistoryBroadcastPkts (32-bit Counter)
- etherHistoryMulticastPkts (32-bit Counter)
- etherHistoryCRCAlignErrors (32-bit Counter, sum of FrameCheckSequenceErrors and AlignmentErrors
- etherHistoryUndersizedPkts (32-bit Counter, same as ShortEvent)
- etherHistoryOversizedPkts (32-bit Counter, same as FramesTooLong)
- etherHistoryFragment (32-bit Counter, same as Runts)
- eaterHistoryCollision (32-bit Counter, same as Collision)

All the above values as well as XRC registers and counters can be accessed directly through the CPU interface. The FEM occupies a contiguous 4K-byte memory space with 8-bit, 16-bit, and 32-bit datapath choices which allows system designers the maximum flexibility.

3.0 SIMPLIFIED SYSTEM DIAGRAM

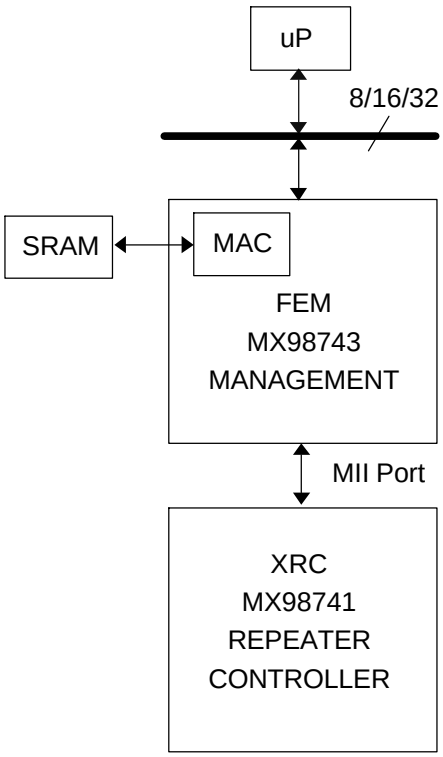


Figure 3-1. 8-Port Management Hub System Diagram

The FEM contains a MAC which is capable of transmitting and receiving management packets that are stored in an external SRAM. The CPU reads and writes packets in SRAM through the FEM.

4.0 CONNECTION DIAGRAM

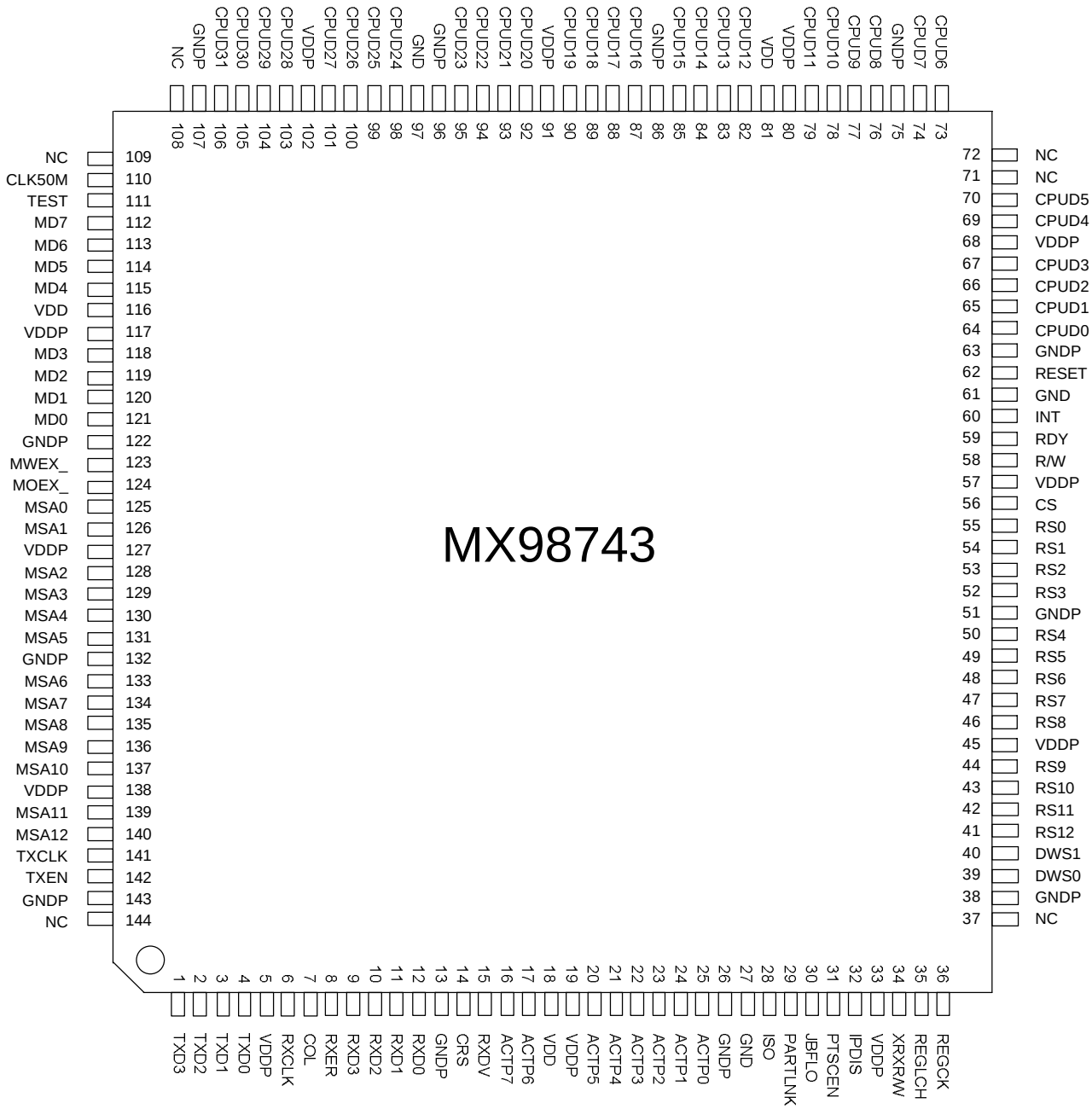


Figure 4-1. 144 Pin PQFP Package

5.0 PIN DESCRIPTION

Table 5-1. Media Independent Interface, 15 pins

PIN#	NAME	I/O	DESCRIPTION
15	RXDV	I, TTL	Receive Data Valid MII. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame delimiter.
14	CRS	I, TTL	Carrier Sense MII. This pin, synchronous to RXCLK in TX mode, is asserted when the receiving medium is not idle.
8	RXER	I. TTL	Receive Error. This pin is synchronous to RXCLK's rising edge. While RXDV is asserted, i.e. a frame is being received, this signal is asserted if any coding error is detected.
6	RXCLK	I, TTL	Receive Clock MII. 25 MHz continuous clock that provides the timing reference for the transfer of the RXDV, RXD and RXER signals.
9-12	RXD3-0	I, TTL	Receive Data MII. RXD3-0 are synchronous to RXCLK's rising edge with RXD3 being the Most Significant Bit. For each RXCLK period in which RXDV is asserted, RXD3-0 should be latched by the MAC. While RXDV is deasserted , RXD3-0 are the 5B/4B nibbles decoded from RDAT4-0.
7	COL	I, TTL	Collision Mll. This signal is asserted if both the receiving media and TXEN are active.
141	TXCLK	I, TTL	25 MHz Transmit Clock Input.
142	TXEN	O	Transmit Enable. This output becomes active when the first data packet is valid on TXD3-0 and goes low after the last packet is clocked out of TXD[3:0].
1-4	TXD[3:0]	O	Transmit Data MII. TXD3-0 are synchronous to TXCLK's rising edge with TXD3 being the Most Significant Bit

Table 5-2. Expansion Port, 8 pins

PIN#	NAME	I/O	DESCRIPTION
16,17, 20-25	ACTP[7:0]	I, TTL	Activity Out. These pins, synchronous to the 50 MHz clock, represent the activities of each port and also serve as data framing signals for the packet on EDATA. ACT_P leads EDAT's /J/K pattem by more than 80ns and is deasserted 40 ns after the /T/R or the last byte of Jam patterns.

Table 5-3. XRC Register Access Pins, 8 pins

PIN#	NAME	I/O	DESCRIPTION
29	PARTLNK	I, TTL	Partition/Link Good. This pin, active high, shows the Patition and Link status of the repeater MX98741. The serial input data is stored in Register RS[12:1]=081h.
30	JBFLO	I, TTL	JAB/Elastic Buffer Over/Underflow. This pin, active high, shows the Jabber status and Elastic Buffer Over/Underflow status of the XRC. The serial input data is stored in Register RS[12:1]=01Ah.
28	ISO	I, TTL	Isolation. This pin shows the Isolation status of the XRC. The serial input data is stored in Register RS[12:1]=01Ch.

Table 5-3. XRC Register Access Pins, 8 pins

PIN#	NAME	I/O	DESCRIPTION
31	PTSCEN	I/O	Port Enable/Scramble Enable. If XRCR/W is high, each port's Enable/Scramble status is displayed at the rising edge of REGCK and the serial input data is stored in Register RS[12:1]=016h. If XRCRW is low, the content of Register RS[12:1]=016h is read out serially.
32	IPDIS	I/O	Isolation/Partition Disable. If XRCR/W is high, each port's Isolation/Partition status is displayed at the rising edge of REGCK and the serial input data is stored in Register RS[12:1]=01Eh. If XRCRW is low, the content of Register RS[12:1]=01Eh is read out serially.
34	XRCR/W	O, TTL	XRC Read or Write. High indicates 'Read' Mode; register is being read out. Low indicates 'Write' Mode. The FEM will issue XRC register write cycle when the CPU is writing Register RS[12:1]=016h or 01Eh.
35	REGLCH	I/O, TTL	Register Latch. REGLCH is an input pin when XRCRW is held high and an output pin when XRCRW is held low.
36	REGCK	O	Register Clock . This pin is providing the 12.5MHz frequency whenever the FEM is accessing the XRC registers.

Table 5-4. CPU Interface, 51 pins

PIN#	NAME	I/O	DESCRIPTION
56	CS	I,TTL	Chip Select. This pin, active low, is used to access the FEM internal register or SRAM buffer when held low.
58	R/W	I,TTL	System Read/Write. High for read, and low for write.
59	RDY	O,OD	Ready. This pin, active low, is an tri-state output.
60	INT	O,OD	Interrupt. Active low. Open Drain.
64-67, 69, 70, 73, 74, 76-79, 82-85, 87-90, 93-95, 98-101, 103-106	CPUD0-31	I/O	Data. A group of 8,16, or 32 pins can become active depending on the value of DWS1-0. Inactive pins are tri-stated.
40-39,	DWS[1:0]	I,TTL	Datapath Width Selection. These two pins determin which datapath width for CPUD31-0. DWS[1:0] = '00' : 8 bit, = '01' or '10' : 16 bit, = '11' : 32 bit.
41-44, 46-50, 52-55	RS12-0	I,TTL	FEM Register or CPU Selection. When RS12=0, RS[11:0] represents FEM internal registers select pins. When RS12=1, RS[11:0] represents CPU interface address lines. RS[11:0] is mapped to MA[11:0] for 4Kbytes memory: 0h~7ffh for receive buffer, and 800h~fffh for transmit buffer.

Table 5-5. SRAM Interface, 24 pins

PIN#	NAME	I/O	DESCRIPTION
140, 139, 137-133, 131-128, 126-125	MSA[12:0]	O	SRAM Address. 13-bit address to select the minimum 8Kbytes memory.
112-115, 118-121	MD[7:0]	I/O, TTL	SRAM Data Bus.
124	MOEX_	O	SRAM Read Enable. Active low.
123	MWEX_	O	SRAM Write Enable. Active low.
110	CLK50M	I, TTL	50 MHz Oscillator Input. This is the clock reference for SRAM Interface bus timing.

Table 5-6. Miscellaneous Pins, 2 pin

PIN#	NAME	I/O	DESCRIPTION
62	RESET	I, TTL	Reset. Reset is active low and places all the MX98743 logic in a reset mode.
111	TEST	I, TTL	Test Pin. This is the internal test pin which is internal pulled low. User can either leave it uncommented or tie it to ground for normal operation.

Table 5-7. Power/Ground, 30 pins

PIN#	NAME	I/O	DESCRIPTION
13, 26, 27 38, 51, 61, 63, 75, 86, 96, 97, 107, 122, 132, 143	GND/GNDP		Ground.
5, 18, 19, 33, 45, 57, 68, 80, 81, 91, 102, 116, 117, 127,138	VDD/VDDP		Power.

Table 5-7. No Connection, 6 pins

PIN#	NAME	I/O	DESCRIPTION
37, 71, 72, 108, 109, 144	NC		No Connection. Do not connected to these pins.

6.0 SRAM BUFFER OPERATION

6.1 RECEIVE & TRANSMIT PAGE FORMAT

SRAM Map consists a total of 8K bytes memory which is divided equally into 4 pages. Each Page is 12K bytes; there are three received pages and one transmit page. The Receive buffer uses a Buffer Ring Structure comprised of three ontiguous 2K-byte buffers, Page 0-2, for storage of received packet.

RX Page 0 (2K bytes)
RX Page 1 (2K bytes)
RX Page 2 (2K bytes)
TX Page (2K bytes)

The first two bytes of each Receive Page is used to store the receive status. Byte0 contains Receive Byte Count--Countbit[7:0]; while byte1 contains various information as follows:

Byte0 & Byte1

BIT	DESCRIPTION
byte 1[7:0]	Receive byte count -- Countbit[7:0]
byte 1[7]	Packet received with no error.
byte 1[6]	CRC error.
byte 1[5]	Multicast/Broadcast or Physical Address.
byte 1[4]	Internal four-byte FIFO overrun.
byte 1[3:0]	Receive byte count -- Countbit[11:8]

The first word if the Transmit Page contains the transmit byte count information with byte0--Countbit[7:0] and byte 1[3:0]--Countbit[11:8].

6.2 Receive Buffer Ring

Two pointers are used to control the Receive Buffer Ring. These are the Current Page Number Pointers and the Select Page Number Pointer. The Current Number Pointer points to the first Page that MAC will use to update the received data, whereas the Select Page Number Pointer points to the first page in the Ring not yet read by the CPU. Under normal operation, the CPU activates Receive Enable Bit in the Register 3C(MAC Control Register) and the packet beings arriving. The MAC starts storing the packet at the location pointed to be the Current Page Number Pointer. If three packets have successfully arrived the Buffer Ring and the CPU has not read a single page from the SRAM, the values of the Current and the Select Page Number are equal. As a result, the Receive Enable bit is disable and it remains disabled untile the CPU has removed at least one Packet data from the Ring to advance the Select Page Number Pointer. Each time a packet is successfully written on the SRAM, an interrupt is issued. The CPU will acknowledge interrupt and removes a packet from the Buffer Ring where the Select Page Number Pointer is point to. Usually the Select Page Number Pointer will advance when a packet is removed. If the values of Select Page Number and the Current Page Number are not equal, CPU will continue reading data from the Buffer Ring. However, if the values are equal, CPU will abort reading activity. The following procedures better illustrates how CPU handles different Receive Buffer Ring situations:

Initial Receive Enable procedure:

1. Get Current Page Number from the MAC Status Register.
2. Assign Select Page Number the value of Current Page Number and set Receive Enable bit.

Procedure During Normal Receive Operation:

1. If Select Page Number dose not equal to the Current Page Number, go to step 2.
2. Read Receive Buffer Ring data.
3. Assign Select Page Number to the next page.
4. Go back to step 1.

Procedure For Receive Buffer Overflow:

1. Read the Receive Buffer data.
2. Assign Select Page Number to the next page.
3. Read Receive Buffer data.
4. Assign Select Page Number to the next page.
5. Read Receive Buffer data.
6. Assign the Select Page Number to the next page.
7. Re-initial receive enable procedure.

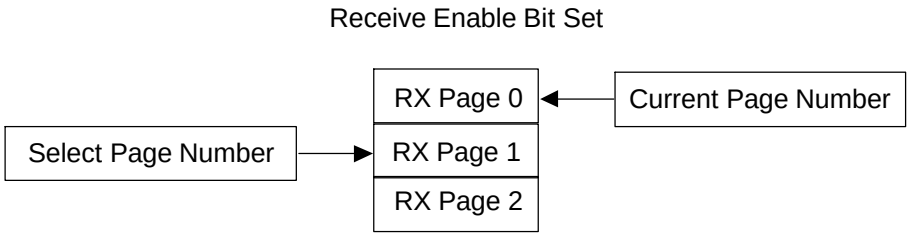


Figure 6-1. Receive Buffer Ring

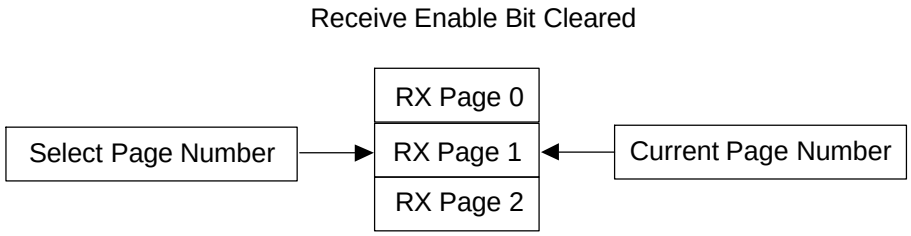


Figure 6-2. Received Packet Enters the Buffer Ring

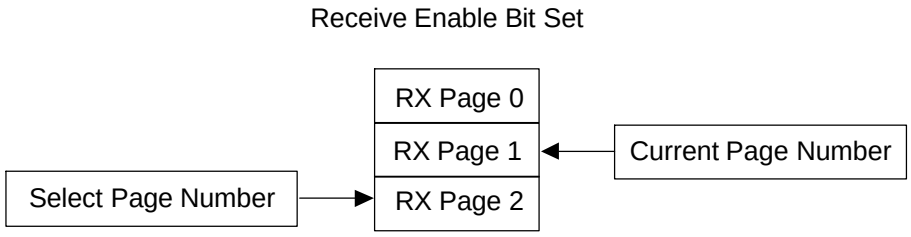


Figure 6-3. CPU Removed One Packet from the Buffer Ring

7.0 Programming Guide

All the FEM registers, attributes as well as XRC registers can be accessed through the CPU interface directly with indexing. All registers are 16-bit wide and mapped directly to RS[12:0] is used to determine FEM Register selection or SRAM access. RS12=0 indicates FEM register select; RS12=1 indicates SRAM access. For SRAM access, RS[11:0] is mapped to MA[11:0] for 4Kbyte memory; 0h-7ffh for receive buffer, 800h-fffh for transmit buffer.

7.1 GENERAL DESCRIPTION OF REGISTER ACCESS METHODS

Each entry in the following tables represents a 16-bit wide register space. Only RS0 is used to selected the bytes within the 16-bit register if the datapath is 8-bit wide; however, RS[12:2] are needed to access the registers if 32-bit datapath is selected.

7.2 SRAM ACCESS & FEM REGISTER SELECTION TABLE

Table 6-1. SRAM Access & FEM Register Selection Table

RS12	RS11	RS[10:8]	RS[7:1]	RS0	REGISTER	R/W
1	0	x	x	x	SRAM Access, 0-7ffh:Receive Buffer	R/W
1	1	x	x	x	SRAM Access, 800-fffh:Transmit Buffer	R/W
0	0	0	00	x	Repeater Interrupt Status Register	R
0	0	0	02	x	Repeater Interrupt Mask Register	R/W
0	0	0	04	x	Port Link/Partition Change Interrupt Status Register	R
0	0	0	06	x	Port Link/Partition Change Interrupt Mask Register	R/W
0	0	0	08	x	Data Rate Mismatch/Jabber Interrupt Status Register	R
0	0	0	0A	x	Data Rate Mismatch/Jabber Interrupt Mask Register	R/W
0	0	0	0C	x	Isolation/SA Change Interrupt Status Register	R
0	0	0	0E	x	Isolation/SA Change Interrupt Mask Register	R/W
0	0	0	12	x	Sample Period Register	R/W
0	0	0	14	x	Sample Enable Register	R/W

Table 6-1. SRAM Access & FEM Register Selection Table

RS12	RS11	RS[10:8]	RS[7:1]	RS0	REGISTER	R/W
0	0	0	16	x	XRC Port Control Register	R/W
0	0	0	18	x	Link and Partition Status Register	R
0	0	0	1A	x	EB O/U and Jabber Status Register	R
0	0	0	1C	x	Isolation Status	R
0	0	0	1E	x	Partition/Isolation Disable Status	R/W
0	0	0	22	x	Stored SA Lo for SA Match Interrupt	R/W
0	0	0	24	x	Stored SA Mid for SA Match Interrupt	R/W
0	0	0	26	x	Stored SA Hi for SA Match Interrupt	R/W
0	0	0	28	x	Stored DA Lo for DA Match Interrupt	R/W
0	0	0	2A	x	Stored DA Mid for DA Match Interrupt	R/W
0	0	0	2C	x	Stored DA Hi for DA Match Interrupt	R/W
0	0	0	30	x	Stored SA1 Lo for Management Packet Received	R/W
0	0	0	32	x	Stored SA1 Mid for Management Packet Received	R/W
0	0	0	34	x	Stored SA1 Hi for Management Packet Received	R/W
0	0	0	36	x	Stored SA2 Lo for Management Packet Received	R/W
0	0	0	38	x	Stored SA2 Mid for Management Packet Received	R/W
0	0	0	3A	x	Stored SA2 Hi for Management Packet Received	R/W
0	0	0	3C	x	MAC Control Register	R/W
0	0	0	3E	x	MAC Status Register	R/W
0	1	0	00-6F	x	Port 0 802.3 Attributes and RMON MIBs	R
0	1	1	00-6F	x	Port 1 802.3 Attributes and RMON MIBs	R
0	1	2	00-6F	x	Port 2 802.3 Attributes and RMON MIBs	R
0	1	3	00-6F	x	Port 3 802.3 Attributes and RMON MIBs	R
0	1	4	00-6F	x	Port 4 802.3 Attributes and RMON MIBs	R
0	1	5	00-6F	x	Port 5 802.3 Attributes and RMON MIBs	R
0	1	6	00-6F	x	Port 6 802.3 Attributes and RMON MIBs	R
0	1	7	00-6F	x	Port 7 802.3 Attributes and RMON MIBs	R

Table 6-2. IEEE Attributes and RMON MIB Selection Table

RS[7:1]	RS0	IEEE Attributes	R/W
00	x	dot3 Readable Frames Lo	R
01	x	dot3 Readable Frames Hi	R
02	x	dot3 Readable Octets Lo	R
03	x	dot3 Readable Octets Hi	R
04	x	dot3 Frame Check Sequence Errors Lo	R
05	x	dot3 Frame Check Sequence Errors Hi	R
06	x	dot3 Aligment Errors Lo	R
07	x	dot3 Aligment Errors Hi	R
08	x	dot3 Frame Too Long Lo	R
09	x	dot3 Frame Too Long Hi	R
0A	x	dot3 Short Events Lo	R
0B	x	dot3 Short Events Hi	R
0C	x	dot3 Runts Lo	R
0D	x	dot3 Runts Hi	R
0E	x	dot3 Collision Lo	R
0F	x	dot3 Collision Hi	R
10	x	dot3 Late Event Lo	R
11	x	dot3 Late Event Hi	R
12	x	dot3 Very Long Events Lo	R
13	x	dot3 Very Long Events Hi	R
14	x	dot3 Data Rate Mismatches Lo	R
15	x	dot3 Data Rate Mismatches Hi	R
16	x	dot3 Auto Partitions Lo	R
17	x	dot3 Auto Partitions Hi	R
18	x	dot3 Isolates Lo	R
19	x	dot3 Isolates Hi	R
1A	x	dot3 Symbol Error During packet Lo	R
1B	x	dot3 Symbol Error During packet Hi	R
1C	x	dot3 Last Source Address Lo	R/W
1D	x	dot3 Last Source Address Mid	R/W
1E	x	dot3 Last Source Address Hi	R/W
20	x	dot3 Source Address Change Lo	R
21	x	dot3 Source Address Change Hi	R
22	x	dot3 False Carriers Lo	R
23	x	dot3 False Carriers Hi	R
23-2F	x	reserved	

Table 6-3. RMON MIB Selection Table

RS[7:1]	RS0	IEEE Attributes	R/W
30	x	Rmon Ether Stats Drop Events Lo	R
31	x	Rmon Ether Stats Drop Events Hi	R
32	x	Rmon Ether Stats Octets Lo	R
33	x	Rmon Ether Stats Octets Hi	R
34	x	Rmon Ether Stats Pkts Lo	R
35	x	Rmon Ether Stats Pkts Hi	R
36	x	Rmon Ether Stats Broadcast Pkts Lo	R
37	x	Rmon Ether Stats Broadcast Pkts Hi	R
38	x	Rmon Ether Stats Multicast Pkts Lo	R
39	x	Rmon Ether Stats Multicast Pkts Hi	R
3A	x	Rmon Ether Stats CRC Align Errors Lo	R
3B	x	Rmon Ether Stats CRC Align Errors Hi	R
3C	x	Rmon Ether Stats Undersized Pkts Lo	R
3D	x	Rmon Ether Stats Undersized Pkts Hi	R
3E	x	Rmon Ether Stats Oversized Pkts Lo	R
3F	x	Rmon Ether Stats Oversized Pkts Hi	R
40	x	Rmon Ether Stats Fragments Lo	R
41	x	Rmon Ether Stats Fragments Hi	R
42	x	Rmon Ether Stats Jabbers Lo	R
43	x	Rmon Ether Stats Jabbers Hi	R
44	x	Rmon Ether Stats Collision Lo	R
45	x	Rmon Ether Stats Collision Hi	R
46	x	Rmon Ether Stats Pkts 64 Octets Lo	R
47	x	Rmon Ether Stats Pkts 64 Octets Hi	R
48	x	Rmon Ether Stats Pkts 65 to 127 Octets Lo	R
49	x	Rmon Ether Stats Pkts 65 to 127 Octets Hi	R
4A	x	Rmon Ether Stats Pkts 128 to 255 Octets Lo	R
4B	x	Rmon Ether Stats Pkts 128 to 255 Octets Hi	R
4C	x	Rmon Ether Stats Pkts 236 to 511 Octets Lo	R
4D	x	Rmon Ether Stats Pkts 236 to 511 Octets Hi	R
4E	x	Rmon Ether Stats Pkts 512 to 1023 Octets Lo	R
4F	x	Rmon Ether Stats Pkts 512 to 1023 Octets Hi	R
50	x	Rmon Ether Stats Pkts 1024 to 1518 Octets Lo	R
51	x	Rmon Ether Stats Pkts 1024 to 1518 Octets Hi	R
52	x	Rmon Ether History Drop Events Lo	R
53	x	Rmon Ether History Drop Events Hi	R
54	x	Rmon Ether History Octets Lo	R

Table 6-3. RMON MIB Selection Table

RS[7:1]	RS0	RMON MIB	R/W
55	x	Rmon Ether History Octets Hi	R
56	x	Rmon Ether History Pkts Lo	R
57	x	Rmon Ether History Pkts HI	R
58	x	Rmon Ether History Broadcast Pkts Lo	R
59	x	Rmon Ether History Broadcast Pkts Hi	R
5A	x	Rmon Ether History Multicast Pkts Lo	R
5B	x	Rmon Ether History Multicast Pkts Hi	R
5C	x	Rmon Ether History CRC Align Errors Lo	R
5D	x	Rmon Ether History CRC Align Errors Hi	R
5E	x	Rmon Ether History Undersized Pkts Lo	R
5F	x	Rmon Ether History Undersized Pkts Hi	R
60	x	Rmon Ether History Oversized Pkts Lo	R
61	x	Rmon Ether History Oversized Pkts Hi	R
62	x	Rmon Ether History Fragments Lo	R
63	x	Rmon Ether History Fragments Hi	R
64	x	Rmon Ether History Jabbers Lo	R
65	x	Rmon Ether History Jabbers Hi	R
66	x	Rmon Ether History Collision Lo	R
67	x	Rmon Ether History Collision Hi	R

8.0 REGISTER DEFINITIONS

8.1 MAC CONTROL REGISTER (R/W)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	RB	RM	REN	S1	S0	X	X	TEN

Table 7-1.

BIT	NAME	DESCRIPTION	R/W
15:8	Reserved	Reserved	R/W
7	RB	1: Receive brocast packet. 0: Not to eceive brocast packet.	R/W
6	RM	1: Receive multicast packet. 0: Not to receive multicast packet.	R/W
5	REN	1: Receive enable. It is cleared whenreceive buffer overflows or the FEM is in reset state. 0: Receive disable.	R/W
4-3	S1-0	Select page number of receive buffer for CPU access. [S1,S0] = 00: Page 0; 01: Page 1; 1x: Page 2.	R/W
2-1		Reserved	R/W
0	TEN	1:Transmit enable. It is cleared by packet transmitted to FEM reset. 0:Transmit disable.	R/W

8.2 MAC STATUS REGISTER (R)

msb lsh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX	COL	ABT	CRS	UR	X	X	X	RX	CRC	MB	OR	BF	ABT	S1	S0

Table 7-2.

BIT	NAME	DESCRIPTION	R/W
15	TX	1:Packet transmitted with no errors.	R
14	COL	1: Collision at least once.	R
13	ABT	1: Transmit is aborted after 16 collisions.	R
12	CRS	1: Carrier sense lost during transmission.	R
11	UN	1:Internal 4 bytes FIFO underrun.	R
10-8	X	Reserved	R
7	RX	1:Packet received with no errors.	R
6	CRC	1:CRC error.	R
5	MB	1:Multicast/Broadcast Address match. 0:Physical Address match.	R
4	OR	1:Internal 4 bytes FIFO overrun.	R
3	BF	1:Receive Buffer Full.	R
2	ABT	1:Packet aborted due to Receive Buffer full.	R
1-0	S1-0	Current Page Number of Receive Buffer for MAC receiver.	R

8.3 REPEATER INTERRUPT STATUS REGISTER (RO)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	GI	IE	SA	DA	X	TX	RX	X

Table 7-3.

BIT	NAME	DESCRIPTION	R/W
15:8	Reserved	Indeterminate	R
7	G	Global Interrupt. 1:INT is not active. 0:INT is active. This bit becomes '1' only if all the interrupt sources are cleared.	R
6	I	Interface Error Interrupt. Set to '1' if interface error with XRC occurs.	R
5	S	Source Address Match Interrupt. The SA of incoming packet matches a pre-defined 6-byte DA value.	R
4	D	Destination Address Match Interrupt. The DA of incoming packet matches a pre-defined 6-byte DA value.	R
3	Reserved	Indeterminate	R
2	TX	Management Packet Transmitted. 1:Packet transmitted. It is clear after reset. 0:No packet transmitted.	R
1	RX	Management Packet Received. 1:Packet received. It is cleared after reset.	R
0	Reserved	Reserved	R

8.4 REPEATER INTERRUPT MASK/CONFIGURATION REGISTER (R/W)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	GM	IM	SM	DM	X	TM	RM	RS

Table 7-4.

BIT	NAME	DESCRIPTION	R/W
15:8	Reserved	Indeteminate	R/W
7	GM	Global Interrupt Mask. 1:Masking INT. 0:Unmasking INT.	R/W
6	IM	Interface Error Interrupt Mask. 1:Masking INT. 0:Unmasking INT	R/W
5	SM	Source Address Match Interrupt Mask. 1:Masking INT. 0:Unmasking INT	R/W
4	DM	Destination Address Match Interrupt Mask. 1:Masking INT. 0:Unmasking INT	R/W
3	Reserved	Indeterminate	R
2	TM	Management Packet Transmitted Interrupt Mask. 1:Masking INT. 0:Unmasking INT	R/W
1	RM	Management Packet Received Interrupt Mask. 1:Masking INT. 0:Unmasking INT	R/W
0	RS	1:Reset FEM. 0:Not Reset FEM. '0' after RESET pin is asserted low.	R/W

8.5 PORT LINK STATUS CHANGE/PARTITION INTERRUPT (RO)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0	P7	P6	P5	P4	P3	P2	P1	P0

Table 7-5.

BIT	NAME	DESCRIPTION	R/W
15	L7	Set to '1' if Link Status changes on Port 7.	R
14	L6	Set to '1' if Link Status changes on Port 6.	R
13	L5	Set to '1' if Link Status changes on Port 5.	R
12	L4	Set to '1' if Link Status changes on Port 4.	R
11	L3	Set to '1' if Link Status changes on Port 3.	R
10	L2	Set to '1' if Link Status changes on Port 2.	R
9	L1	Set to '1' if Link Status changes on Port 1.	R
8	L0	Set to '1' if Link Status changes on Port 0.	R
7	P7	Set to '1' if Partition Status changes on Port 7.	R
6	P6	Set to '1' if Partition Status changes on Port 6.	R
5	P5	Set to '1' if Partition Status changes on Port 5.	R
4	P4	Set to '1' if Partition Status changes on Port 4.	R
3	P3	Set to '1' if Partition Status changes on Port 3.	R
2	P2	Set to '1' if Partition Status changes on Port 2.	R
1	P1	Set to '1' if Partition Status changes on Port 1.	R
0	P0	Set to '1' if Partition Status changes on Port 0.	R

All bits are cleared after read and reset.

8.6 PORT LINK/PARTITION INTERRUPT MASK REGISTER (R/W)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Table 7-6.

BIT	NAME	DESCRIPTION	R/W
15	LM7	1:Mask Link Status change interrupt on Port 7. 0:Unmask Link Status change Interrupt on Port 7.	R/W
14	LM6	1:Mask Link Status change interrupt on Port 6. 0:Unmask Link Status change Interrupt on Port 6.	R/W
13	LM5	1:Mask Link Status change interrupt on Port 5. 0:Unmask Link Status change Interrupt on Port 5.	R/W
12	LM4	1:Mask Link Status change interrupt on Port 4. 0:Unmask Link Status change Interrupt on Port 4.	R/W
11	LM3	1:Mask Link Status change interrupt on Port 3. 0:Unmask Link Status change Interrupt on Port 3.	R/W
10	LM2	1:Mask Link Status change interrupt on Port 2. 0:Unmask Link Status change Interrupt on Port 2.	R/W
9	LM1	1:Mask Link Status change interrupt on Port 1. 0:Unmask Link Status change Interrupt on Port 1.	R/W
8	LM0	1:Mask Link Status change interrupt on Port 0. 0:Unmask Link Status change Interrupt on Port 0.	R/W
7	PM7	1:Mask Partition Status change interrupt on Port 7. 0:Unmask Partition Status change Interrupt on Port 7.	R/W
6	PM6	1:Mask Partition Status change interrupt on Port 6. 0:Unmask Partition Status change Interrupt on Port 6.	R/W
5	PM5	1:Mask Partition Status change interrupt on Port 5. 0:Unmask Partition Status change Interrupt on Port 5.	R/W
4	PM4	1:Mask Partition Status change interrupt on Port 4. 0:Unmask Partition Status change Interrupt on Port 4.	R/W
3	PM3	1:Mask Partition Status change interrupt on Port 3. 0:Unmask Partition Status change Interrupt on Port 3.	R/W
2	PM2	1:Mask Partition Status change interrupt on Port 2. 0:Unmask Partition Status change Interrupt on Port 2.	R/W
1	PM1	1:Mask Partition Status change interrupt on Port 1. 0:Unmask Partition Status change Interrupt on Port 1.	R/W
0	PM0	1:Mask Partition Status change interrupt on Port 0. 0:Unmask Partition Status change Interrupt on Port 0.	R/W

All bits are cleared after reset

8.7 DATA RATE MISMATCH/JABBER INTERRUPT (RO)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O7	O6	O5	O4	O3	O2	O1	O0	J7	J6	J5	J4	J3	J2	J1	J0

Table 7-7.

BIT	NAME	DESCRIPTION	R/W
15	O7	Set to '1' if Elastic Buffer Over/Underflow on Port 7.	R
14	O6	Set to '1' if Elastic Buffer Over/Underflow on Port 6.	R
13	O5	Set to '1' if Elastic Buffer Over/Underflow on Port 5.	R
12	O4	Set to '1' if Elastic Buffer Over/Underflow on Port 4.	R
11	O3	Set to '1' if Elastic Buffer Over/Underflow on Port 3.	R
10	O2	Set to '1' if Elastic Buffer Over/Underflow on Port 2.	R
9	O1	Set to '1' if Elastic Buffer Over/Underflow on Port 1.	R
8	O0	Set to '1' if Elastic Buffer Over/Underflow on Port 0.	R
7	J7	Set to '1' if Jabber occurs on Port 7.	R
6	J6	Set to '1' if Jabber occurs on Port 6.	R
5	J5	Set to '1' if Jabber occurs on Port 5.	R
4	J4	Set to '1' if Jabber occurs on Port 4.	R
3	J3	Set to '1' if Jabber occurs on Port 3.	R
2	J2	Set to '1' if Jabber occurs on Port 2.	R
1	J1	Set to '1' if Jabber occurs on Port 1.	R
0	J0	Set to '1' if Jabber occurs on Port 0.	R

All bits are cleared after read and reset.

8.8 DATA RATE MISMATCH/JABBER INTERRUPT MASK REGISTER (R/W)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O7	O6	O5	O4	O3	O2	O1	O0	J7	J6	J5	J4	J3	J2	J1	J0

Table 7-8.

BIT	NAME	DESCRIPTION	R/W
15	OM7	1:Mask Buffer Over/Underflow interrupt on Port 7. 0:Unmask Buffer Over/Underflow Interrupt on Port 7.	R/W
14	OM6	1:Mask Buffer Over/Underflow interrupt on Port 6. 0:Unmask Buffer Over/Underflow Interrupt on Port 6.	R/W
13	OM5	1:Mask Buffer Over/Underflow interrupt on Port 5. 0:Unmask Buffer Over/Underflow Interrupt on Port 5.	R/W
12	OM4	1:Mask Buffer Over/Underflow interrupt on Port 4. 0:Unmask Buffer Over/Underflow Interrupt on Port 4.	R/W
11	OM3	1:Mask Buffer Over/Underflow interrupt on Port 3. 0:Unmask Buffer Over/Underflow Interrupt on Port 3.	R/W
10	OM2	1:Mask Buffer Over/Underflow interrupt on Port 2. 0:Unmask Buffer Over/Underflow Interrupt on Port 2.	R/W
9	OM1	1:Mask Buffer Over/Underflow interrupt on Port 1. 0:Unmask Buffer Over/Underflow Interrupt on Port 1.	R/W
8	OM0	1:Mask Buffer Over/Underflow interrupt on Port 0. 0:Unmask Buffer Over/Underflow Interrupt on Port 0.	R/W
7	JM7	1:Mask Jabber interrupt on Port 7. 0:Unmask Jabber Interrupt on Port 7.	R/W
6	JM6	1:Mask Jabber interrupt on Port 6. 0:Unmask Jabber Interrupt on Port 6.	R/W
5	JM5	1:Mask Jabber interrupt on Port 5. 0:Unmask Jabber Interrupt on Port 5.	R/W
4	JM4	1:Mask Jabber interrupt on Port 4. 0:Unmask Jabber Interrupt on Port 4.	R/W
3	JM3	1:Mask Jabber interrupt on Port 3. 0:Unmask Jabber Interrupt on Port 3.	R/W
2	JM2	1:Mask Jabber interrupt on Port 2. 0:Unmask Jabber Interrupt on Port 2.	R/W
1	JM1	1:Mask Jabber interrupt on Port 1. 0:Unmask Jabber Interrupt on Port 1.	R/W
0	JM0	1:Mask Jabber interrupt on Port 0. 0:Unmask Jabber Interrupt on Port 0.	R/W

All bits are cleared after reset

8.9 ISOLATION/SA CHANGE INTERRUPT (RO)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0	S7	S6	S5	S4	S3	S2	S1	S0

Table 7-9.

BIT	NAME	DESCRIPTION	R/W
15	O7	Set to '1' if Isolation occurs on Port 7.	R
14	O6	Set to '1' if Isolation occurs on Port 6.	R
13	O5	Set to '1' if Isolation occurs on Port 5.	R
12	O4	Set to '1' if Isolation occurs on Port 4.	R
11	O3	Set to '1' if Isolation occurs on Port 3.	R
10	O2	Set to '1' if Isolation occurs on Port 2.	R
9	O1	Set to '1' if Isolation occurs on Port 1.	R
8	O0	Set to '1' if Isolation occurs on Port 0.	R
7	J7	Set to '1' if Source occurs on Port 7.	R
6	J6	Set to '1' if Source occurs on Port 6.	R
5	J5	Set to '1' if Source occurs on Port 5.	R
4	J4	Set to '1' if Source occurs on Port 4.	R
3	J3	Set to '1' if Source occurs on Port 3.	R
2	J2	Set to '1' if Source occurs on Port 2.	R
1	J1	Set to '1' if Source occurs on Port 1.	R
0	J0	Set to '1' if Source occurs on Port 0.	R

All bits are cleared after read and reset.

8.10 ISOLATION/SA CHANGE INTERRUPT MASK REGISTER (R/W)

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IM7	IM6	IM5	IM4	IM3	IM2	IM1	IM0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

Table 7-10.

BIT	NAME	DESCRIPTION	R/W
15	IM7	1:Mask Isolation interrupt on Port 7. 0:Unmask Isolation Interrupt on Port 7.	R/W
14	IM6	1:Mask Isolation interrupt on Port 6. 0:Unmask Isolation Interrupt on Port 6.	R/W
13	IM5	1:Mask Isolation interrupt on Port 5. 0:Unmask Isolation Interrupt on Port 5.	R/W
12	IM4	1:Mask Isolation interrupt on Port 4. 0:Unmask Isolation Interrupt on Port 4.	R/W
11	IM3	1:Mask Isolation interrupt on Port 3. 0:Unmask Isolation Interrupt on Port 3.	R/W
10	IM2	1:Mask Isolation interrupt on Port 2. 0:Unmask Isolation Interrupt on Port 2.	R/W
9	IM1	1:Mask Isolation interrupt on Port 1. 0:Unmask Isolation Interrupt on Port 1.	R/W
8	IM0	1:Mask Isolation interrupt on Port 0. 0:Unmask Isolation Interrupt on Port 0.	R/W
7	SM7	1:Mask SA Change interrupt on Port 7. 0:Unmask SA Change Interrupt on Port 7.	R/W
6	SM6	1:Mask SA Change interrupt on Port 6. 0:Unmask SA Change Interrupt on Port 6.	R/W
5	SM5	1:Mask SA Change interrupt on Port 5. 0:Unmask SA Change Interrupt on Port 5.	R/W
4	SM4	1:Mask SA Change interrupt on Port 4. 0:Unmask SA Change Interrupt on Port 4.	R/W
3	SM3	1:Mask SA Change interrupt on Port 3. 0:Unmask SA Change Interrupt on Port 3.	R/W
2	SM2	1:Mask SA Change interrupt on Port 2. 0:Unmask SA Change Interrupt on Port 2.	R/W
1	SM1	1:Mask SA Change interrupt on Port 1. 0:Unmask SA Change Interrupt on Port 1.	R/W
0	SM0	1:Mask SA Change interrupt on Port 0. 0:Unmask SA Change Interrupt on Port 0.	R/W

8.11 SAMPLE PERIOD REGISTER

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT15	CTI4	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

The 16-bit value which determines the length of the sample period in seconds in seconds in RMON f\history group is loaded into the sampling state machine whenever it is enabled. The maximum sampling window is 65536 seconds.

8.12 SAMPLE ENABLE REGISTER

msb lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SME

Table 7-9.

BIT	NAME	DESCRIPTION	R/W
15:1		Reserved.	
0	SME	1:This bit is used to enable the sampling state machine and is self-cleared at the end of the sampling period. 0:Sampling state machine is in the idle state. After reset, this bit is '0'.	R/W

8.13 XRC REGISTERS

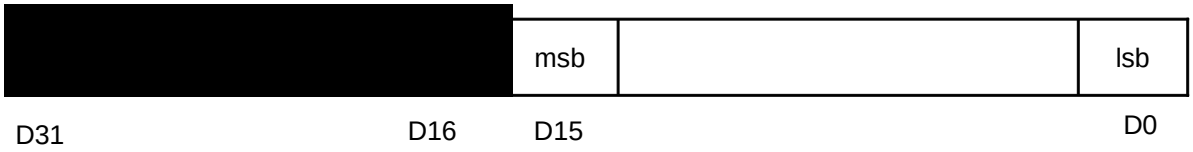
Refer to MX98741 XRC 100BASE TX/FX repeater specification Section 8.

8.14 BIT ACCESS ORDER

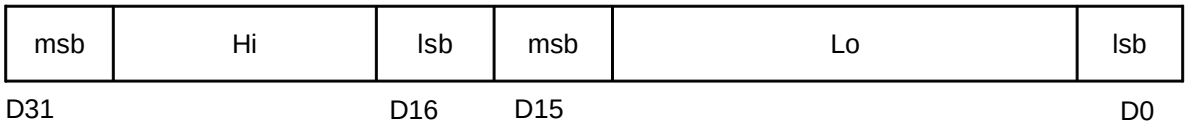
In the address table, 16-bit register format are used. However, the addresses are assigned in such a way that in 32-bit mode, on it RS[11:2] are needed, and in 8-bit mode, RS[11:0] are needed.

32-bit Access

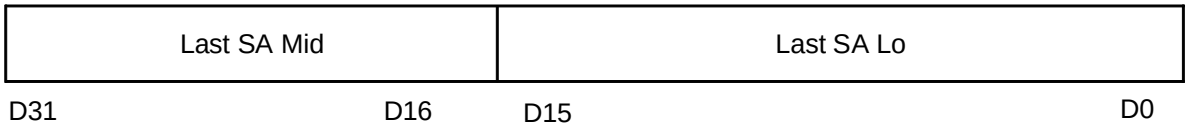
16-bit register access (RS 11='0')

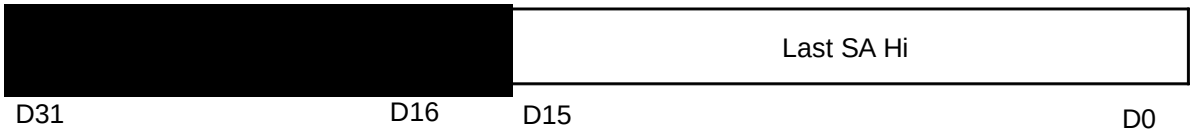


32-bit counter access (RS11='1')



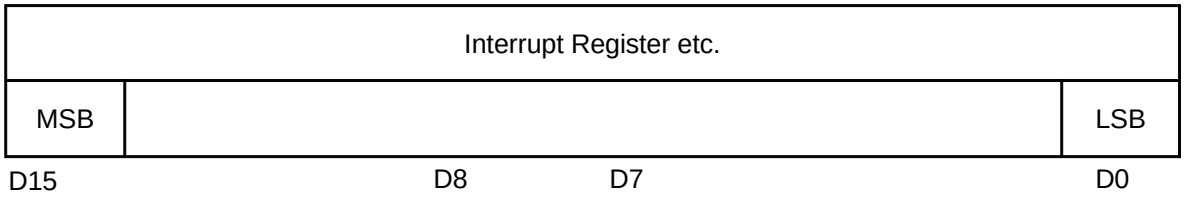
48-bit Last SA access



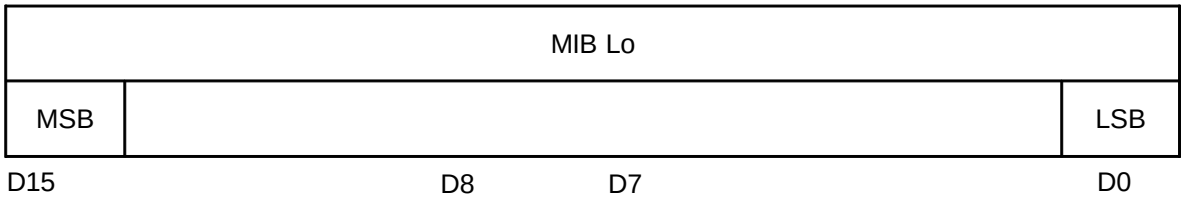


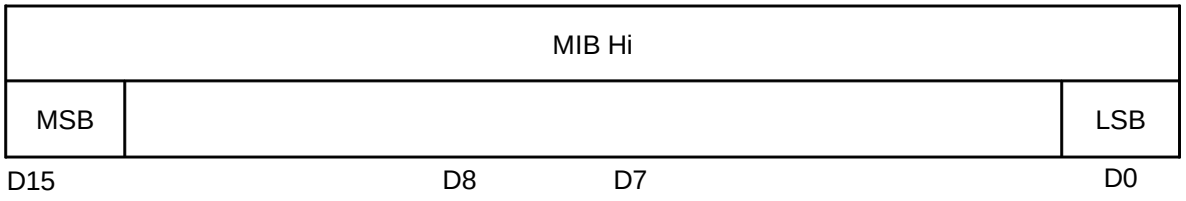
16-bit Access

16-bit Register Access



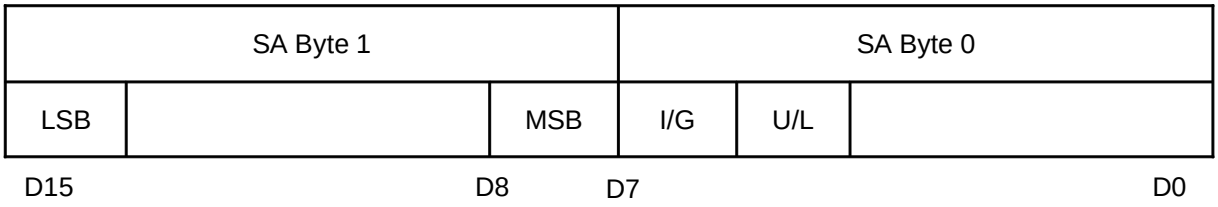
32-Bit Register Access



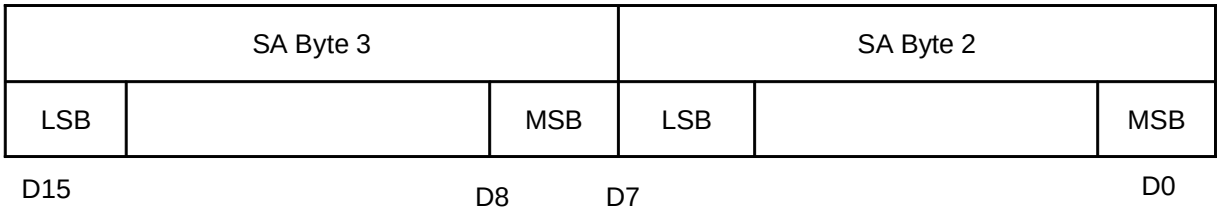


48-Bit Last SA Access

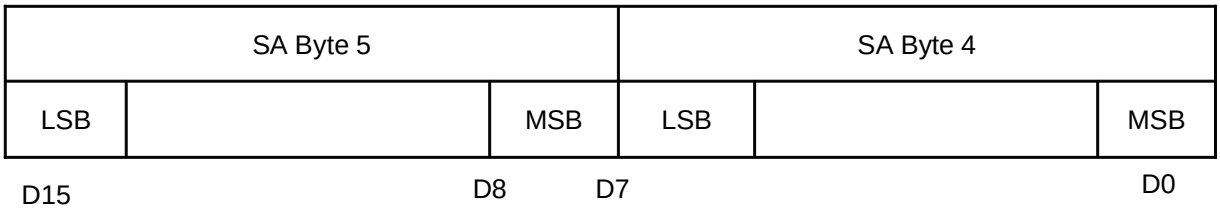
SA Lo



SA Mid

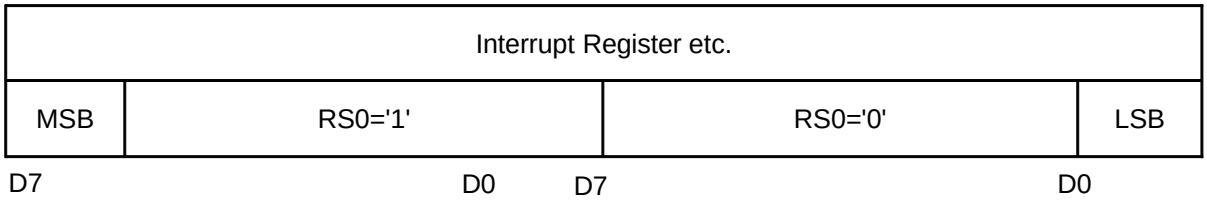


SA Hi

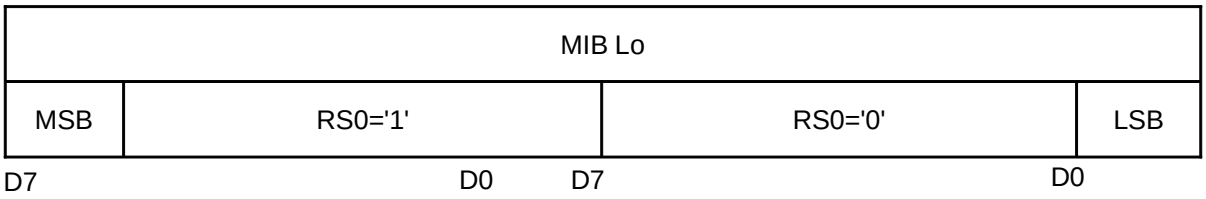


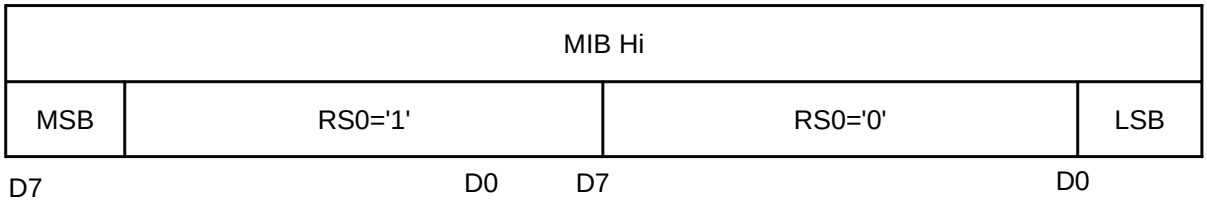
8-bit Access

16-bit Register Access



32-Bit Register Access



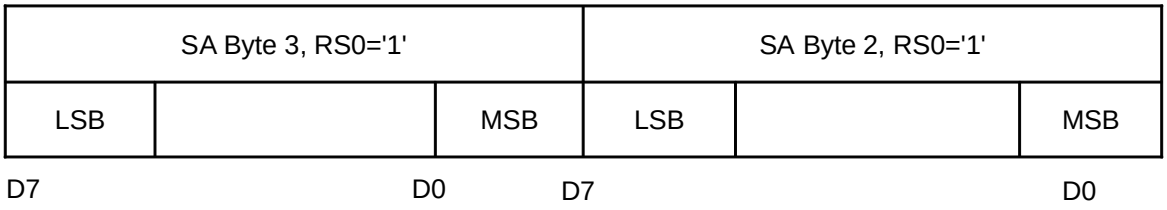


48-Bit Last SA Access

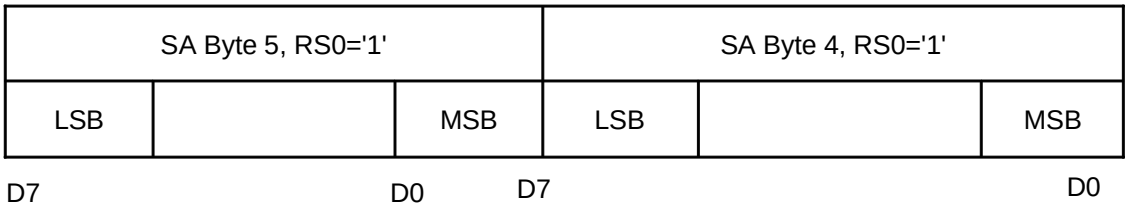
SA Lo



SA Mid



SA Hi



9.0 ABSOLUTE MAXIMUM RATINGS

Table 10-1. Absolute Maximum Ratings

RATING	VALUE
SupplyVoltage (VCC)	4.75 V to 5.25 V
DC Input Voltage (Vin)	-0.5 V to VCC + 0.5 V
DC Output Voltage (Vout)	-0.5 V to VCC + 0.5 V
Storage Temperature Range (TSTG)	-55C to 150 C
Power Dissipation (PD)	600 mW
ESD Rating (Rzap=1.5K, Czap=100pF)	2000 V

Note :

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Preliminary, subject to change.

10.0 DC CHARACTERISTICS

Table 10-1. Supply Current

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
ICC	Average Active (TXing/ RXing) Supply Current	VIN=Switching	-		mA
ICCIDLE	Average Idle Supply Current	COCLK=50 MHz VIN=VCC/GND	-	TBD (note)	mA
IDD	Static IDD Current	COCLK=Undriven	-	TBD (note)	uA

Note :

These two parameters will be measured while DC/AC characterization is proceeding.

Table 10-2. TTL Inputs, Outputs, Tri-States Excluding CPU Interface

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Vil	Maximum Low Level Input Voltage	GND=0V	-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	VCC + 0.5	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA
Voh	Minimum High Level Input Voltage	Ioh=-2mA	2.4	-	V
Vol	Maximum High Level Input Voltage	Iol=2mA	-	0.4	V
Ioz	Maximum Tri-State Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA

10-3. CPU Inputs/Outputs, Tri-State, Open-drain

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voh	Maximum High Level Input Voltage	Ioh=-4mA	2.4	-	V
Vol	Minimum Low Level Input Voltage	Ioh=-4mA		0.4	V
Vil	Minimum Low Level Input Voltage			0.8	V
Vih	Maximum High Level Input Voltage		2.0		V
Ioz	Maximum Tri-State Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA

11.0 AC CHARACTERISTICS

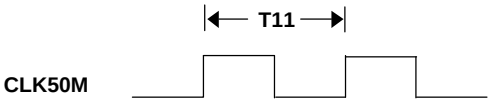


Figure 11-1. Clock CLK50M Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	SRAM bus clock period	20	33	ns

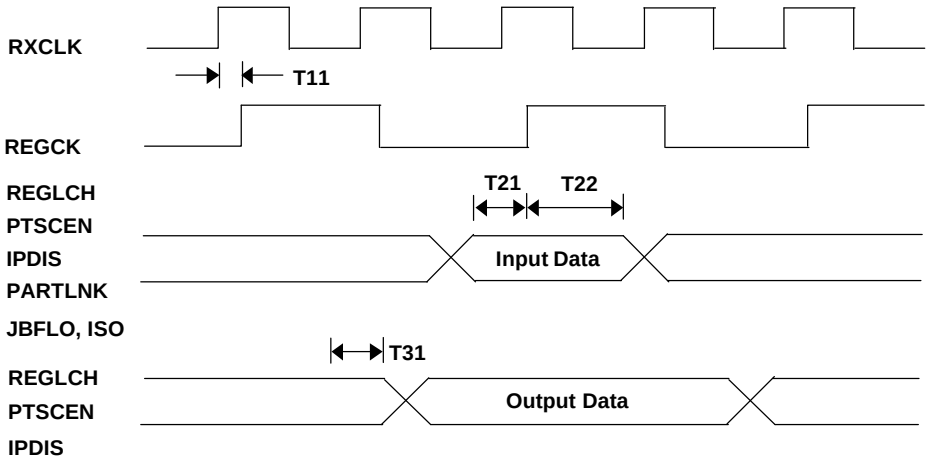


Figure 11-2. XRC Register Read & Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	RXCLK rising to REGCK high		6	ns
T21	PTSCEN setup time	10		ns
T22	PTSCEN hold ttime	10		ns
T31	REGCL low to PTSCEN valid		5	ns

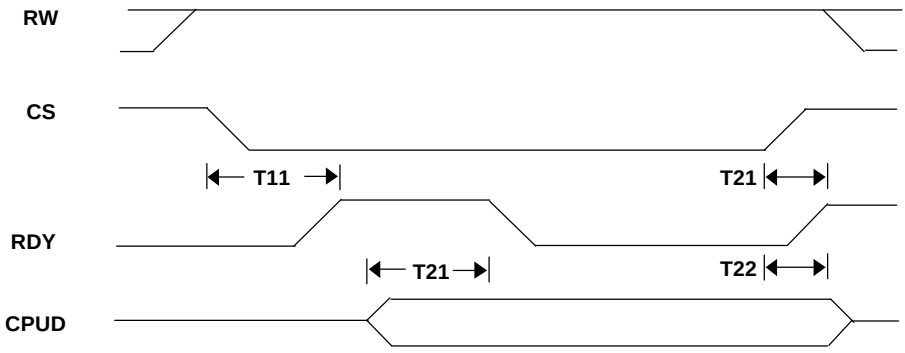


Figure 11-3. CPU Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	CS active to RDY high		6	ns
T12	CS inactive to RDY tristated		2	ns
T21	CPUD to RDY active setup time	70		ns
T22	CS inactive to CPUD tristated		2	ns

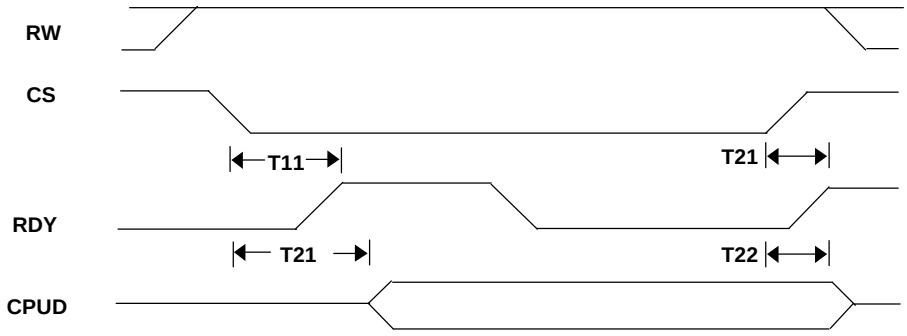


Figure 11-4. CPU Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	CS active to RDY high		6	ns
T12	CS inactive to RDY tristated		2	ns
T21	CPUD active to CPUD valid		40	ns
T22	CS inactive to CPUD hold time	6		ns

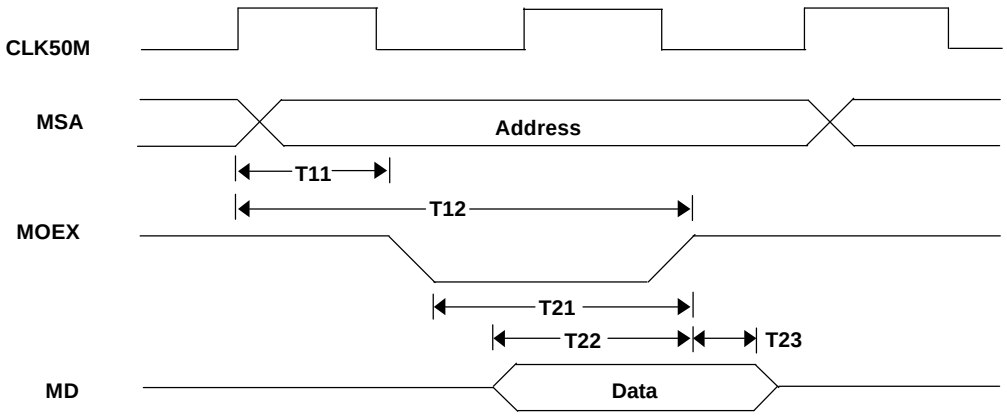


Figure 11-5. SRAM Buffer Read

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	MDA[12:0] MOEX asserted	1/2*TCLK-4		ns
T12	MSA[12:0] to MOEX inactive	3/2*TCLK-6		ns
T21	MOEX valid low pulse width	TCLK-2		ns
T22	MD valid to MOEX asserted setup time	5		ns
T23	MD to MOEX asserted hold time	0		ns

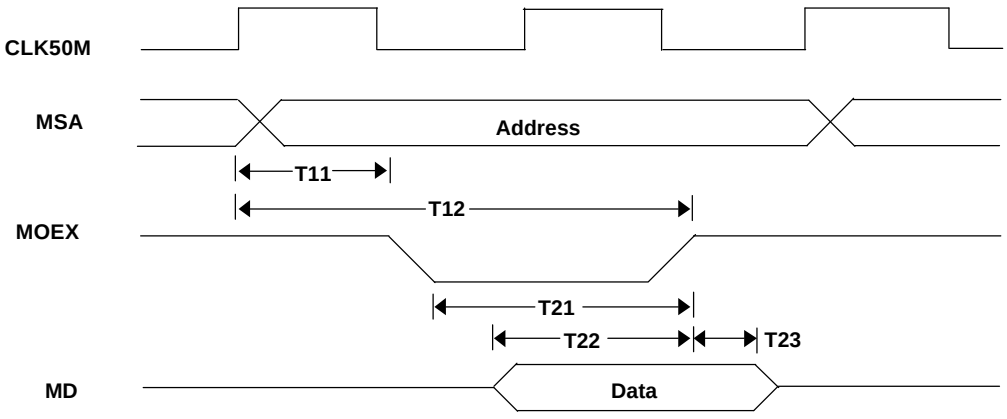


Figure 11-6. SRAM Buffer Write

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T11	MSA[12:0] MOEX asserted	1/2*TCLK-4		ns
T12	MSA[12:0] to MOEX inactive	3/2*TCLK-6		ns
T21	MOEX valid low pulse width	TCLK-2		ns
T22	MD valid to MWEX asserted setup time	3/2*TCLK-6		ns
T23	MWEX asserted to MD tristated	1/2*TCLK-4		ns

12.0 PACKAGE INFORMATION

144-PIN QUAD FLAT PACK

ITEM	MILLIMETERS	INCHES
A	31.2+/-0.3	1.228+/-0.12
B	28.0+/-0.1	1.102+/-.004
C	28.0+/-0.1	1.102+/-.004
D	31.2+/-0.3	1.228+/-0.12
E	22.75	0.896
F	2.63 [REF]	.103 [REF]
G	2.63 [REF]	.103 [REF]
H	0.30 [Typ.]	.012 [Typ.]
I	0.65 [Typ.]	.026 [Typ.]
J	1.60 [REF]	.063 [REF]
K	0.8+/-0.2	.031+/-.008
L	0.15 [Typ.]	.006 [Typ.]
M	0.10 max.	.004 max.
N	3.35 max.	.132 max.
O	0.10 min.	.004 min.
P	3.68 max.	.145 max.

Note:Each lead centerline is located within .25mm (.01 inch) of its true position [TP] at a maximum material condition.

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