F. Elastic Buffer Over/Underflow and Jabber Status Register (register #19) (R)

Bit(s)	Name	Description	R/W
19.15	EBOUF7	1 : Elastic Buffer Over/Underflow at Port 7 0 : Normal Condition. Clear to 0 by RESETL (or RESETP7).	R
19.14	EBOUF6	1 : Elastic Buffer Over/Underflow at Port 6 0 : Normal Condition. Clear to 0 by RESET (or RESETP6).	R
19.13	EBOUF5	1 : Elastic Buffer Over/Underflow at Port 5 0 : Normal Condition. Clear to 0 by RESET (or RESETP5).	R
19.12	EBOUF4	1 : Elastic Buffer Over/Underflow at Port 4 0 : Normal Condition. Clear to 0 by RESET (or RESETP4).	R
19.11	EBOUF3	1 : Elastic Buffer Over/Underflow at Port 3 0 : Normal Condition. Clear to 0 by RESET (or RESETP3).	R
19.10	EBOUF2	1 : Elastic Buffer Over/Underflow at Port 2 0 : Normal Condition. Clear to 0 by RESET (or RESETP2).	R
19.9	EBOUF1	1 : Elastic Buffer Over/Underflow at Port 1 0 : Normal Condition. Clear to 0 by RESET (or RESETP1).	R
19.8	EBOUF0	1 : Elastic Buffer Over/Underflow at Port 0 0 : Normal Condition. Clear to 0 by RESET (or RESETP0).	R

Table 5-6 Elastic Buffer Over/Underflow and Jabber Register Bit Definition

F. Elastic Buffer Over/Underflow and Jabber Status Register (register #19) (R) (Continued)

Bit(s)	Name	Description	R/W
19.7	JABP7	1 : Receive Jabber Active at Port 7 0 : No Jabber condition at Port 7	R
19.6	JABP6	1 : Receive Jabber Active at Port 6 0 : No Jabber condition at Port 6	R
19.5	JABP5	1 : Receive Jabber Active at Port 5 0 : No Jabber condition at Port 5	R
19.4	JABP4	1 : Receive Jabber Active at Port 4 0 : No Jabber condition at Port 4	R
19.3	JABP3	1 : Receive Jabber Active at Port 3 0 : No Jabber condition at Port 3	R
19.2	JABP2	1 : Receive Jabber Active at Port 2 0 : No Jabber condition at Port 2	R
19.1	JABP1	1 : Receive Jabber Active at Port 1 0 : No Jabber condition at Port 1	R
19.0	JABP0	1 : Receive Jabber Active at Port 0 0 : No Jabber condition at Port 0	R

Table 5-6 Elastic Buffer Over/Underflow and Jabber Register Bit Definition (Continued)

G. Isolation Status Register (register #20) (R)

Bit(s)	Name	Description	R/W
20.15	ISO7	1 : Port Isolation is occuring at port 7, 0 : Port Isolation is not occuring at port 7. Set to 1 by CIM state machine, cleared to 0 by asserting RESETL pin or writing to Port Reset Register or by CIM state machine.	R
20.14	ISO6	1 : Port Isolation is occuring at port 6, 0 : Port Isolation is not occuring at port 6.	R
20.13	ISO5	1 : Port Isolation is occuring at port 5, 0 : Port Isolation is not occuring at port 5.	R
20.12	ISO4	1 : Port Isolation is occuring at port 4, 0 : Port Isolation is not occuring at port 4.	R
20.11	ISO3	1 : Port Isolation is occuring at port 3, 0 : Port Isolation is not occuring at port 3.	R
20.10	ISO2	1 : Port Isolation is occuring at port 2, 0 : Port Isolation is not occuring at port 2.	R
20.9	ISO1	1 : Port Isolation is occuring at port 1, 0 : Port Isolation is not occuring at port 1.	R
20.8	ISO0	1 : Port Isolation is occuring at port 0, 0 : Port Isolation is not occuring at port 0.	R
20.7:0	Reserved	Ignored while read.	R

Table 5-7 Isolation Status Register Bit Definition

H. Isolation/Partition Disable Register (register #21) (R/W)

Bit(s)	Name	Description	R/W
21.15	ISODIS7	1 : Port 7 Isolation function is disabled 0 : Port 7 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.14	ISODIS6	1 : Port 6 Isolation function is disabled 0 : Port 6 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.13	ISODIS5	1 : Port 5 Isolation function is disabled 0 : Port 5 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.12	ISODIS4	1 : Port 4 Isolation function is disabled 0 : Port 4 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.11	ISODIS3	1 : Port 3 Isolation function is disabled 0 : Port 3 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.10	ISODIS2	1 : Port 2 Isolation function is disabled 0 : Port 2 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.9	ISODIS1	1 : Port 1 Isolation function is disabled 0 : Port 1 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.8	ISODIS0	1 : Port 0 Isolation function is disabled 0 : Port 0 Isolation function is not disabled. The default value is 0 after reset.	R/W

Table 5-8 Isolation/Partition Disable Register Bit Definition

H. Isolation/Partition Disable Register (register #21) (R/W)

Bit(s)	Name	Description	R/W
21.7	PARDIS7	1 : Port 7 Parition function is disbled. 0 : Port 7 Partition function is not disabled. The default value is 0 after reset.	R/W
21.6	PARDIS6	1 : Port 6 Parition function is disbled. 0 : Port 6 Partition function is not disabled. The default value is 0 after reset.	R/W
21.5	PARDIS5	1 : Port 5 Parition function is disbled. 0 : Port 5 Partition function is not disabled. The default value is 0 after reset.	R/W
21.4	PARDIS4	1 : Port 4 Parition function is disbled. 0 : Port 4 Partition function is not disabled. The default value is 0 after reset.	R/W
21.3	PARDIS3	1 : Port 3 Parition function is disbled. 0 : Port 3 Partition function is not disabled. The default value is 0 after reset.	R/W
21.2	PARDIS2	1 : Port 2 Parition function is disbled. 0 : Port 2 Partition function is not disabled. The default value is 0 after reset.	R/W
21.1	PARDIS1	1 : Port 1 Parition function is disbled. 0 : Port 1 Partition function is not disabled. The default value is 0 after reset.	R/W
21.0	PARDIS0	1 : Port 0 Parition function is disbled. 0 : Port 0 Partition function is not disabled. The default value is 0 after reset.	R/W

Table 5-8 Isolation/Partition Disable Register Bit Definition (Continued)

Note : Physical address input from ACTP[4:0] during RESETL is asserted will be stored at bit 4:0 of register #31.

6.0 ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Supply Voltage (VCC)	4.75V to 5.25V
DC Input Voltage (Vin)	-0.5V to VCC+0.5V
DC Output Voltage (Vout)	-0.5V to VCC+0.5V
Storage Temperature Range (TSTG)	-55 C to 150 C
Power Dissipation (PD)	750 mW
ESD rating (Rzap = 1.5K, Czap = 100pF)	2000V

Table 6-1 Absolute Maximum Rating for MX98741

Notice :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cauase permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Preliminary, Subject to change.

7.0 DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
A. Supply Current					
ICC	Average Active (TXing/ RXing) Supply Current	COCLK = 50MHz VIN = Switching	-	150	mA
ICCIDLE	Average Idle Supply Current	COCLK = 50MHz VIN=VCC/GND	-	TBD (Note)	mA
IDD	Static IDD Current	COCLK=Undriven	-	TBD (Note)	uA

Table 7-1 DC Characteristics for MX98741

Note : These two parameters will be measured while DC/AC characterization is proceeding.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
B. TTL Inputs, Outputs, Tri-States					
Vil	Maximum Low Level Input Voltage	GND = 0V	-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	VCC+0.5	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA
Voh	Minimum High Level Output Voltage	Ioh = -2mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 2mA	-	0.4	V
Ioz	Maximum TRI-STATE Output Leakage Current	VOUT=VCC/ GND	-10.0	10.0	uA
C. EXP Outputs, Tri-States					
Voh	Minimum High Level Output Voltage	Ioh = -4mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	-	0.4	V
Vil	Maximum Low Level Input Voltage		-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	-	V
Ioz	Maximum TRI-STATE Output Leakage Current	VOUT=VCC/ GND	-10.0	10.0	uA

Table 7-1 DC Characteristics for MX98741 (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
D. MII Inputs, Outputs, Tri-States					
Voh	Minimum High Level Output Voltage	Ioh = -8mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 8mA	-	0.4	V
Vil	Maximum Low Level Input Voltage		-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	-	V
Ioz	Maximum TRI-STATE Output Leakage Current	VOUT=VCC/ GND	-10.0	10.0	uA
***E.* TTL Input With Schmitt Trigger**					
Vil	Maximum Low Level Input Voltage		-	0.6	V
Vih	Minimum High Level Input Voltage		2.7	-	V

Table 7-1 DC Characteristics for MX98741 (Continued)

Note :
1.All parameters listed in category A/B/C/D are preliminary, subject to change. After wafer is out, the value measured on tester will be the finalized Voltage Characteristics.
2.For MII port, see item F in next page for one's reference.

SYMBOL	PARAMETER	Signals	MIN.	MAX.	UNIT
F. Input Current Limits for MII					
Iih	Input High Current with Vi = 5.25 Volt	All Except COL, MDC, MDIO (Note 1)	-	200	uA
		COL (NOTE 2)	-	20	uA
		MDC (NOTE 3)	-	20	uA
		MDIO (NOTE 4)	-	3000	uA
		MDIO (Note 5)	-	20	uA
Iil	Input Low Current with Vi = 0.00 Volt	All Except COL, MDC, MDIO (NOTE 1)	-20	-	uA
		COL (NOTE 2)	-200	-	uA
		MDC (NOTE 3)	-20	-	uA
		MDIO (NOTE 4)	- 180	-	uA
		MDIO (NOTE 5)	-3800	-	uA
Iiq	Input Quiescent Current with Vi = 2.4 Volt	MDIO (NOTE 4)	-	1450	uA
		MDIO (NOTE 5)	-1450	-	uA

Table 7-1 DC Characteristics for MX98741 (Continued)

Note1 : Measured at input of Reconcilation sublayer for CRSs, RXD[3:0], RXCLK, RXDVs, RXER, and TXCLK. Measured at inputs of XRC for TXD[3:0], TXEN, and TXER.
Note 2 : Measured at input of Reconciliation sublayer.
Note 3 : Measured at input of XRC.
Note 4 : Measured at input of STA.
Note 5 : Measured at input of XRC which cn be attached via the mechanical interface specified in section 22.6 in [1].

Caution : Input Current limit is only for board designer's reference. In MX98741, we will not use this specification to verify the input signals provided by stimulus patterns.

8.0 AC CHARACTERISTICS AND WAVEFORMS

A. Media Independent Interface

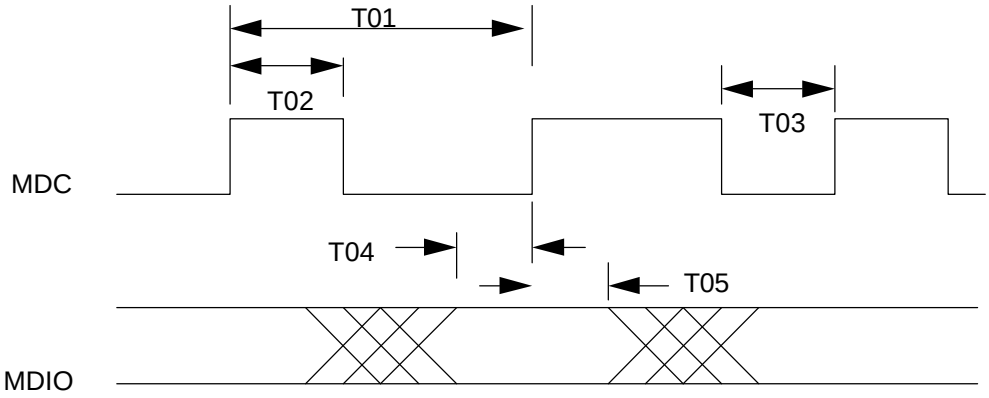

Figure 8-1 MDIO Timing Relationship to MDC

Symbol	Description	MIN.	MAX.	UNIT
T01	Period for MDC	400	-	ns
T02	High Time for MDC	160	-	ns
T03	Low Time for MDC	160	-	ns
T04	MDIO Setup to MDC rising edge (Write Command)	10	-	ns
T05a	MDIO Hold to MDC rising edge (Write Command)	10	-	ns
T05b	MDIO Hold to MDC rising edge (Read Command)	5	10	ns

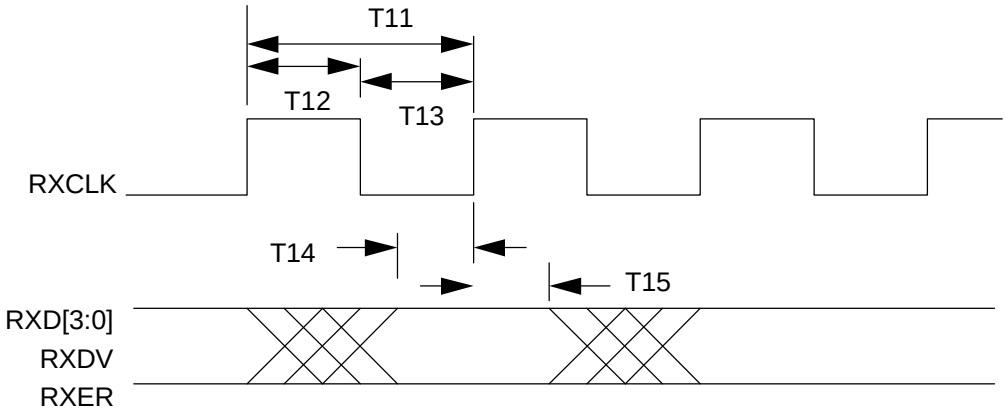

Figure 8-2 Receive Signal Timing Relationships at the MII

Symbol	Description	MIN.	MAX.	UNIT
T11	RXCLK Period (Note 1)	40	40	ns
T12	RXCLK High Time	19	-	ns
T13	RXCLK Low Time	17	-	ns
T14	RXD[3:0]/RXDVs/RXER Setup Time to RXCLK rising edge (Note 2)	10	-	ns
T15	RXD[3:0]/RXDVs/RXER Hold Time to RXCLK rising edge (Note 2)	15	-	ns

Note 1 : The accurate RXCLK frequency shall be 25 MHz +/- 100 ppm.

Note 2 : The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

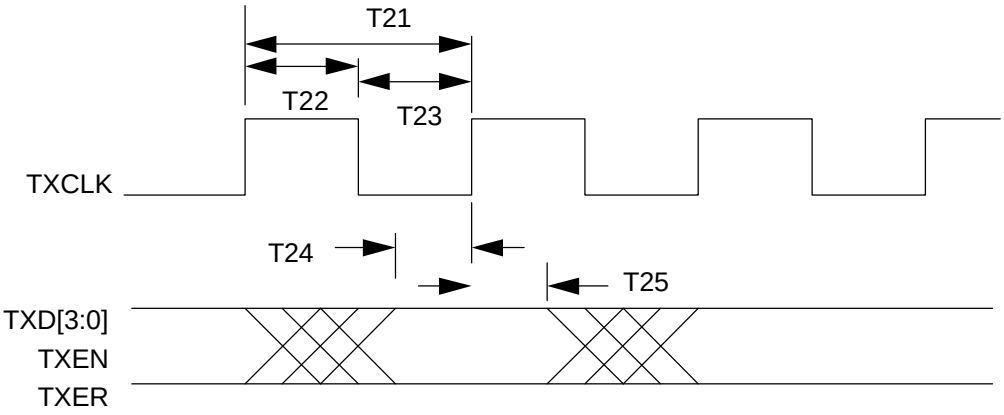

Figure 8-3 Transmit Signal Timing Relationships at the MII

Symbol	Description	MIN.	MAX.	UNIT
T21	TXCLK Period (Note 1)	40	40	ns
T22	TXCLK High Time	0.35*T21	0.65*T21	ns
T23	TXCLK Low Time	0.35*T21	0.65*T21	ns
T24	TXD[3:0]/TXENs/TXERs Setup Time to TXCLK rising edge (Note 2)	10	-	ns
T25	TXD[3:0]/TXENs/TXERs Hold Time to TXCLK rising edge (Note 2)	10	-	ns

Note 1 : The accurate TXCLK frequency shall be 25 MHz +/- 100 ppm.

Note 2 : The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

B. Data Transceiver Interface

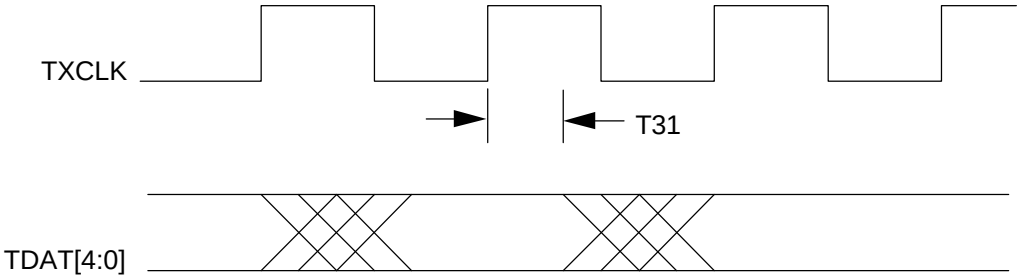

Figure 8-4 Transmit Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
T31	TDAT[4:0] to TXCLK Rise Delay Time	5	15	ns

Note : Tested under 30pF loading.

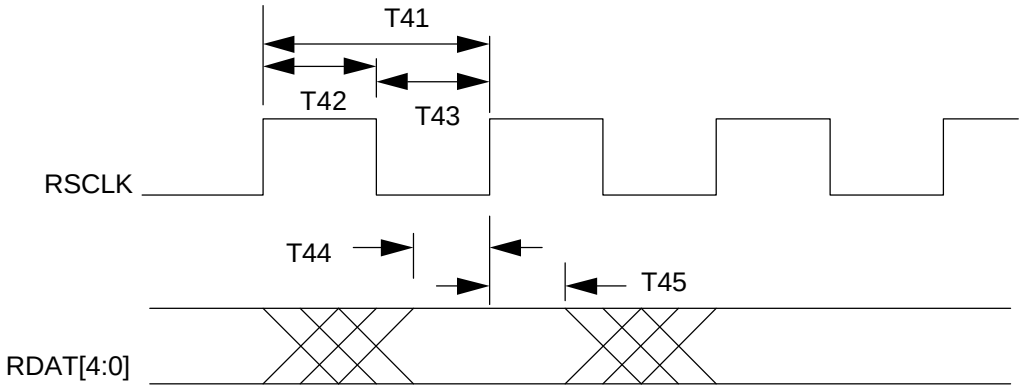

Figure 8-5 Receive Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
T41	RSCLK Period (Note 1)	40	40	ns
T42	RSCLK Pulse Width High	10	-	ns
T43	RSCLK Pulse Width Time	20	-	ns
T44	RDAT[4:0] Valid to RSCLK Rise	2	-	ns
T45	RSCLK Rise to RDAT[4:0] Invalid	4	-	ns

Note 1 : The accurate RXCLK frequency shall be 25 MHz +/- 100 ppm.

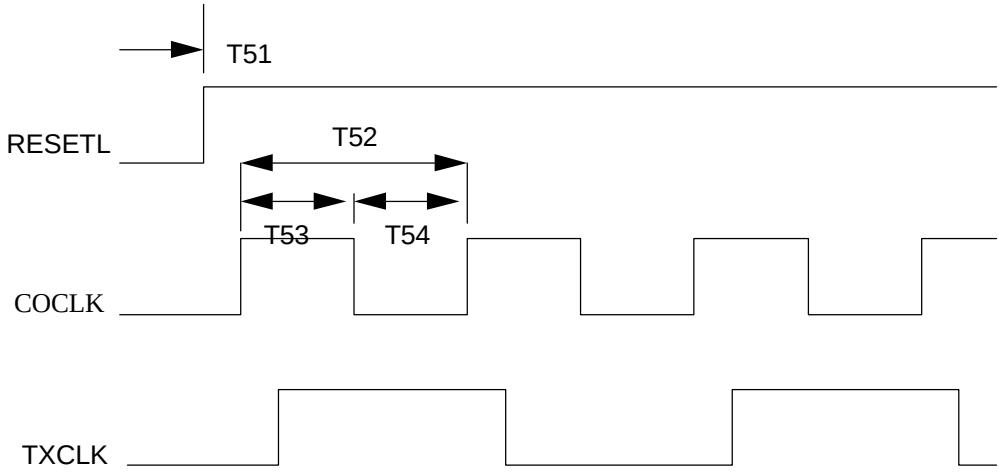

Figure 8-6 Timing Relationship for COCLK, TXCLK, and RESETL

Symbol	Description	MIN.	MAX.	UNIT
T51	Pulse Width for RESETL	2400	-	ns
T52	COCLK Period (Note 1)	20	20	ns
T53	COCLK Pulse Width High	8	-	ns
T54	COCLK Pulse Width Low	8	-	ns

Note 1 : The Maximum Frequency variation for COCLK shold be less than 100ppm.

D. Status Pins

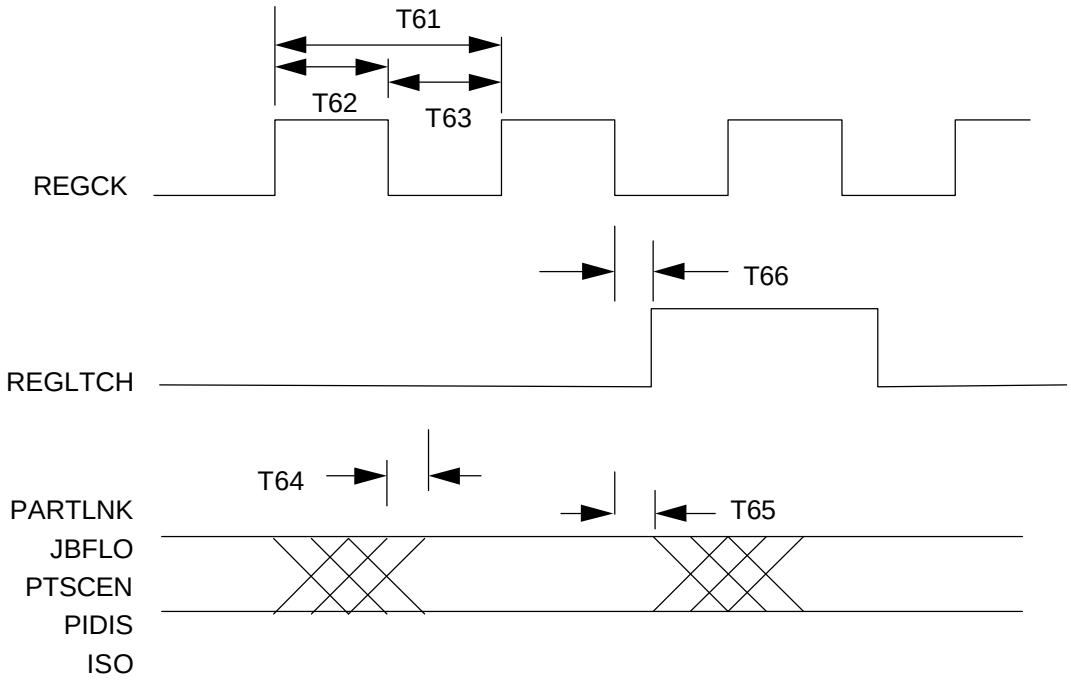

Figure 8-7 Timing Relationship for REGCK, REGLTCH and Round-Robin Status pins

Symbol	Description	MIN.	MAX.	UNIT
T61	REGCK Period	50	-	ns
T62	REGCK Pulse width High	12	-	ns
T63	REGCK Pulse Width LOW	12	-	ns
T64	REGCK falling to Status Valid	-	10	ns
T65	RegCK Falling to Status Invalid	-	12	ns
T66	REGCK falls to REGLTCH asserted (Note 1)	5	10	ns

Note 1 : One can use REGCK rising edge to latch data in system application.
Note 2 : Test under 30pF loading.

E. Network Interface Pins

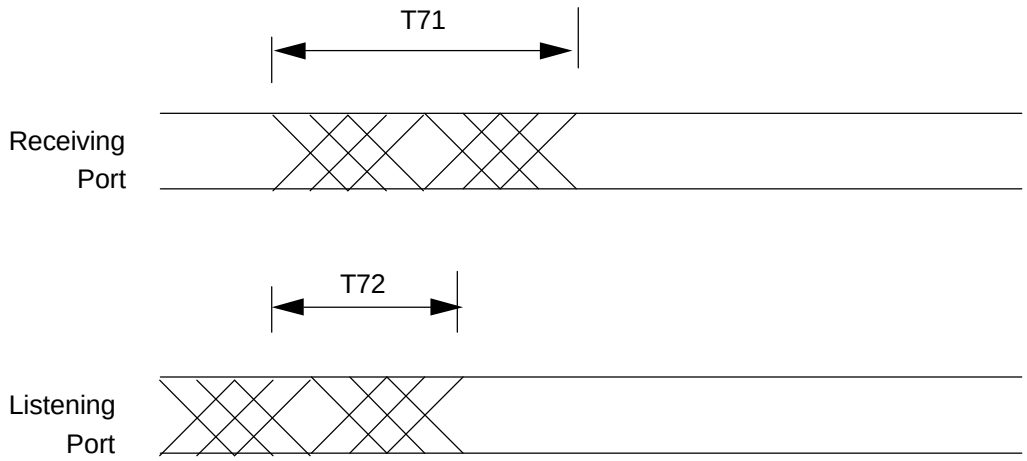

Figure 8-8 Port Activity Restriction Timing

Symbol	Description	MIN.	MAX.	UNIT
T71	Receiving Port goes to IDLE to activate again (Note)	100	-	ns
T72	Listening Port activate after other port IDLE (Note)	100	-	ns

Note : The restriction in IEEE 802.3u specifiction is 96BT. i.e 960 ns. Interframe Gap time less than the value shown above may cause packet loss and internal state machine malfunction.

F. Expansion Port Interface

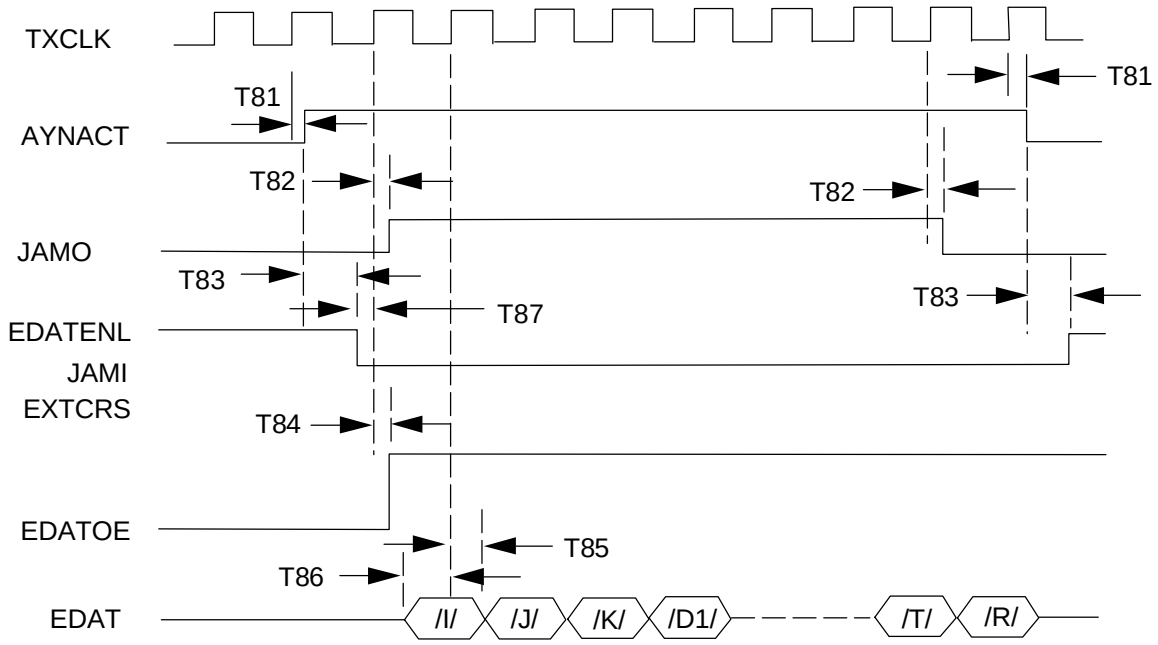

Figure 9-9 Expansion Port Timing Relationship

Symbol	Description	MIN.	MAX.	UNIT
T81	TXCLK rising to ANYACT assert/deassert	-	18	ns
T82	TXCLK rising to JAMO assert /deassert	-	13	ns
T83	ANYACT assert to EDATENL assert (Note)	-	17	ns
T84	TXCLK rising to EDATOE assert	-	25	ns
T85a	EDAT to TXCLK delay time (Output by MX98741)	12	26	ns
T85b	EDAT to TXCLK hold time (Input by MX98741)	4	-	ns
T86	EDAT to TXCLK setup time (Input by MX98741)	2	-	ns
T87	EDATENL asserted to TXCLK rising setup time	5	-	ns

Note :
If the external arbitor cannot generate EDATENL signals within 35 ns form TXCLK rising edge (or 17 ns after ANYACT is asserted in figure 9-9) for some reason, EDAT has to be delayed by one TXCLK cycle. Consequently, the longer the delay time changes the repeater from Class II to Class I. A 7ns PAL is suggested to be used for external arbitor to minimize the delay.

9.0 CHANGES MADE FOR REVISION 1.4 (NOV. 7, 1996)

1. P.13 : 5.2 Internal Registers, register 0, 1, and 16 can only be accessed through MDC and MD10.

2. P.21 : Delete the redundant page.

3. P.35 : Figure 8-6, delete T55.

4. P.38 : Figure 9-9, EDAT to TXCLK setup/hold time and EDATENL to TXCLK rising edge setup time are added.

10.0 PACKAGE INFORMATION

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