MX98741

XRC
100 BASE-TX/FX
Repeater Controller

1.0 FEATURES

* Eight 100 BASE-TX/FX ports; each port individually configurable to TX or FX
* Direct interface with analog clock generation/recovery chips
* Three Media Independent Interface (MII)
* Expandable to increase number of repeater ports
* Low latency design simplified high port number Class II repeater implementation
* Management features accessible through MII or serial ports
* All ports can be separately isolated or partitioned in reponse to fault conditions
* Conforms to IEEE 802.3u Repeater Unit Specification
* LED display for TX/FX port activities and collisions
* 208-pin, CMOS device in PQFP package

2.0 GENERAL DESCRIPTION

The MX98741 (100BASE-TX Repeater Controller, XRC) is a 208-pin PQFP device that interfaces directly with offshell clock generation/recovery chips. Eight ports can be configured as 100 BASE-TX or FX ports individually. Three additional ports have Media Independent Interfaces (MII) which allow easy connection of management and bridge devices. The expansion port allows multiple XRCs to be linked together to form a repeater of high port counts. LEDs are provided for visual monitoring of TX/FX port activities and collisions.

The XRC's design inserts minimum delay between the TX/FX ports and the expansion port. A master-slave type arbitration is also implemented to shorten the communciation time among multiple XRCs. As a result, design for Class II stackable hub is greatly simplified.

Control Functions and management status are implemented through internal registers. These registers are accessed via either standard MII management interface (MDC, MDIO) or several serial ports. These serial ports are accessed easily by hardware for debugging and configuration purposes. A dedicated management chip can also utilize these serial ports to access the XRC.

3.0 PIN CONFIGURATION

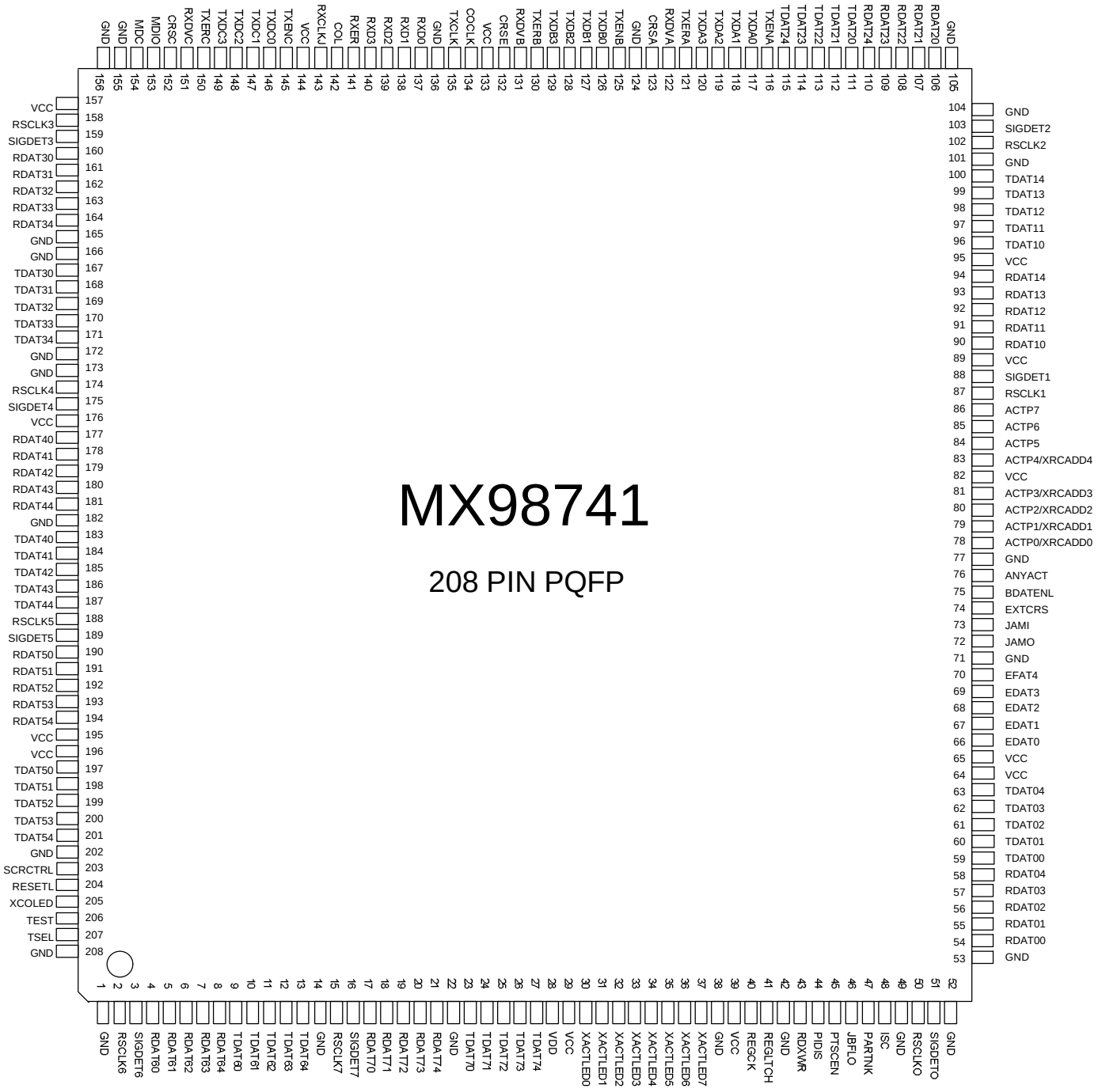

Figure 3-1 Pin Configuration for MX98741

4.0 PIN DESCRIPTION

A. MX Data Transceiver (Am78965/Am78966 or MC68836), 98 pins			
PAD #	**Name**	**I/O**	**Description**
59-63 96-100 111-115 167-171 183-187 197-201 9-13 23-27	TDAT[0:7][0:4]	O, EXP	**Transmit Data**. These five outputs are 4B/5B encoded transmit data symbols, driven at the rising edge of TXCLK. TDAT4 is the Most Significant Bit.
135	TXCLK	I, TTL	**Transmit Clock**. This pin supplies the frequency reference to the transmit logic. It should be driven by an external 25 MHz crystal-controlled clock source.
54-58 90-94 106-110 160-164 177-181 190-194 4-8 17-21	RDAT[0:7][0:4]	I, TTL	**Receive Data**. These 5-bit parallel data symbols from transceiver are latched by the rising edge of RSCLK. RDAT4 is the Most Significant Bit.
50,87 102,158 174,188 2,15	RSCLK[0:7]	I, TTL	**Recovered Sumbol Clock**. This is a 25 MHz clock, which is derived from the clock synchroniztion PLL circuit.
51,88 103,159 175,189 3,16	SIGDET[0:7]	I, TTL	**Signal Detect**. This signal indicates that the received signal is above the detection threshold and will be used for the link test state machine.
134	COCLK	I, TTL	**Core Clock**. 50M Clock input used by Repeater Core.

Table 4-1 Pin Description for MX98741

B. Expansion Port, 18 pins			
PAD #	**Name**	**I/O**	**Description**
72	JAMO	O, TTL	**Forced Jam Out**. Active High. The OR'd forced jam signals (exclude JAMI input) controlled by Carrier Integrity Monitor of each port. If collision occurs inside the XRC, this pin is also asserted.
73	JAMI	I, Schm	**Forced Jam Input**. Active High. Asserted by external arbiter, and XRC will generate JAM patterns to all its ports. Note : Glitch on JAMI and EDATENL may cause internal state machine malfunction.
75	EDATENL	I, Schm	**Enable Expansion Data**. Active Low. Asserted by an external arbitor. XRC will drive data into EDAT.
66-70	EDAT[0:4]	I/O, EXP	**Expansion Data**. Bidirectional 5-bit wide data. By default, EDAT is an input. When EDATENL is low, EDAT changed from input mode to output mode. Internally pull-up.
84-86	ACTP[5:8]	O, TTL	**Activity Out**. This is the activity of port 5..8 synchronous to COCLK (50M clock used by core). It also serves as data framing signal for the packet on EDAT. ACTP leads EDAT's /J/K/ pattern by more than 80 ns and deasserted 40ns after the /T/R/ or the last byte of jam patterns.
78-81, 83	ACTP[0:4] /XRCADD[0:4]	I/O, TTL	**Activity Out/Physical Address**. When RESETL goes high, value on ACTP[0;4] will be latched into internal buffer as physical address of XRC. After reset, these five pins have the same function as ACTP[5:8].
76	ANYACT	O, TTL	**Any Activity**. Active High. The OR'd ACTP[7:0] and TXEN A to C. This is used as an indication that an XRC is ready to drive data into EDAT.
74	EXTCRS	I, Schm	**External Carrier Sense**. Active high. Asserted by an external arbitor indicating activity from other XRC's at the expansion port.
C. Miscellaneous Pins, 2 pins			
204	RESETL	I, Schm	**Reset**. Active Low. This signal is output by the system to reset all the logic on the chip.

Table 4-1 Pin Description for MX98741 (Continued)

C. Miscellaneous Pins, 2 pins (Continued)			
203	SCRCTRL	I, TTL	**Scrambler Control**. If high, the scrambler/descrambler of each port is individually controlled by MII register 17. If low, the scrambler/descrambler is bypassed in all the ports.
D. Register Access Pins, 8 pins			
PAD #	**Name**	**I/O**	**Description**
47	PARTLNK	O, TTL	**Partition/Link Status**. This pin shows the status of internal register #18 in round-robin fashion starting at port 0 partition status and ending at port7 Link Status after REGLTCH is deasserted.
46	JBFLO	O, TTL	**Jabber/Buffer Status**. This pin shows the status of internal register #19 in round-robin fashion starting at port 0 Jabber Status and ending at port 7 Elastic Buffer Over/Underflow Status after REGLTCH is deasserted.
45	PTSCEN	I/O, TTL	**Port/Scrambler Enable**. If RDXWR is high, each port's enable/disable status (register #17) will be displayed at the rising edge of REGCK in round-robin fashion starting at port 0 Port 0 Enable status and ending at port 7 Scrambler Enable status after REGLTCH is deasserted. If RDXWR is low, 16-bit data can be written into the XRC at the rising edge of REGCK in round-robin fashion starting at port 0 Port Enable Signal and ending at port 7 Scrambler enable after REGLTCH is asserted high. Internally pull-up.
44	PIDIS	I/O, TTL	**Partition/Isolation Disable**. If RDXWR is high, each port's partition/Isolation Disable status will be displayed at the rising edge of REGCK in round-robin fashion starting at port 0 partition disable status and ending at port7 Isolation Disable status after REGLTCH is deasserted. If RDXWR is low, 16-bit data can be written into the XRC at the rising edge of REGCK in round-robin fashion starting at port 0 partition disable status and ending at port 7 Isolation disable status after REGLTCH is asserted high. Internally pull-down.

Table 4-1 Pin Description for MX98741 (Continued)

D. Register Access Pins (Continue)			
PAD #	**Name**	**I/O**	**Description**
48	ISO	O, TTL	**Isolation**. Active High. Each port's isolation status will be displayed at the rising edge of REGCK in round-robin fashion starting at port0 after REGLTCH is deasserted.
43	RDXWR	I, TTL	**Read/Write**. High indicates "Read" mode; register is being read out. REGLTCH is output. Low indicates "Write" mode; control registers are being written and REGLTCH is input. When RDXWR is programmed to "Write" Mode, internal "Read" status machine will be reset immediately.
41	REGLTCH	I/O, TTL	**Register Latch**. An output if RDXWR is high; an input if RDXWR is low. At the rising edge of REGCK, PARTLNK, JBFLO, PTSCEN, PIDIS, ISO display bit 0 status of corresponding registers, at the rising edge of next REGCK, bit 1 status is displayed, etc. After bit 15 is displayed, REGLTCH is asserted at the rising edge of next REGCK. Note : Both Data and REGLTCH are driven at the falling edge of REGCK inside the XRC. To make sure the data setup time, it is strongly recommended that the frequency of REGCK is below 12.5 MHz. Internally pull-down.
40	REGCK	I, TTL	**Register Clock**. A clock used as reference to display various status of each port or to latch control information inside XRC. The recommended clock's frequency is below 12.5M Hz.
E. LED Pins, 9 pins			
30-37	XACTLED[0:7]	O, TTL	**Activity LED**. Active Low. This pin provides a minimum 80ms ON time (low) and 20ms OFF time (high) for activities on each port. External buffers are necessary to drive LEDs.
205	XCOLED	O, MII	**Collision LED**. This pin is capable of driving LED directly to display Activity status. The ON (active low) time and OFF (active high) time of LED's is 80ms and 20ms respectively.

Table 4-1 Pin Description for MX98741 (Continued)

F. Media Independent Interface (MII), 33 pins			
PAD #	**Name**	**I/O**	**Description**
116	TXENA	I, TTL	**Transmit Enable MII A**. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
117-120	TXDA[0:3]	I, TTL	**Transmit Data MII A**. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENA is asserted, TXDA[3:0] are also driven by the MAC. While TXENA is de-asserted, the value of TXDA[3:0] is ignored. TXDA3 is the Most Significant Bit.
121	TXERA	I, TTL	**Transmit Error MII A**. Synchronous to the TXCLK's rising edge. When TXERA is asserted for one or more TXCLK period while TXENA is also asserted, one or more "HALT" symbols will present at TDAT4_0.
122	RXDVA	O, TTL	**Receive Data Valid MII A**. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame delimiter. High impedance after reset.
123	CRSA	O, TTL	**Carrier Sense MII A**. In TX mode, synchronous to RXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. High impedance after reset.
153	MDIO	I/O, TTL	**Management Data Input/Output**. A bi-directional signal. After reset, this pin is in high-impedance state. The selection of input/output direction is based on IEEE 802.3u management functions (Section 22.2.4). Low after reset due to internally pull-down. When RDXWR is low (i.e. Write operation, MDIO will be forced to low to disable the function of MDC and MDIO. i.e. Programming internal registers through register access pins owns higher priority.

Table 4-1 Pin Description for MX98741 (Continued)

F. Media Independent Interface (MII, Continued)			
PAD #	**Name**	**I/O**	**Description**
125	TXENB	I, TTL	**Transmit Enable MII B**. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
126-129	TXDB[0:3]	I, TTL	**Transmit Data MII B**. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENB is asserted, TXDB[3:0] are also driven by the MAC. While TXENB is de-asserted, the value of TXDB[3:0] is ignored. TXDB3 is the Most Significant Bit.
130	TXERB	I, TTL	**Transmit Error MII B**. Synchronousto the TXCLK's rising edge. When TXERB is asserted for one or more TXCLK period while TXENB is also asserted, one or more "HALT" symbols will present at TDAT4_0.
131	RXDVB	O, TTL	**Receive Data Valid MII B**. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter. High impedance after reset.
132	CRSB	O, TTL	**Carrier Sense MII B**. In TX mode, synchronous to RXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. High impedance after reset.
145	TXENC	I, TTL	**Transmit Enable MII C**. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
146-149	TXDC[0:3]	I, TTL	**Transmit Data MII C**. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENC is asserted, TXDC[3:0] are also driven by the MAC. While TXENC is de-asserted, the value of TXDC[3:0] is ignored. TXDC3 is the Most Significant Bit.

Table 4-1 Pin Description for MX98741 (Continued)

F. Media Independent Interface (MII, Continued)			
PAD #	**Name**	**I/O**	**Description**
150	TXERC	I, TTL	**Transmit Error MII C**. Synchronousto the TXCLK's rising edge. When TXERC is asserted for one or more TXCLK period while TXENC is also asserted, one or more "HALT" symbols will present at TDAT4_0
151	RXDVC	O, TTL	**Receive Data Valid MII C**. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter. High impedance after reset.
152	EDATACT	O, TTL	**Expansion DATa Activity**. When XRC is outputing data onto expansion EDAT, this pin will be asserted high. User can use this pin to control external EDAT bus switch in case multiple HUBs application is necessary.
141	RXER	O, EXP	**Receive Error**. Synchronous to RXCLK's rising edge. While RXDV is asserted, i.e. a frame is being received, this signal is asserted if any coding error is detected. High-impedence after reset.
143	RXCLK	O, MII	**Receive Clock MII**. 25 MHz continuous clock that provides the timing reference for the transfer of the RXDV, RXD and RXER signals. High-impedance after reset.
137-140	RXD[0:3]	O, MII	**Receive Data MII**. Synchronous to RXCLK's rising edge. For each RXCLK period in which RXDV is asserted, RXD[3:0] should be latched by the MAC. While RXDV is deasserted, RXD[3:0] are the nibbles 5B/4B decoded from RDAT[4:0]. RXD3 is the Most Significant Bit. High-impedance after reset.
142	COL	O, EXP	**Collision MII**. This signal is asserted if both the receiving media and TXEN are active. High-impedance after reset.
154	MDC	I, TTL	**Management Data Clock**. The timing reference for MDIO. The minumum high and low times are 200 ns each. No limitation on the maximum high and low time.

Table 4-1 Pin Description for MX98741 (Continued)

G. Power/Ground/Test/Loopback, 39 pins			
206	TEST	I, TTL	**Test**. Industrial test pin. Set to 0 or left unconnected for normal operation. When programmed to logic 1, XRC is in test mode. Internal Pulldown.
207	TSEL	I, TTL	**Test Mode Select**. When TEST is high and TSEL is low, XRC is in "Real Time Counter" Mode; when TEST is high and TSEL is high, XRC is in "Test Mode Counter" mode. Internally pull down.
1,14,22, 38,42,49 52,53,71, 77,101 104,105, 124,136, 155,156, 165,166, 173,182, 202,208	GND		**Ground**.
28,29, 39,64, 65,82, 89,95, 133,144, 157,176, 195,196	VCC		**5V Power Supply**.

Table 4-1 Pin Description for MX98741 (Continued)

5.0 FUNCTIONAL & OPERATION DESCRIPTION

5.1 MINIMUM AND MAXIMUM MODE APPLICATION

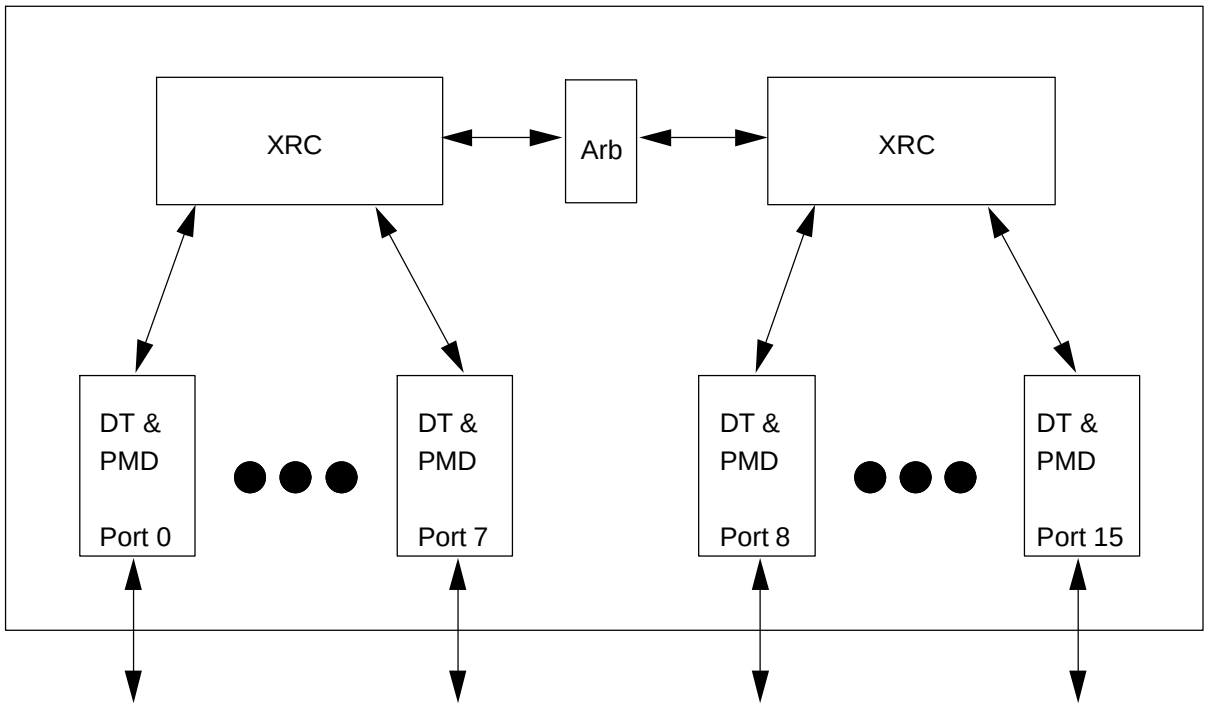

Figure 5-1 Minimum Mode operation for XRC

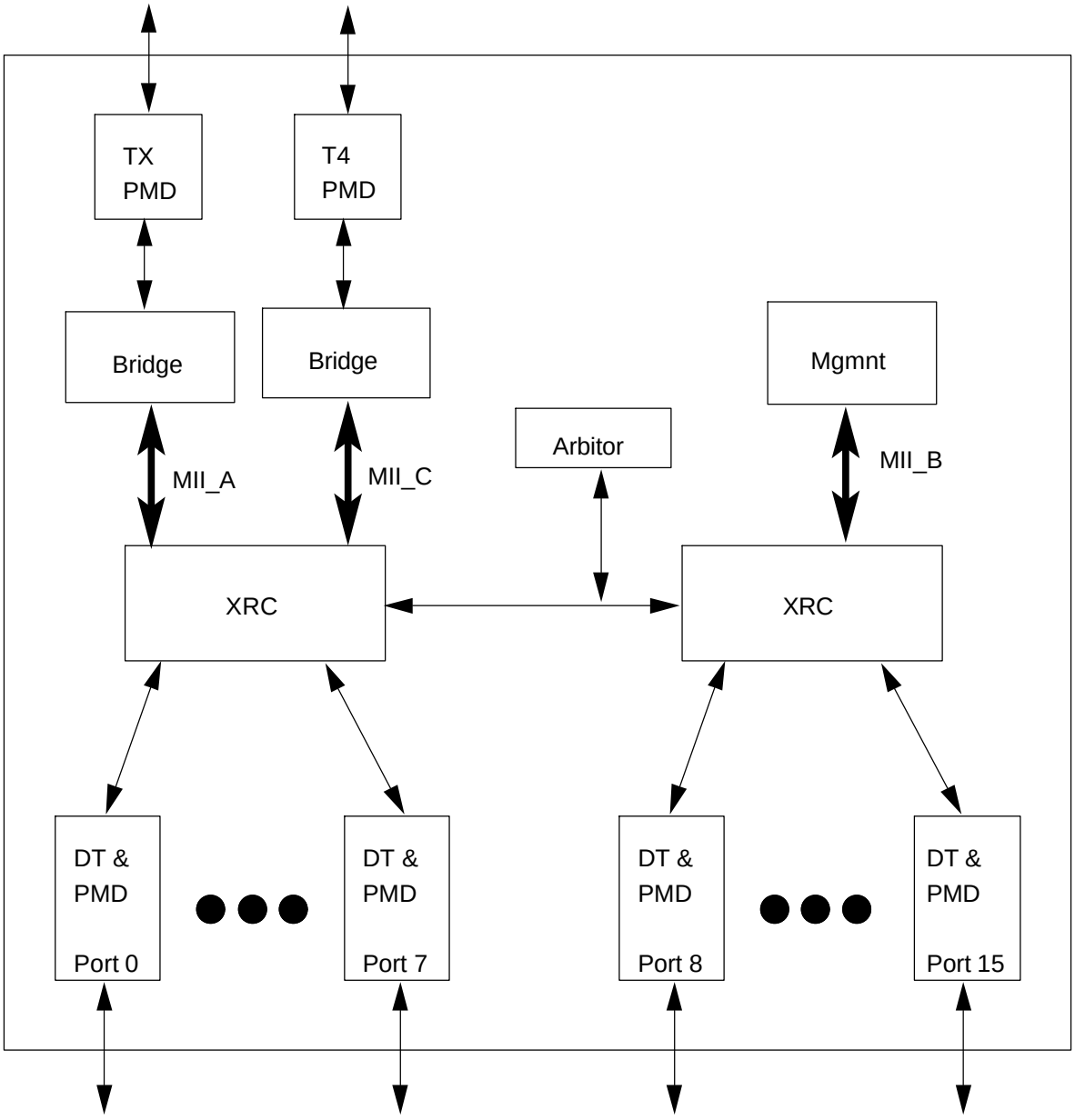

Figure 5-2 Maximum Mode operation for XRC

5.2 INTERNAL REGISTERS

There are two ways to access the XRC internal registers.

All the registers can be accessed through MII's MDC and MDIO. Although XRC connects to multiple 100-TX PHY's, they are all identical. Each XRC has only one PHY address as defined by ACTP[4:0] pins. If multiple XRC's are on the same MDIO bus, each of them should have different PHY address. Other non-XRC PHY devices (e.g. T4) are also allowed to be managed with the same management interface as long as PHY address of each device is distinct.

Another way to access registers is through register access pins. Register 17 (Scrambler Enable and Port Enable), Register 18 (Link Status, Partition Status), Register 19 (Elastic Buffer Status and Jabber Status), Register 20 (Isolation Status), Register 21 (Isolation Disable and Partition Disable) can also be read through PTSCEN, PARTLNK, JBFLO, ISO and PIDIS, respectively. The exception are register 0 (Command Register), register 1 (Status Register), and register 16 (Port Reset Register) which can only be accessed through MDC and MDIO. The register access pins facilitate a simple read/write protocol suitable for hardware-only configuration and status display design.

A. Command Register (register #0) (R/W)

Bit(s)	Name	Description	R/W
0.15	Reset	1 : PHY reset. A 240ns reset pulse will be generated to reset XRC internal logic. 0 : normal operation.	R/W SC
0.14	Loop Back	1 : enable loopback mode. 0 : disable loopback mode. The default setting is 0.	R/W
0.13	Speed Selection	Forced to 1 and indicate 100 Mb/s. Write 0 to this bit has no effect.	R
0.12	Auto-Negotiation Enable	Forced to 0 and indicate that Auto-Negotiation process is disabled. Write 1 to this bit has no effect.	R

Table 5-1 Control Register Bit Definition

A. Command Register (register #0) (R/W) (Continued)

Bit(s)	Name	Description	R/W
0.11	Power-Down	1 : power-down. COCLK and TXCLK for each port will be disabled. Clock for Management Block will keep running. During power-down, all state machines will be reset to its default state. 0 : normal operation.	R/W
0.10	Isolate	1 : electrically Isolate PHY from MII 0 : normal operation	R/W
0.9	Restart Auto-Negotiation	Forced to 0 and indicate that Auto-Negotiation process is disable. Write 1 to this bit has no effect.	R
0.8	Duplex Mode	Forced to 0 and indicate that only Half Duplex is available. Write 1 to this bit has no effect.	R
0.7	Collision Test	1 : enable COL signal test. The PHY will assert the COL signal within 5120 ns in response to the assertion of TXEN. While this bit is set to one, the PHY will deassert the COL signal within 40 ns in response to the deassertion of TXEN. 0 : normal operation. Set to 0 after power on reset.	R/W
0.6:0	Reserved	Value 0 will be read when one tries to read these bits.	R

Table 5-1 Control Register Bit Definition

B. Status Register (register #1) (R)

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	Forced to 0 and indicates that XRC is not able to perform 100BASE-T4.	R
1.14	100BASE-X Full Duplex	Forced to 0 and indicates that XRC is not able to perform 100BASE-X Full Duplex.	R
1.13	100BASE-X Half Duplex	Forced to 1 and indicates that XRC is able to perform 100BASE-X Half Duplex.	R
1.12	10 Mb/s Full Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Full Duplex.	R
1.11	10 Mb/s Half Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Half Duplex.	R
1.10:6	Reserved	Value 0 will be released by XRC when read.	R
1.5	Auto-Negotiation Complete	Forced to 0.	R
1.4	Remote Fault	Forced to 0.	R
1.3	Auto-Negotiation Ability	Forced to 0.	R
1.2	Link Status	1 : All ports are link up. 0 : Any port is link fail. Will be set to 1 after this port is read.	R
1.1	Jabber Detect	1 : Jabber condition in any port is detected. 0 : No Jabber condition detected for all ports	R
1.0	Extended Capability	Forced to 1.	R

Table 5-2 Status Register Bit Definition

C. Port Reset Register (register #16) (R/W)

Bit(s)	Name	Description	R/W
16.15:8	Reserved	Ignored when read.	R
16.7	ResetP7	1 : reset Port 7's Logic. 0 : not reset Port 7's Logic. Power on low.	R/W
16.6	ResetP6	1 : reset Port 6's Logic. 0 : not reset Port 6's Logic. Power on low.	R/W
16.5	ResetP5	1 : reset Port 5's Logic. 0 : not reset Port 5's Logic. Power on low.	R/W
16.4	ResetP4	1 : reset Port 4's Logic. 0 : not reset Port 4's Logic. Power on low.	R/W
16.3	ResetP3	1 : reset Port 3's Logic. 0 : not reset Port 3's Logic. Power on low.	R/W
16.2	ResetP2	1 : reset Port 2's Logic. 0 : not reset Port 2's Logic. Power on low.	R/W
16.1	ResetP1	1 : reset Port 1's Logic. 0 : not reset Port 1's Logic. Power on low.	R/W
16.0	ResetP0	1 : reset Port 0's Logic. 0 : not reset Port 0's Logic. Power on low.	R/W

Table 5-3 Port Reset Register Bit Definition

D. Port Control Register (register #17) (R/W)

Bit(s)	Name	Description	R/W
17.15	ScrenP7	1 : Enable Scrambler/Descrambler at Port 7 0 : Disable Scrambler/Descrambler at Port 7 The default value after power on is 1.	R/W
17.14	ScrenP6	1 : Enable Scrambler/Descrambler at Port 6 0 : Disable Scrambler/Descrambler at Port 6 The default value after power on is 1.	R/W
17.13	ScrenP5	1 : Enable Scrambler/Descrambler at Port 5 0 : Disable Scrambler/Descrambler at Port 5 The default value after power on is 1.	R/W
17.12	ScrenP4	1 : Enable Scrambler/Descrambler at Port 4 0 : Disable Scrambler/Descrambler at Port 4 The default value after power on is 1.	R/W
17.11	ScrenP3	1 : Enable Scrambler/Descrambler at Port 3 0 : Disable Scrambler/Descrambler at Port 3 The default value after power on is 1.	R/W
17.10	ScrenP2	1 : Enable Scrambler/Descrambler at Port 2 0 : Disable Scrambler/Descrambler at Port 2 The default value after power on is 1.	R/W
17.9	ScrenP1	1 : Enable Scrambler/Descrambler at Port 1 0 : Disable Scrambler/Descrambler at Port 1 The default value after power on is 1.	R/W
17.8	ScrenP0	1 : Enable Scrambler/Descrambler at Port 0 0 : Disable Scrambler/Descrambler at Port 0 The default value after power on is 1.	R/W

Table 5-4 Port Control Register Bit Definition

D. Port Control Register (register #17) (R/W) (Continued)

Bit(s)	Name	Description	R/W
17.7	EnP7	1 : Enable RX/TX functions at Port 7. 0 : Disable RX/TX functions at Port 7. The default value after power on is 1.	R/W
17.6	EnP6	1 : Enable RX/TX functions at Port 6. 0 : Disable RX/TX functions at Port 6. The default value after power on is 1.	R/W
17.5	EnP5	1 : Enable RX/TX functions at Port 5. 0 : Disable RX/TX functions at Port 5. The default value after power on is 1.	R/W
17.4	EnP4	1 : Enable RX/TX functions at Port 4. 0 : Disable RX/TX functions at Port 4. The default value after power on is 1.	R/W
17.3	EnP3	1 : Enable RX/TX functions at Port 3. 0 : Disable RX/TX functions at Port 3. The default value after power on is 1.	R/W
17.2	EnP2	1 : Enable RX/TX functions at Port 2. 0 : Disable RX/TX functions at Port 2. The default value after power on is 1.	R/W
17.1	EnP1	1 : Enable RX/TX functions at Port 1. 0 : Disable RX/TX functions at Port 1. The default value after power on is 1.	R/W
17.0	EnP0	1 : Enable RX/TX functions at Port 0. 0 : Disable RX/TX functions at Port 0. The default value after power on is 1.	R/W

Table 5-4 Port Control Register Bit Definition (Continued)

E. Link and Partition Status Register (register #18) (R)

Bit(s)	Name	Description	R/W
18.15	LinkP7	1 : Link Status is OK at port 7 0 : Link Status is Fail at Port 7 Status is updated at every TXCLK clock.	R
18.14	LinkP6	1 : Link Status is OK at port 6 0 : Link Status is Fail at Port 6 Status is updated at every TXCLK clock.	R
18.13	LinkP5	1 : Link Status is OK at port 5 0 : Link Status is Fail at Port 5 Status is updated at every TXCLK clock.	R
18.12	LinkP4	1 : Link Status is OK at port 4 0 : Link Status is Fail at Port 4 Status is updated at every TXCLK clock.	R
18.11	LinkP3	1 : Link Status is OK at port 3 0 : Link Status is Fail at Port 3 Status is updated at every TXCLK clock.	R
18.10	LinkP2	1 : Link Status is OK at port 2 0 : Link Status is Fail at Port 2 Status is updated at every TXCLK clock.	R
18.9	LinkP1	1 : Link Status is OK at port 1 0 : Link Status is Fail at Port 1 Status is updated at every TXCLK clock.	R
18.8	LinkP0	1 : Link Status is OK at port 0 0 : Link Status is Fail at Port 0 Status is updated at every TXCLK clock.	R

Table 5-5 Link and Partition Status Register Bit Definition

E. Link and Partition Status Register (register #18) (R) (Continued)

Bit(s)	Name	Description	R/W
18.7	PartP7	1 : Port 7 has been partitioned 0 : Port 7 has not been partitioned Status is updated every 40 ns.	R
18.6	PartP6	1 : Port 6 has been partitioned 0 : Port 6 has not been partitioned Status is updated every 40 ns.	R
18.5	PartP5	1 : Port 5 has been partitioned 0 : Port 5 has not been partitioned Status is updated every 40 ns.	R
18.4	PartP4	1 : Port 4 has been partitioned 0 : Port 4 has not been partitioned Status is updated every 40 ns.	R
18.3	PartP3	1 : Port 3 has been partitioned 0 : Port 3 has not been partitioned Status is updated every 40 ns.	R
18.2	PartP2	1 : Port 2 has been partitioned 0 : Port 2 has not been partitioned Status is updated every 40 ns.	R
18.1	PartP1	1 : Port 1 has been partitioned 0 : Port 1 has not been partitioned Status is updated every 40 ns.	R
18.0	PartP0	1 : Port 0 has been partitioned 0 : Port 0 has not been partitioned Status is updated every 40 ns.	R

Table 5-5 Link and Partition Status Register Bit Definition (Continued)