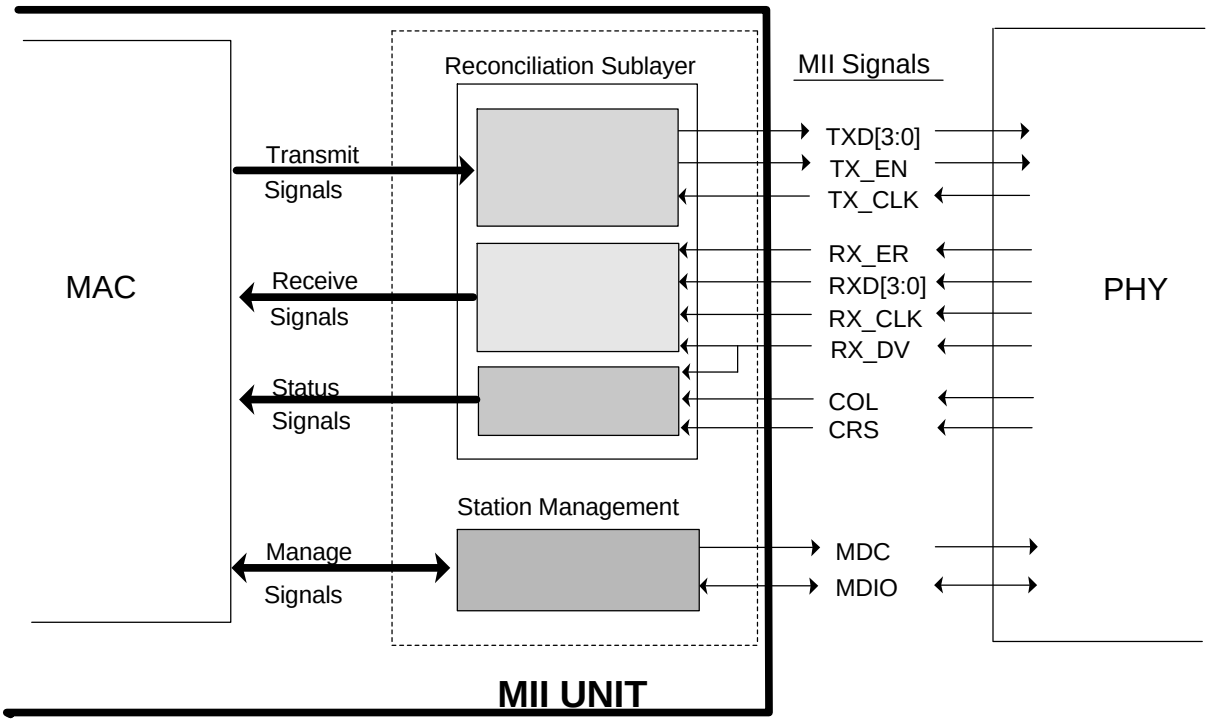
5.5. NETWORK INTERFACE OPERATION

5.5.1. SYM/MII PORT

When bit 18 (PS) of CSR6 is set, the SYM/MII port is selected. Then if bit 23(PCS) of CSR6 is set, this port will operate in SYM mode. If bit 23 of CSR6 is reset, this port will operate in MII mode. The MII is an IEEE 802.3 compliant interface that provides a simple and easily implemented interconnection between CSMA/CD Media Access Control(MAC) sublayer and Physical (PHY) layer devices, and between PHY layer devices and Station Management (STA) entities. This interface is used to provide media independence for various forms of unshielded twisted pair wiring, shielded twisted pair wiring, fiber optic cabling, and other potential media, so that identical media access controllers may be used with any of these media.
The MII unit consists of two parts: one is the Reconciliation Sublayer and the other is the Station Management Entity.



MX98713

5.5.1.1. RECONCILIATION SUBLAYER AND MII SIGNALS

The Reconciliation sublayer maps the signals provided from the MII to the PLS service defined in the IEEE802.3. The MII signal functional specification is decribed as follows:

Signal Name	Description
TXEN	Transmit enable is asserted by the MAC sublayer when the first transmit preamble nibble is driven over the MII and remains asserted for the remainder of the frame.
TXC	Transmit clock that is driven by PHY layer synchronizes all transmit signals.

TXD[3:0]	These lines provide transmit data.
RXDV	Receive data valid is asserted by the PHY layer when the first received preamble nibble is driven over MII and remains asserted for the remainder of the frame.
RXER	Receive error is asserted by the PHY layer to indicate either a coding error or any other type of error was received. This error was detected on the frame currently being received and transferred over the MII.
RXC	Receive clock synchronizes all receive signals.
RXD[3:0]	These lines provide receive data.
COL	Collision detect is asserted by the PHY layer when it detects a collision on the medium. It remains asserted while this condition persists.
CRS	Carrier sense is asserted by the PHY layer when either the transmit or receive medium is active (not idle).

5.5.1.2. STATION MANAGEMENT ENTITY

Station Management Entity (STA) is a MII management interface supported according to IEEE 802.3u. This management interface, comprised of two signals MDC and MDIO, provides access to management parameters and services.
MDC is an output signal to the PHY as the timing reference for transferring of information on the MDIO signal.

MDIO is a bidirection signal which is used to transfer control information and status between the PHY and the STA.

The management command frame structure is as follows :

<IDLE> <ST><OP><PHYAD><REGAD><TA><DATA><IDLE>
READ: <01><10><AAAAA><RRRRR> <Z0><DDDDDDDDDDDDDDDD>
WRITE: <01><01><AAAAA><RRRRR> <10><DDDDDDDDDDDDDDDD>

* The IDLE condition is a logic one. All tri-state drivers will be disabled and the PHY's pull-up resistor will pull the MDIO line to logic one.
* Prior to initiating any other transaction, the station management entity shall send a sequence of 32 logic one bits on MDIO with 32 corresponding cycles on MDC to provide a pattern that it can be used to estalish synchronization.

5.5.1.3. SYMBOL SIGNALS

Symbol mode is activated when the MII/SYM port uses either the 100BASE-TX or 100BASE-FX applications. These signals that support the exchange of code-bits and status indication between the PCS (Physical Coding Sublayer) and PMA(Physical Medium Attachment) map the PMA service interface specified in IEEE 802.3u/D4.

Signal Name	Description
TXC	Transmit clock is common to SYM amd MII modes.
TXD[4:0]	Transmit data which are coded output to external device.
RXC	Receive clock is recovered by the PHY.
RXD[4:0]	Receive data is driven by external PMD device and is synchronized to the receive clock(RXC).
SD	Signal Detect indication is supplied by external PMD devices.

The PCS function is decribed in Section 5.6.

5.5.1.4. OPERATING MODES

The PMAC implements MII/SYM port signals to support the following operating modes:

(1)100Mb/s MII mode -- The PMAC implements the MII with a data rate of 100Mbps and both the receive clock RXC and the transmit clock TXC operate at 25 MHz.

(2)10Mb/s MII mode -- The PMAC implements the MII with a data rate of 10 Mbps and both the receive clock RXC and the transmit clock TXC operate at 2.5 MHz.

(3)100BASE-TX mode -- The PMAC implements the PCS functions which include:

* 4-bit and 5-bit decoding and encoding
*Start-of-stream delimiter (SSD) and end-of-stream delimiter(ESD) detection and generation
* Bit alignment
*Carrier detection
*Symbol error detection
*Scrambling and descrambling
*Link timer

(4)100BASE-FX mode -- The PMAC implements the PCS functions for multi-mode fiber. These functions are the same as those in the 100BASE-TX mode, except for their no scrambling and descrambling function.

(5)NWay mode-- The MX98713 implements the auto-negotiation function to detect the attached media and to decide the operation mode with maximum advantage.

5.5.2. 10MBPS ENDEC INTERFACE

The interface consists of seven signals that provide a conventional interface to the existing 10-bps Ethernet ENDEC components. In the MX98713, the seven signals connect to the embeded MCC/TP port.

5.5.3. PACKAGE STRUCTURE AND 802.3U CONFORMANCE

In frequency, the PMAC could be operated in network with speed running under 2.5MHz and 25MHz. Which means the MX98713 100Mbps PMAC is scaleable not only in speed but also for the driver. Same buffer management structure and internal FIFO structure are used in PMAC to run both 10M bps & 100M bps network for software compatibility purpose. Furthermore, 100Mbps MAC supports full duplex mode where transmit and receive processes are running independently.

The use of FIFO logic serves as asynchronous packet buffer between PCIBIU and network where each one has its own data throughput rate. A nibblewise CRC circuit is also needed to process 4 bits network data in one network clock period. As in full duplex mode, two CRC circuit is used by transmit process and receive process respectively.

5.5.3.1 ETHERNET AND IEEE 802.3 FRAMES

An Ethernet frame format consists of the following:

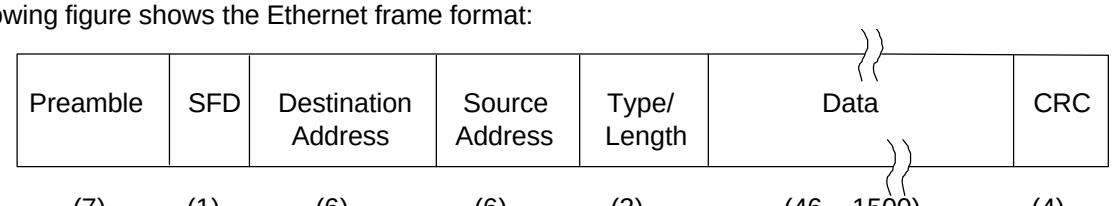
Field	Description
Preamble	A 7-byte field of 56 alternating 1s and 0s, beginning with a 0.
SFD	A 1-byte field that contains the value 10101011; the MSB is transmitted and received first.
Destination	A 6-byte field that contains the specific station address, the broadcast address, or a multicast address where this frame is directed.
Source	A 6-byte field that contains the specific station address where this frame originated.
Type/Length	A 2-byte field that indicates whether the frame is in IEEE 802.3 format or Ethernet format. A field greater than 1500 is interpreted as a type field, which defines the type of procotol of the

frame.A field smaller than or equal to 1500 is interpreted as a length field, which indicates the number of data bytes in the frame.

Data — A data field consists of 46 to 1500 bytes that is fully transparent. A data field shorter than 46 bytes is allowed,. Unless padding is disabled (TDES1<23>), it is added by PMAC when transmitting to fill the data field upto 46 bytes.

CRC — A frame check sequence (FCS) is a 32-bit cyclic redundancy check (CRC) value that is computed as a function of the destination address field, source address field, type field and data field. The FCS is appended to each transmitted frame, and used at reception to determine if the receive frame is valid.

The following figure shows the Ethernet frame format:



Ethernet Frame Format

*Numbers in parentheses indicate field length in bytes.

The CRC polynomial, as specified in the Ethernet specification, is as follows:

FCS(X) = X31 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5+ X4 + X2 + X1 + 1

The 32 bits of the CRC value are placed in the FCS field so that the X31 term is the right-most bit of the first octet, and the X0 term is the left-most bit of the last octet. The bits of the CRC are thus transmitted in the order of X31,X30,....X1,X0.

5.5.4. MAC TRANSMIT OPERATION

5.5.4.1. OVERVIEW

The PMAC supports a complete implementation of the MAC sublayer of IEEE 802.3 including half-duplex, full-duplex and loopback operation. The MAC block is divided into two parts: the transmit MAC and the receive MAC.

The transmit MAC reads data from transmit FIFO through an 8- bit data bus and transfers data through MII interface to MII/SYM port or 10BASE-T interface.

5.5.4.2. TRANSMIT INITIATION

When host CPU prepares a content of frame to be transmited in memory and a companion transmit descriptor, it signals the PMAC to take it by sending start transmission command (Section 5.2.6). After the PMAC has been noticed of this transmit list, the PMAC starts to move the data through the PCI bus from host memory to the internal transmit FIFO (TXFIFO).

When the TXFIFO is filled to the programmed threshold level, or when there is a full frame buffered into the TXFIFO, the transmit MAC begins to encapsulate the frame after a minimum IPG time at least. The transmit encapsulation is performed by transmit state machine which delays the actual transmission of the data onto the network and appends the 56 preamble bits together with the SFD to the basic frame beginning and the CRC to the basic frame end.

If the data field is less than 46 bytes, and padding (TEDS1<23>) is enabled, the MAC pads the basic frame with the pattern 00 for up to 46 bytes before appending the CRC field to the end. If the PMAC operates in

100BASE-FX mode or 100BASE-TX mode, it encapsulates the frames to be transmited according to IEEE 802.3, clause 24.
Actual transmission of the data onto the network occurs only if the network has been idle for a 96-bit time duration or named a interpacket gap (IPG), and any backoff time requirements have been satisfied. The IPG time is divided into two parts: IPS1 and IPS2.

1. IPS1 time (56- to 60-bit time): the PMAC monitors the network for an idle state. If a carrier is sensed on the serial line during the time, the MX98713 defers and waits until the line is idle again before restarting the IPS1 time count.
2. IPS2 time (36- to 40-bit time): the PMAC continues to count time even though a carrier has been sensed on the network, and thus forces collisions on the network. This enables all network stations to have access to the serial line.

5.3.4.3. COLLISION AND TERMINATING TRANSMISSION

The PMAC detects a collision event by one of the following ways:

1. In MII mode, when COL asserts.
2. In SYM or 10BASE-Tmode, when the receive input is active while the PMAC transmits.

When the PMAC senses a collision while transmitting, it halts the transmission of the data. Then it transmits a jam pattern consisting of hexadecimal AAAAAAAA. At the end of the jam transmission, it begins the backoff wait period. The PMAC scheduling of retransmission is determined by a controlled randomization process called truncated binary exponential backoff. When 16 times of attempts have been made at transmission and all have been terminated by a collision, the PMAC sets an error status bit in the descriptor (TEDS0<8>) and if it is enabled, it issues a normal transmit termination (CSR5<0>) interrupt to the host.
The specific frame transmission is terminated by any of the following conditions:

1. Normal -- The frame has been transmitted successfully.
2. Underflow -- Transmit data is not ready when needed for transmission. The underflow bits (TDES0<1> and CSR5<5>) are set, and the packet is terminated with a bad CRC.
3. Excessive collisions -- If a collision occurs for the 15th consecutive retransmission attempt of the same frame, TDES0<8> is set.
4. Jabber Timer expired -- If the jabber timer expires, TEDS0<8> is set, The "programmed interval" transmission is cut off.
5. Memory error -- This error means either a host bus timeout or a host memory error.
6. Late collision -- If a collision occurs after the collision window (transmitting at least 64 bytes), transmission is cut off and TEDS0<9> is set.

5.5.5. MAC RECEIVE OPERATION

5.5.5.1. RECEIVE INITIATION

The PMAC continuously monitors the network for a new frame reception. When a new frame is recognized, it starts to process the incoming data. It detects activity by one of the following ways:

1. In 10 BASE-T mode, when the receiving input is active.
2. In MII mode, when both RXDV and CRS assert.
3. In SYM mode, when the receive input is active. After detecting activity on the network line, the receive MAC starts to process the preamble bytes.

The PMAC allows any arbitrary preamble length. However, depending on the mode, there is a minimum preamble length.

* In MII/SYM mode, at least 8-bits are required to recognize a preamble.
* In 10 BASE-T mode, at least 16-bits are required to recognize a preamble.

Recognition of preamble occurs as follows:

* In MII/SYM mode, the receive MAC checks for the SFD byte content of 10101011.
* In SRL mode, the first 8 preamble bits are ignored. The receive MAC checks for the SFD byte content of 10101011.

5.5.5.2 ADDRESS MATCHING

The first bit of the destination address signifies whether it is a physical address(0) or a multicast address. The receive MAC filters the frame based on the Ethernet receive address group filtering mode that has been enabled.

Ethernet Receive Address Groups

Group	Description
1	16-address perfect filtering
2	One physical address, unlimited multicast addresses imperfect filtering
3	Unlimited physical addresses, unlimited multicast addresses imperfect filtering
4	Promiscuous Ethernet reception
5	16-address perfect filtering and reception of all multicast Ethernet addresses
6	16-address inverse filtering

If the frame address passes the filter, the receive MAC removes the preamable and delivers the frame to the host processor memory. If, however, the address does not pass the filter when mismatch is recognized, the receive MAC terminates this reception.

5.5.5.3 RECEIVE TERMINATION AND ERROR STATUS

Reception of a specific frame is terminated when any of the following conditions occurs:

1. Normal termination -- The frame has been received successfully and the network activity stops.
2. Overflow -- The receive DMA cannot empty the receive FIFO into host memory as rapidly as it is filled, and an error occurs as frame data is lost. The overflow bit (REDS0<0>) is set.
3. Watchdog timer expired -- If the timer expires(CSR5<9> and REDS0<4> both set) while reception is still in process, and reception is cut off.
4. Collision -- If a late collision occurs after the reception of 64 bytes of the package, the collision seen bit (REDS0<6>) is set.

When reception terminates, the receive MAC determines the status of the received frame and loads it into the recieve buffer descriptor. Some other errors that may be reported are described as follows:

1. CRC error -- The 32-bit CRC did not match the CRC calculated upon reception. In addition, the PMAC reports a CRC error in any of the following cases:
   The RXER signal asserts during frame reception in the MII mode.
   In the SYM mode and one of the following occurs:
   (1) An invalid symbol is received in the middle of the frame.
   (2) The frame does not end with the symbol T followed by symbol R.
   (3) Between the JK and TR symbol pairs, the frame contains any symbol which does not belong to the data code groups defined in IEEE 802.3 clause 24.
2. Dribble bits error -- This indicates the frame did not end by a byte boundary. The receive MAC signals a dribble bits error only if the number of dribbling bits in the last byte is 4 in MII/SYM operating mode, or at least 3 in 10Mbps serial operating mode. Only the whole bytes are run through the CRC check.
3. Alignment error -- A CRC error and a dribble bit error occur together. This means that the frame did not contain an integral number of bytes and the CRC check failed.
4. Runt frame -- A frame containing less than 64 bytes was received (including CRC). The MX98713 defaults to inhibit reception of runt frame.
5. Long frame -- A frame containing more than 1518 bytes was received (including CRC).

5.5.6. ADDRESS FILTERING MODES

A setup frame defines Ethernet addresses that are used to filter all incoming frames to PMAC. Setup frame is not transmitted on to the cable but is internally processed by PMAC to either fill address CAM or address hash table. The size of setup frame must be 192 bytes exactly and located in a single host buffer that is doubleword aligned, and only word on even address is used while word on odd address is ignored. The TDES1<29> and TDES1<30> field must both be zero.

Setup frame for perfect filtering mode CSR6<0> = 0:

31 16 15 0

XXX	Physical Address 00 Byte<1:0>
XXX	Physical Address 00 Byte<3:2>
XXX	Physical Address 00 Byte<5:4>
XXX	Physical Address 01 Byte<1:0>
XXX	Physical Address 01 Byte<3:2>
:	:
:	:
XXX	Physical Address 14 Byte<3:2>
XXX	Physical Address 14 Byte<5:4>
XXX	Physical Address 15 Byte<1:0>
XXX	Physical Address 15 Byte<3:2>
XXX	Physical Address 15 Byte<5:4>

Imperfect Filtering Setup Frame Format CSR6<0>=1.

31 16 15 0

XXX	Hash Filter Byte<1:0>
XXX	Hash Filter Byte<3:2>
XXX	Hash Filter Byte<5:4>
:	:
XXX	Hash Filter Byte<63:62>
:	XXX
:	XXX
XXX	Physical Address Byte<1:0>
XXX	Physical Address Byte<3:2>
Location< 167:164 > XXX	Physical Address Byte<5:4>
:	XXX
<Location 191:188> XXX	XXX

For any incoming frame with a multicast destination address, PMAC applies the CRC function to the first 6 bytes containing the destination address, then it uses the most significant 9 bits of the result as a bit index into the hash table. There are 512 bits in hash table. If the incoming address is a physical address then it is compared against the phsical address set up in the PMAC.

Since hash table is adopted to screen incoming multicast frames, it is obvious that some frames not addressed to this station may slip through, but hash table still decreases the number of frames that the host can receive. Fig 24 shows the configuration of the filtering function.

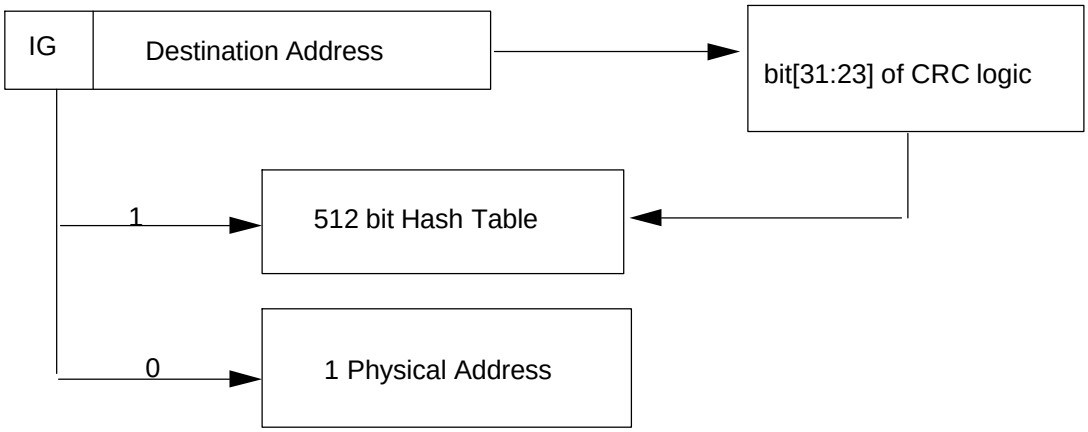


Fig.24 -- Imperfect Address Filtering

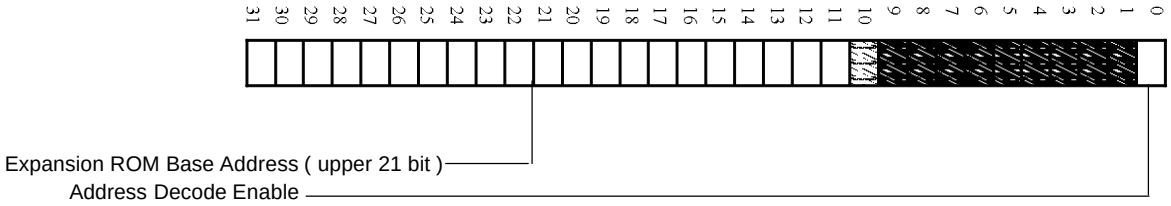
5.6 NWAY INTERFACE

The Nway interface, combined with physical layer parts (FCG and PMD) from many silicon vendors, implements the complete functions of ANSI/IEEE802.3u 100Base-X and ANSI/IEEE802.3 10Base-T. The NWay interfaces with MAC through Media Independent Interface, implementing the 100 Base-TX protocal, Auto-Negotiation, Ethernet Manchester encoder/decoder and 10Base-T transceiver. Detailed implementation schematic please refer to MX98713 Application Note.

5.7 BOOT ROM LOGIC

Boot ROM base address is defined in PCI's configuration memory at offset 33h - 30h. At system reset, system BIOS will try to assign a base address to PBER register such that a read at boot ROM offset 0 is "55"h and offset 1 is "AA"h. If such base address can not be found by system BIOS, no boot ROM base address is assigned and no expansion ROM initialization is granted, therefore no boot ROM of this particular PCI agent is executed or recognized.

PBER Register (33h- 30h)



bit 0 : Address Decode Enable, decoding will be enabled if only both enable bit in PFCS<1> and this expansion ROM register bit are 1.
bit 10 - bit 1 : not used
bit 31 - bit 11 : Defines the upper 21 bits of expansion ROM base address.

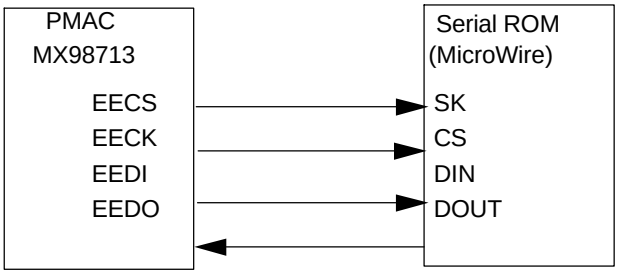
The PMAC support 4 different sizes of boot ROM as defined in table 5.7, default one is 16K bytes.

Table 5.7 Boot ROM size decode

BPSEL2	BPSEL1	ROM SIZE
0	0	8K
0	1	16K
1	0	32K
1	1	64K

5.8 SERIAL ROM INTERFACE

Serial ROM Connection



There are four serial ROM interface pins:
EEDO - Serial ROM (EEPROM) Data Out >> bit 3,CSR9

EEDI - Serial ROM (EEPROM) Data In >> bit 2,CSREG9
EECK - Serial ROM (EEPROM) Serial Clock >> bit 1,CSREG9
EECS - Serial ROM (EEPROM) Chip Select >> bit 0,CSREG9

Software Programming Interface

A Read operation consists of three phases :

1. Command phase - 3-bit (binary code of "110")
2. Address phase - 6-bit for 256-bit to 1Kbit ROM, 8 bit- for 2Kbit to 4Kbit ROM
3. Data phase - 16-bit

These phases are generated through a sequence of write commands to CSR9.. A typical read cycle is mentioned below:

Write CSR9 00004800H (>= 30ns)

Write CSR9 00004801H (>= 50ns)
Write CSR9 00004803H (>= 250ns)
Write CSR9 00004801H (>= 100ns)

Command --

Write CSR9 00004805H (>= 150ns)
Write CSR9 00004807H (>= 250ns)
Write CSR9 00004805H (>= 250ns)
Write CSR9 00004807H (>= 250ns)
Write CSR9 00004805H (>= 100ns)
Write CSR9 00004801H (>= 150 ns)
Write CSR9 00004803H (>= 250 ns)
Write CSR9 00004801H (>= 100ns)

Address --

Write CSR9 0000480XH (>= 150 ns)
Write CSR9 0000480XH (>= 250 ns)
Write CSR9 0000480XH (>= 100ns)

Data --

Write CSR9 00004803H (>= 100ns)
Read CSR9<3> = DX (>= 150ns)
Write CSR9 00004801H (>= 250ns)

Write CSR9 00004800H (>= 100ns)
END

A Write operation consist of three phases :

1. Command phase - 3-bit (binary code of "110")
2. Address phase - 6-bit for 256-bit to 1Kbit ROM, 8-bit for 2Kbit to 4Kbit ROM
3. Data phase - 16-bit

These phases are generated through a sequence of writes to CSR9. In certain action, driver must wait until minimum timing requirement for the serial ROM operation is met in order to advance to next action. A typical driver sequence can look like this

1. Write CSR9 00004800H (>= 30ns)
2. Write CSR9 00004801H (>= 50ns)
3. Write CSR9 00004803H (>= 250ns)

4. Write CSR9 00004801H (>= 100ns)

Command --
Write CSR9 00004805H (>= 150ns)

Write CSR9 00004807H (>= 250ns)
Write CSR9 00004805H (>= 100ns)
Write CSR9 00004801H (>= 150ns)
Write CSR9 00004803H (>= 250 ns)
Write CSR9 00004801H (>= 100 ns)
Write CSR9 00004805H (>= 150 ns)
Write CSR9 00004807H (>= 250 ns)
Write CSR9 00004805H (>= 100ns)

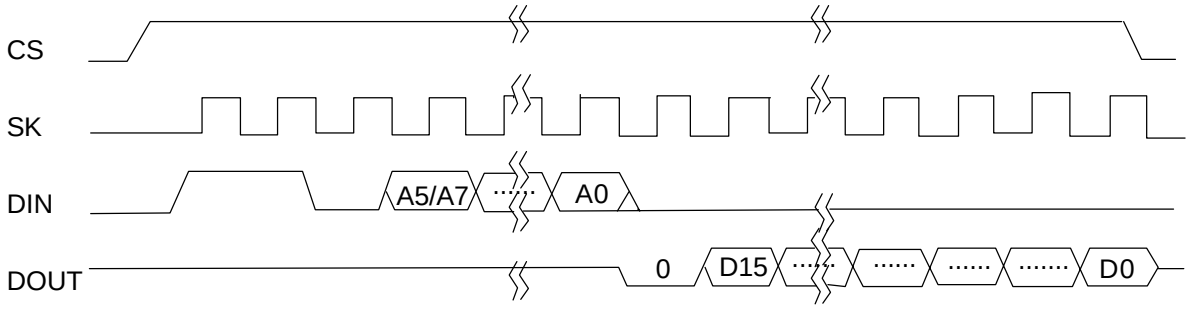
Address --
Write CSR9 0000480XH (>= 150 ns)
Write CSR9 0000480XH (>= 250 ns)
Write CSR9 0000480XH (>= 100ns)

Data --
Write CSR9 00004803H (>= 150ns)
Write CSR9 0000480XH (>= 250ns)
Write CSR9 0000480XH (>= 100ns)

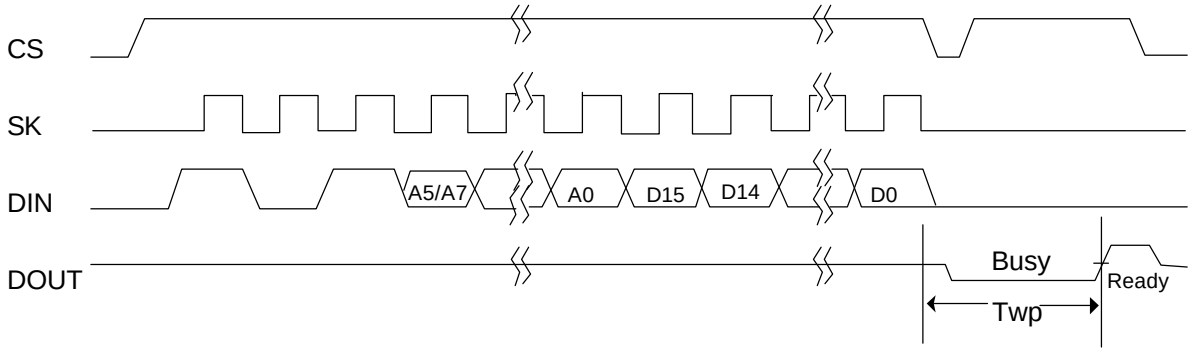
Write CSR9 00004800H (>= 250ns)
Write CSR9 00004801H (>= 250ns)
Read CSR9<3>
if CSr9<3> = 1 then go on
Write CSR9 00004800H (>= 250ns)
else
Wait 1 ms then go to *Read CSR9<3>
END

Typical serial ROM access timing is as follows:

READ Operation Timing



WRITE Operation Timing



Autoload Function

The Autoload Function is executed only when Hardware Reset (PRSTB) ends. At that time the Serial ROM interface is drived by internal circuit to load the data of serial ROM address 3Dh and 3Eh to configuration ID register.

When PRSTB is asserted, the Autoload State Machine (ASM) is reset to idle state. While PRSTB is deasserted, the ASM starts to send read command to the EEPROM and transfer Vender ID and Device ID from EEPROM to CFID register. After the ASM ends these read actions, the ASM is not enabled until next hardware reset comes.

Diagrams

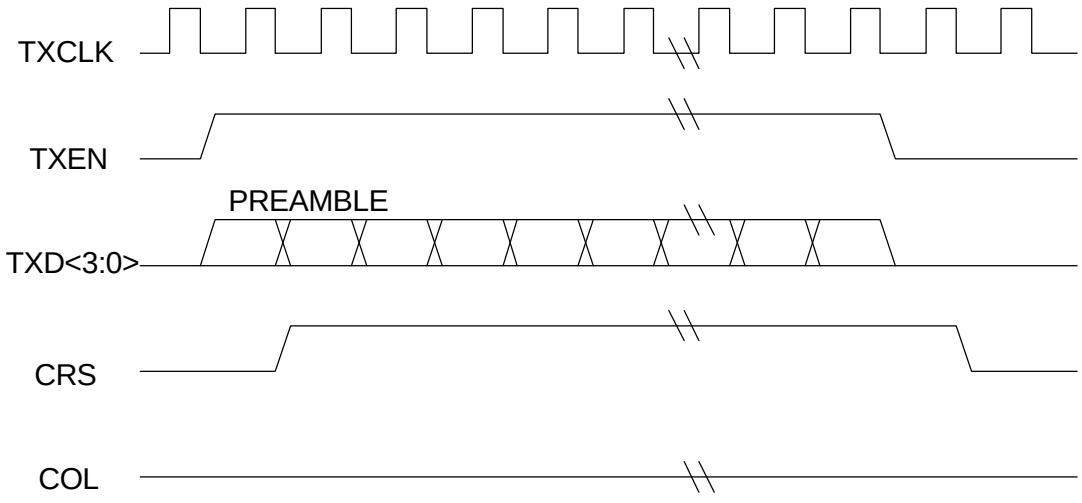


Fig.25 - - Transmission with no collision

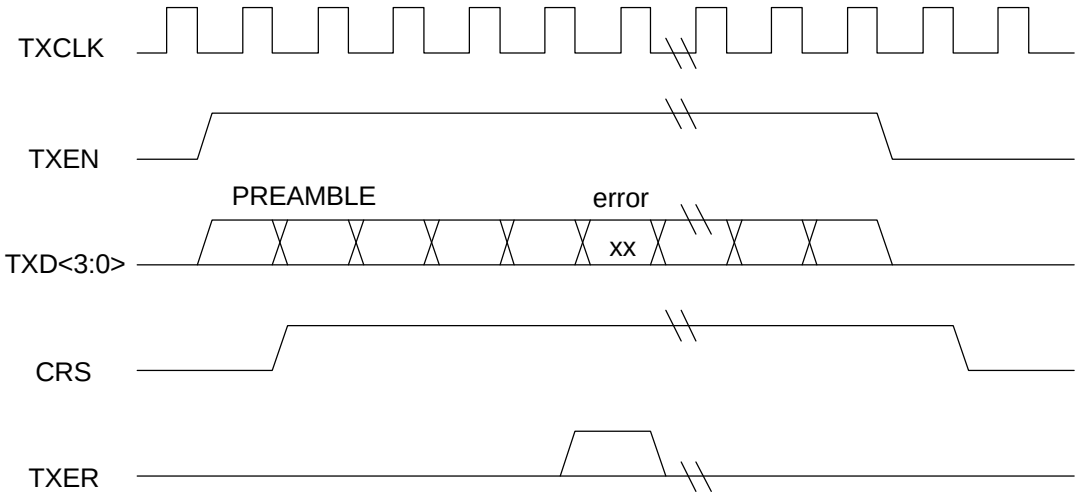


Fig.26 - - Transmission with an error

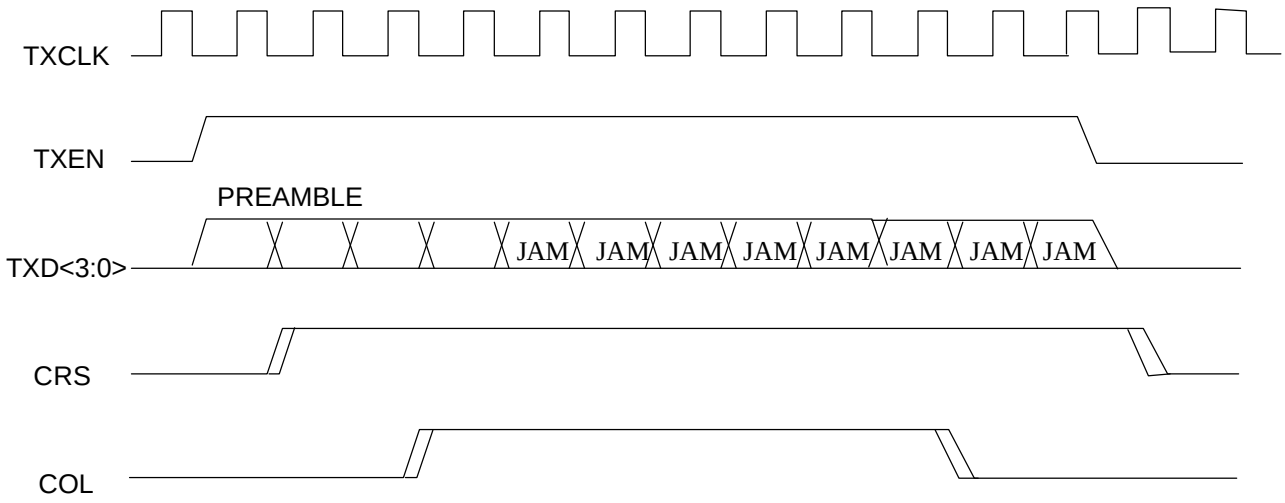


Fig. 27 - - Transmission with collision

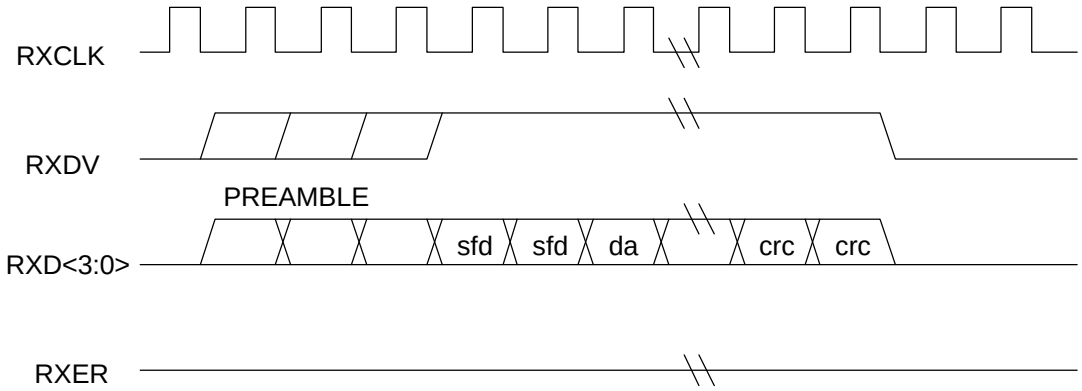


Fig.28 - - Reception with no error

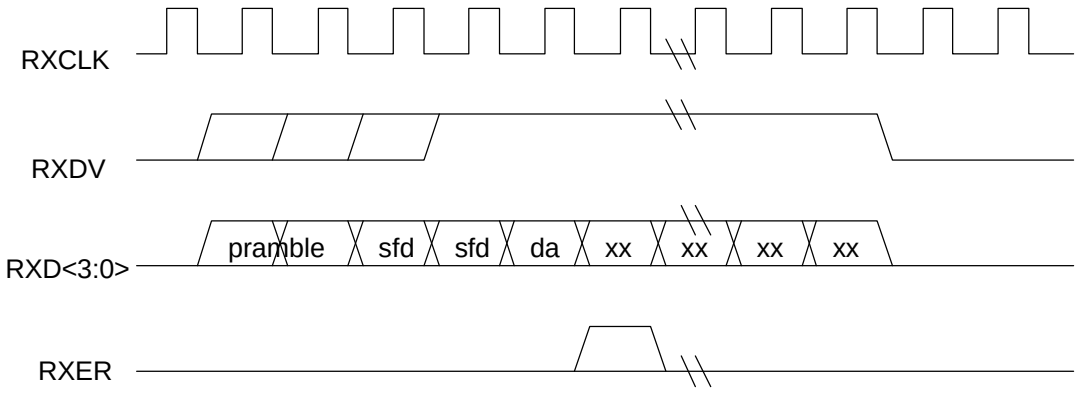


Fig.29 - - Reception with errors

7. ABSOLUTE MAXIMUM RATINGS:

Supply Voltage (VCC)	4.75V to + 5.25V
DC Input Voltage (Vin)	-0.5V to VCC + 0.5V
DC Output Voltage (Vout)	-0.5V to VCC + 0.5V
Storage Temperature Range (Tstg)	-55°C to +150°C
Power Dissipation (PD)	800mW
Lead Temp. (TL) (Soldering, 10 sec)	260°C
ESD Rating (Rzap = 1.5k, Czap = 100pF)	2000V
Clamp Diode Current	$\pm$20mA

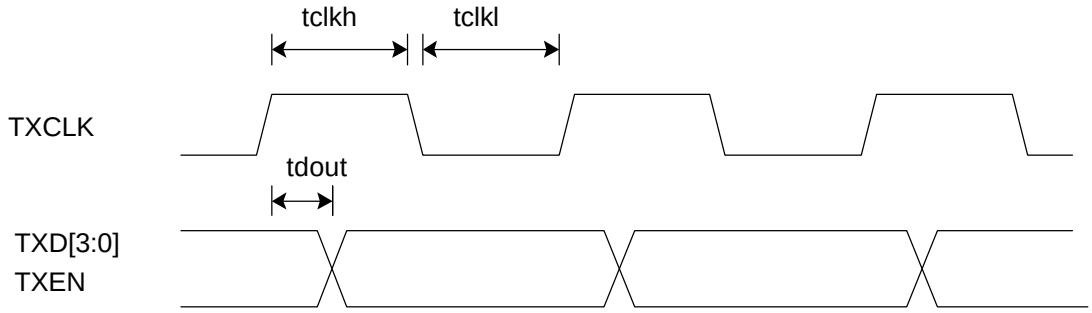
8. DC CHARACTERISTICS:

TA=0°C to 70°C, VCC=5V±10%
Storage Temperature Range=-55°C to 150°C

Symbol	Parameter	Conditions	Min	Max	Units
TTL Input/Output					
Voh	Minimum High Level Output Voltage	Ioh = -3mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol = +6mA		0.4	V
Vih	Minimum High Level Input Voltage		2.0		V
Vil	Maximum Low Level Input Voltage			0.8	V
Iin	Input Current	Vi = VCC or GND	- 1.0	+ 1.0	uA
Ioz	Minimum TRI-STATE Output Leakage Current	Vout = VCC or GND	-10	+10	uA
LED Output Driver					
Vlol	LED turn-on Output Voltage	Iol = 16mA		0.4	V
Supply Current					
Icc	Average Supply Current	X1 = 20MHz TXC =25MHz or 2.5MHz PCICLK = 33MHz			mA
TPI Symbol					
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
VOD	Differential Output Voltage (TX±)	78 ohm termination and 270 ohm from each to GND	± 600		± 1200	mV
Z_{OT}	Transmit Output Impedance			5		ohm
V_{PD}	Peak Differential Output Voltage	Load=100 ohm at TXOP/TXON	3.3	3.5	3.7	V
T_{JO}	Transmit Timing Jitter Addition	Line length is zero		± 4		ns
T_{JL}	Transmit Timing Jitter added by the MAU and PLS sections	After line model specified IEEE 802.3 for 10Base-T		± 5		ns
V_{NTS}	Differential Squelch Threshold (Normal Threshold)			260		mV
V_{RTS}	Differential Squelch Threshold (Reduced Threshold)			160		mV

9. AC CHARACTERISTICS:

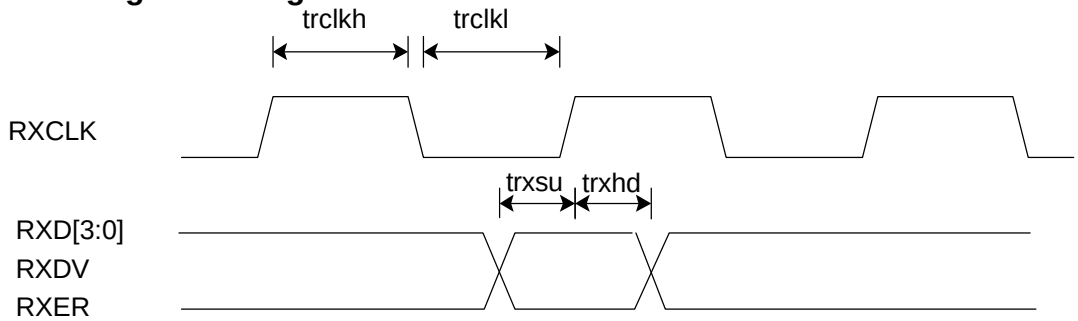
Transmit Signal Timing:



Symbol	Parameter	Min	Max	Units
tclkh	TXCLK high for 25MHz (100 Base-TX)	14	26	ns
	TXCLK high for 2.5MHz (10 Base-T)	140	260	ns
tclkl	TXCLK low for 25MHz (100 Base-TX)	14	26	ns
	TXCLK low for 2.5MHz (10 Base-T)	140	260	ns
tdout	TXD,TXEN to TXCLK rising edge	0	25	ns

* The duty cycle of the TXCLK signal shall be between 35% and 65% inclusively.

Receive Signal Timing

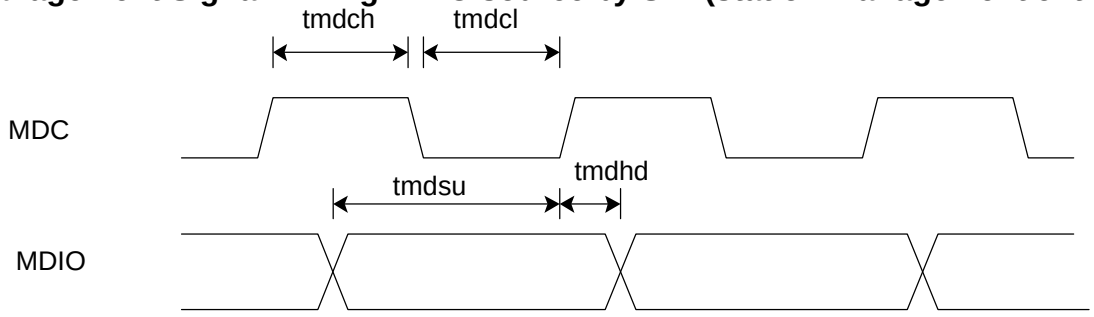


Symbol	Parameter	Min	Max	Units
trclkh**	RXCLK high for 25MHz (100 Base-TX)	14	26	ns
	RXCLK high for 2.5MHz (10 Base-T)	140	260	ns
trclkl**	RXCLK low for 25MHz (100 Base-TX)	14	26	ns
	RXCLK low for 2.5MHz (10 Base-T)	140	260	ns
trxsu	RXD,RXDV & RXER setup time to RXCLK rising edge	10		ns
trxhd	RXD,RXDV & RXER hold time to RXCLK rising edge	10		ns

* The maximum time of 10Base-T is not guaranteed at beginning and end of frame.

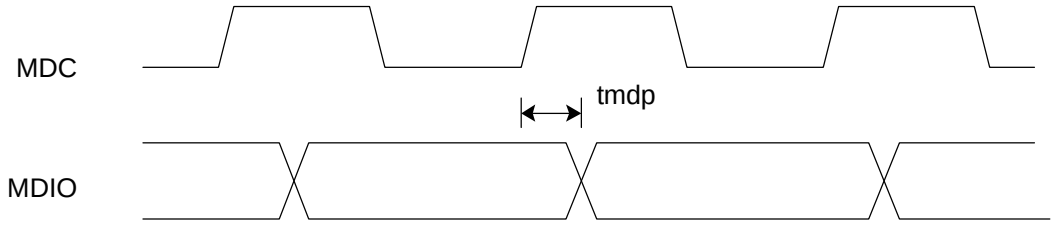
* The minimum high and low times of RXCLK shall be 35% of the nominal period.

Management Signal Timing MDIO source by STA(station management entity):



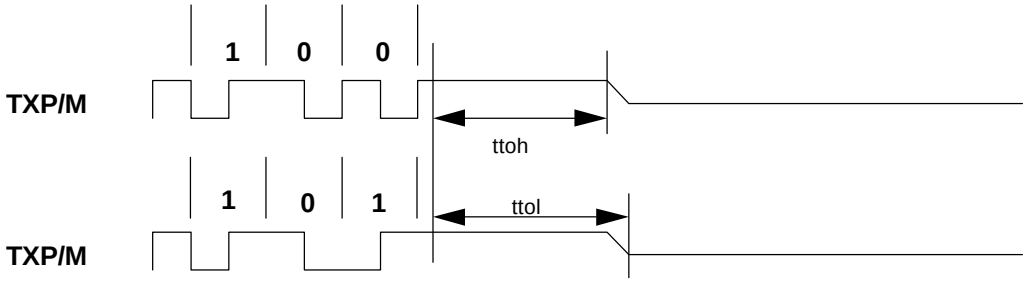
Symbol	Parameter	Min	Max	Units
tmdch	MDC high time	200		ns
tmdcl	MDC low time	200		ns
tmdsu	MDIO to MDC high setup time sourced by STA	10		ns
tmdhd	MDIO to MDC high hold time sourced by STA	10		ns

Management Signal Timing MDIO source by PHY:



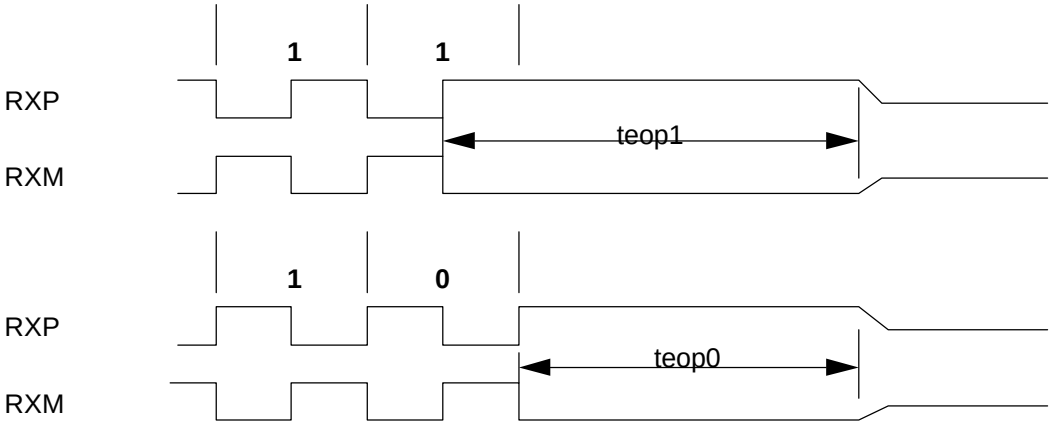
Symbol	Parameter	Min	Max	Units
tmdp	MDC high to MDIO data valid	0	300	ns

10Base-T Transmit Timing (End of Packet)



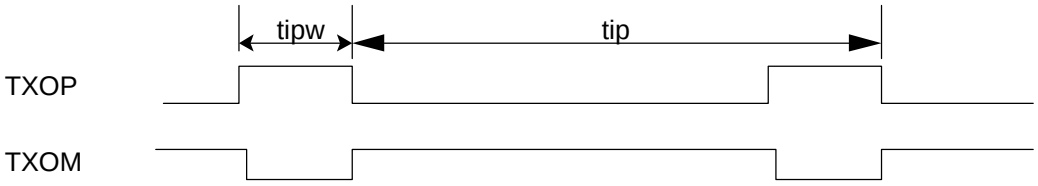
Symbol	Parameter	Min	Max	Units
ttoh	Transmit Output High before Idle (Half Step)	200		ns
ttol	Transmit Output Idle Time (Half Step)		800	ns

10Base-T Receive End of Packet Timing



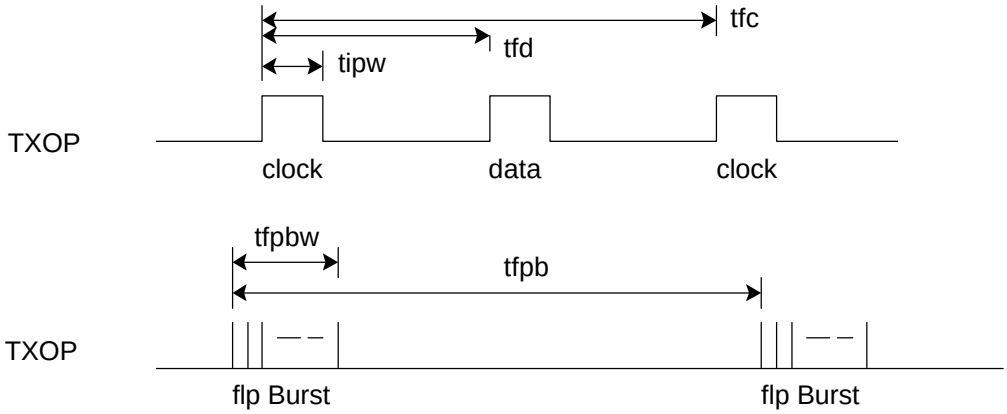
Symbol	Parameter	Min	Max	Units
teop1	Receive End of Packet Hold Time after "1"	225		ns
teop0	Receive End of Packet Hold time after "0"	225		ns

10Base-T Link Pulse Timing



Symbol	Parameter	Min	Max	Units
tip	Time between Link Output Pulses	8	24	ms
tipw	Link Integrity Output Pulse Width	80	130	ns

FLP (Fast Link Pulse) Timing:



Symbol	Parameter	Min	Max	Units
tfd	Flp Clock Pulse to Data Pulse (Data = 1)	58	65	us
tfc	Flp Clock Pulse to Clock Pulse	118	130	us
tipw	Fast Link Output Pulse Width	80	130	ns
tfpb	FLP burst to FLP Burst	12	18	ms
tfpbw	FLP Burst Width	1.8	2.1	ms

Note: FLP related timing parameters are guaranteed by design and not measured data on tester.

10. 10. PACKAGE INFORMATION
160-PIN PLASTIC QUAD FLAT PACK

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