5.3. PCI BUS INTERFACE

The Peripheral Component Interconnect (PCI) is used as an interconnecting mechanism between highly integrated peripheral controller components and processor/memory systems. The MX98713 will be treated as either a 32-bit PCI bus master to transmit and receive packets, or a 8/16 /32-bit PCI slave to access configuration, internal NIC registers and boot PROM data. PCI bus clock is targeted at 33MHz. The PMAC fully complies with PCI Spec. Revision 2.1. A total of 6 PCI commands are supported. The PMAC's internal buffer management is independent of the PCI bus speed. Therefore, it can be operated at both 2.5MHz and 25MHz network frequencies with the PCI interface seamlessly. All inputs and outputs are sychronously sampled and generated on the rising edge of the clock.

The 6 PCI standard command codes and cycle types are depicted as follows:

0010 : IO read,
- 32-bit host read from 32-bit NIC registers
- 16-bit host read from 32-bit NIC registers
- 8-bit host read from 32-bit NIC registers

0011 : IO write,
- 32-bit host write to 32-bit NIC registers
- 16-bit host write to 32-bit NIC registers
- 8-bit host write to 32-bit NIC registers

0110 : memory read,
- 32-bit PMAC read from 32-bit host descriptor/ring buffer
- 32-bit host read from 32-bit NIC registers
- 16-bit host read from 32-bit NIC registers
- 8-bit host read from 32-bit NIC registers
- 8/16/32-bit host reads from 8-bit boot PROM

0111 : memory write,
- 32-bit PMAC wrtite to 32-bit host descriptor/ring buffer
- 32-bit host write to 32-bit NIC registers
- 16-bit host write to 32-bit NIC registers
- 8-bit host write to 32-bit NIC registers

1010 : configuration read, IDSEL acts as a chip select and the content of AD[7:0] are used to select the target configuration registers. Sampled when FRAME# is asserted.

1011 : configuration write, see configuration read for details.

5.4 HOST COMMUNICATION AND BUFFER MANAGEMENT

5.4.1. HOST COMMUNICATION OVERVIEW

The buffer management scheme of the PMAC is based on descriptor lists and data buffers residing in the host memory. Transmitted or received packets are placed in data buffers. The PMAC keeps track of packets in these buffers using the information in descriptor lists. The PMAC and the driver communicate as well as transfer data through descriptor lists and data buffers. It is collectively called the host communication.

5.4.2. DESCRIPTOR AND BUFFER RESOURCE OVERVIEW

The PMAC transfers frame data from and to the transmit and receive buffers in the host memory. Descriptor containing control, status information, buffer byte count and buffer address, act as the pointer of the buffer. There are two descriptor lists, one for receive and another for transmit. CSR3 and CSR4 are programmed as the base address of each list respecively. The descriptor list is defined as forward-linked (either implicity or explicitly). Explicit chaining of descriptors is accomplished by setting the second chained RDES1<24> and TDES1<24> in both the receive and transmit descriptors. As for implicit chaining descriptor, it is accomplished by skipping a number of long words CRS0<6:2> from the end of the previous descriptor. The last descriptor may be pointed back to the first entry to create a ring structure.

5.4.3. RECEIVE BUFFER MANAGEMENT

There is a large on-chip FIFO for RX channel to support fast back to back packet receiving. Both the data ports are organized internally as 32-bit wide data bus into or out of the RX FIFO. Host driver shall allocate double-word aligned descriptors which contain host receive buffers information. All receive buffers are doubleword aligned. The on-chip PCI bus master interface will serve RX DMA machine to move data out of RX FIFO in burst transfer and is capable of zero wait state. It should be noted that RX FIFO can also continuously buffer many packets without any PCI bus DMA service before RX FIFO overflow. The following subsections will describe the control descriptors format.

5.4.3.1. RECEIVE DESCRIPTOR STRUCTURE

Fig. 14 shows the receive descriptor format. Providing status, two buffer byte-counters and two address pointers in each descriptor, the MX98713 enables the adapter to be applied to various types of memory management schemes.

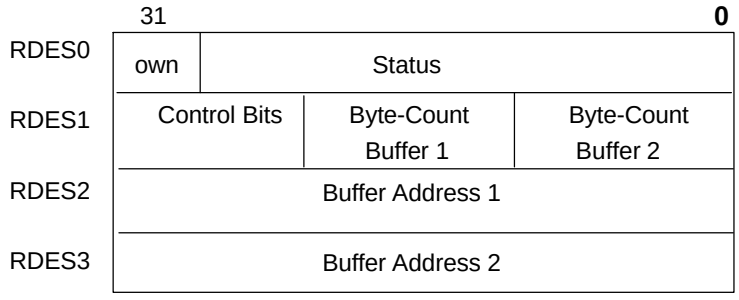

Fig. 14 -- Receive Descriptor Format

5.4.3.2. RECEIVE DESCRIPTOR 0 FORMAT

RDES0 includes the descriptor ownership, received frame status and frame length. Fig. 15 shows the RDES0 bit map and the bit fields is described in Table 9.

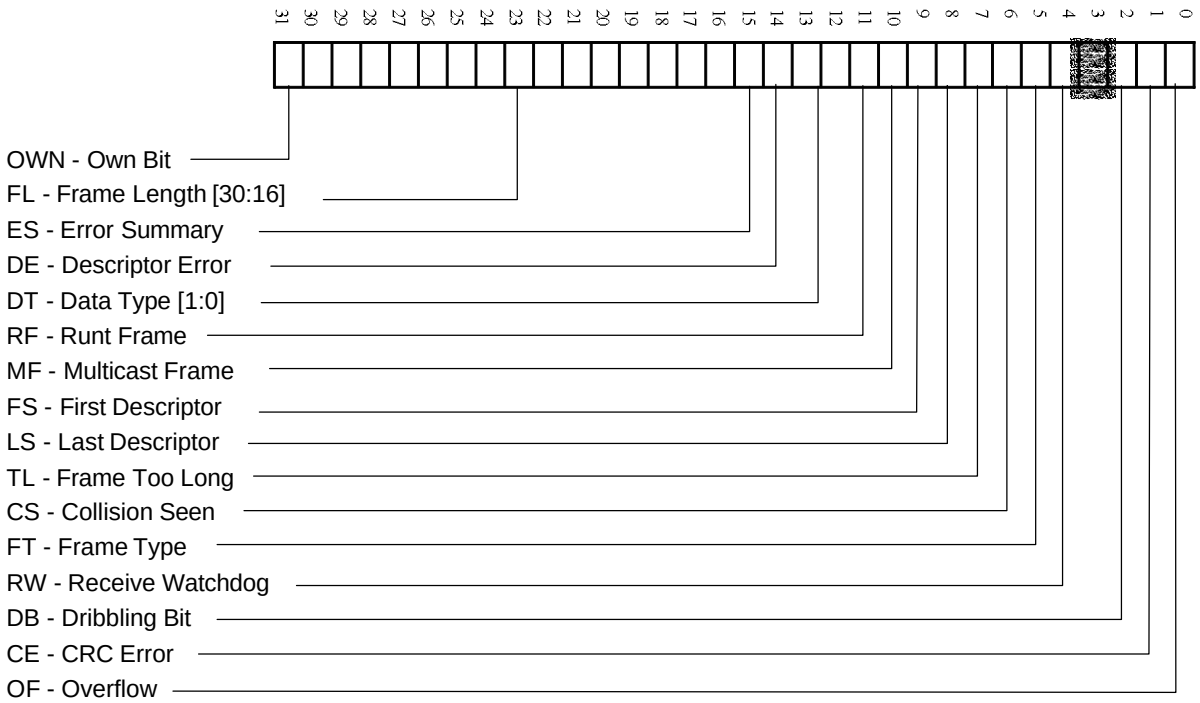

Fig. 15 -- RDES0 Receive Desciptor 0

Table 9 -- Receive descriptor 0

Field	Name	Description
31	OWN	Own Bit When set it indicates that the PMAC has the ownership of the descriptor. When reset it indicates that the descriptor is owned by the host. The PMAC clears the bit either when it completes the frame reception or when the buffers associated with this descriptor are full.
30:16	FL	Frame Length It indicates the length, in bytes, of the received frame including the CRC. It is valid only when the last descriptor RDES0<8> is set and the descriptor error RDES<14> is reset.
15	ES	Error Summary Indicates one of the following receive errors happened: Overflow - RDES<0> CRC error - RDES<1> Collision seen - RDES<6> Frame too long - RDES0<7> Runt frame - RDES0<11> descriptor error - RDES<14> Valid only when the last descriptor RDES0<8> is set.
14	DE	Descriptor Error When set it indicates a frame truncation caused when both frames do not fit within the current descriptor buffers, and the PMAC does not own the next descriptor. The frame is truncated. This bit is valid only when the last desriptor RDES0<8> is set.
13:12	DT	Data Type Indicates the type of frame the buffer contains: 00 - Serial received frame 01 - Internal loopback frame 10 - External loopback frame or serial received frame. 11 - Reserved. Valid only when the last desriptor RDES0<8> is set.
11	RF	Runt Frame When set it indicates that this frame was damaged by a collisiion or premature termination before the collision window had passed. Runt frames are passed to the host only if the passed bad frames CSR6<3> is set.
10	MF	Multicast Frame When set it indicates that the frame address is multicast. It is valid only when the last descriptor RDES0<8> is set.
9	FS	First Descriptor When set it indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the second buffer contains the beginning of the

frame. If the buffer size of the second buffer is also 0, the second descriptor con tains the beginning of the frame. It is valid only when the last descriptor RDES0<8> set.

8	LS	Last Descriptor When set it indicates that the pointer contains the last buffers of the frame. It is valid only when the last desriptor RDES0<8> is set.
7	TL	Frame Too Long When set it indicates that the frame length exceeds the maximum Ethernet-specified size of 1518 bytes. It is valid only when the last desriptor RDES0<8> is set.
6	CS	Collision Seen When set it indicates a late collision, or that the frame was damaged by a collision occurring after 64 bytes followed by the start frame delimiter SFD. It is valid only when the last desriptor RDES0<8> is set.
5	FT	Frame Type When set it indicates that the frame is an Ethernet-type frame (the frame length is greater than 1500 bytes). When reset it indicates that the frame is an IEEE 802.3 frame. It is not valid for runt frames of less than 14 bytes. It is valid only when the last desriptor RDES0<8> is set.
4	RW	Receive Watchdog When set it indicates the received watchdog timer expired when receiving the current frame with length greater than 2048 bytes through 2560 bytes. The PMAC sets the watchdog timeout on CSR5<9>. When it is set the frame length RDES0<30:16> is not valid. It is valid only when the last desriptor RDES0<8> is set.
2	DB	Dribbling Bit When set it indicates that the frame size is a noninteger multiple of 8 bits. It is set only if the number of dribbling bits in the last byte is 4 in MII/SYM operation mode, or at least 3 in 10 Mbps serial operation mode. It is not valid if either the collisiion seen RDES0<6> or the runt frame RDES0<11> is set. If set, and the CRC error RDES0<1> is clear, then the frame is valid. It is valid only when the last desriptor RDES0<8> is set.
1	CE	CRC Error When set it indicates that a CRC error occurred on the received frame. The bit is also set when the MII_ERR pin is asserted during the reception of a packet even though the CRC may be correct.
0	OF	Overflow When set it indicates that the PMAC truncated the received data due to FIFO overflow. It is valid only when the last desriptor RDES0<8> is set.

5.4.3.3. RECEIVE DESCRIPOR 1 FORMAT

Fig. 16 shows the RDES1 bit map and its bit field is described in Table 10.

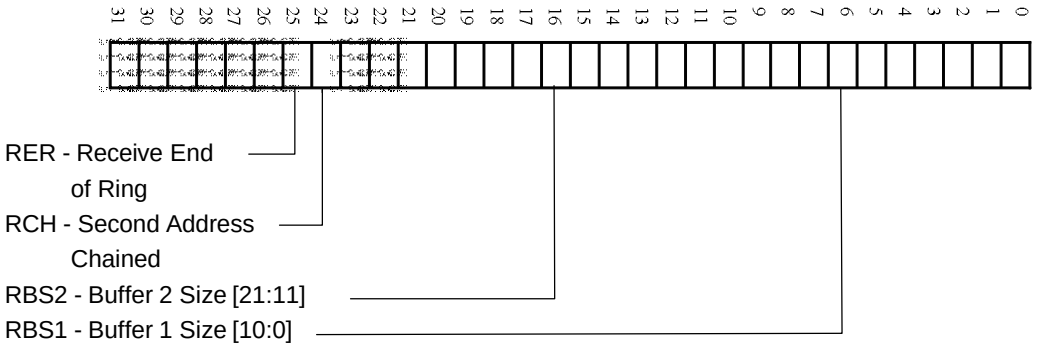

Fig. 16 -- RDES1 Receive Descriptor 1

Table 10 -- Receive descriptor 1

Field	Name	Description
25	RER	Receive End of Ring When set indicates that the descriptor is the last one of the descriptor lists and the PMAC returns to the base address CSR3. This creates a descriptor ring.
24	RCH	Second Address Chained When set indicates that the RDES3 is the next descriptor address, rather than the second buffer address. When set indicates the RDES3 is the next descriptor address, rather than the second buffer address. This is called explicit chained mod When reset the next descriptor address is the end of the previous descriptor address (i.e., the RDES3 address plus one) plus the skipping length CSR0<6:2>. This is a called implicit chained mode. The RDES1<25> takes precedence over the RDES1<24>.
21:11	RBS2	Buffer 2 Size Indicates the size, in bytes, of the second data buffer. If this field is 0, the PMAC ignores this buffer and fetches the next descriptor. It must be a multiple of 4. It is not valid if the RDES1<24> is set.
10:0	RBS1	Buffer 1 Size Indicates the size, in bytes, of the first data buffer. If this field is 0, the PMAC ignores this buffer and uses buffer 2. It must be a multiple of 4.

5.4.3.4. RECEIVE DESCRITPOR 2 FORMAT

Fig. 17 shows the RDES1 bit map and the bit field is described in Table 11.

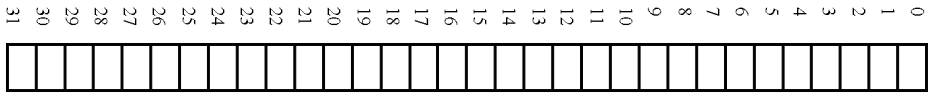

Fig. 17 -- RDES2 Receive Descriptor 2

Table 11 -- Receive descriptor 2

Field	Name	Description
31:0	Buffer Address 1	Physical address of buffer 1. The buffer must be longword aligned, i.e., the RDES2<1:0> = 00.

5.4.3.5. RECEIVE DESCRIPTOR 3 FORMAT

Fig. 18 shows the RDES3 bit map and the bit field is described in Table 12.

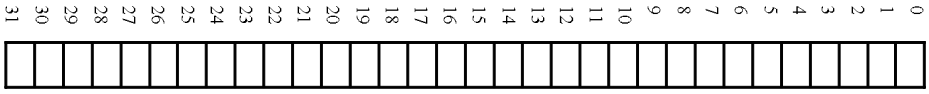

Fig. 18 -- RDES3 Receive Descriptor 3

Table 12 -- Receive descriptor 3

Field	Name	Description
31:0	Buffer Address 2	Physical address of buffer 2. The buffer must be longword aligned, i.e., the RDES3<1:0> = 00h.

5.4.3.6. RECEIVE OPERATION

There are two types of received packets in terms of number of descriptors used for the packet. One is called complex packet which uses multiple descriptors to buffer the whole packet, the other one is called simple packet which uses only one descriptor. Since buffer size can be either small or large, different sizes of packets use different numbers of buffers which need several descriptors. During receiving, RX DMA will pre-acquire a free descriptor and use it for first incoming packet. When current buffer is not enough to keep the whole received packet, RX DMA acquires next descriptor to continue moving data out of RX FIFO. If the newly acquired descriptor is owned by host and current packet is not to its end, a descriptor error flag is generated and RX FIFO will purge the remaining data of the current packet left in RX FIFO.

5.4.3.7. OVERFLOW AND RX FIFO CONTROL

It is possible that network fills up the RX FIFO when PCI bus has been busy enough to show down the data throughput between RX FiFO & host memory. No interrupt is issued when RX FIFO overflow occurs. RX descriptor will record such status.

5.4.4. TRANSMIT BUFFER MANAGEMENT

To begin transmission, the system software issues the start transmission command CSR6<13>. The transmit buffer management uses descriptor lists and data buffers in the host memory for transmitting packets. During transmission, the PMAC fetches control information from the descriptor list, loads its appropriate registers, and then transmits the data from the data buffer.The PMAC writes the status information back to the corresponding descriptor when the transmission is complete. From a single transmit command, packets can either be transmitted singly or in groups if several descriptors have been linked together. The capability to transmit packets in groups is called pipelined transmission.

5.4.4.1 TRANSMIT DESCRIPTOR STRUCTURE

Fig.19 shows the transmit descriptor format. Providing status, two buffer byte-counters, and two address pointers in each descriptor enables the adapter to be applied to various types of memory management schemes.

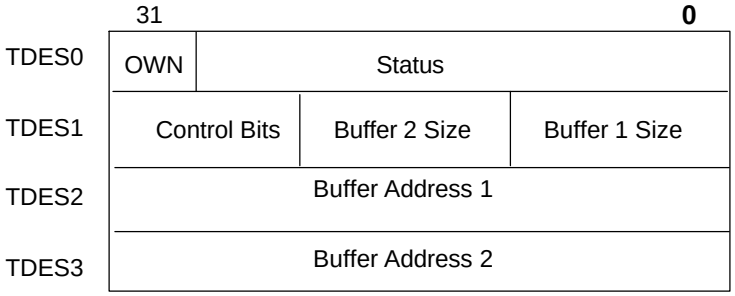

Fig. 19 -- Transmit Descriptor Format

5.4.4.2. TRANSMIT DESCRIPTOR 0 FORMAT

TDES0 includes the descriptor ownership and the transmitted frame status. Fig. 20 shows the TDES0 bit map and the bit field is described in Table 13.

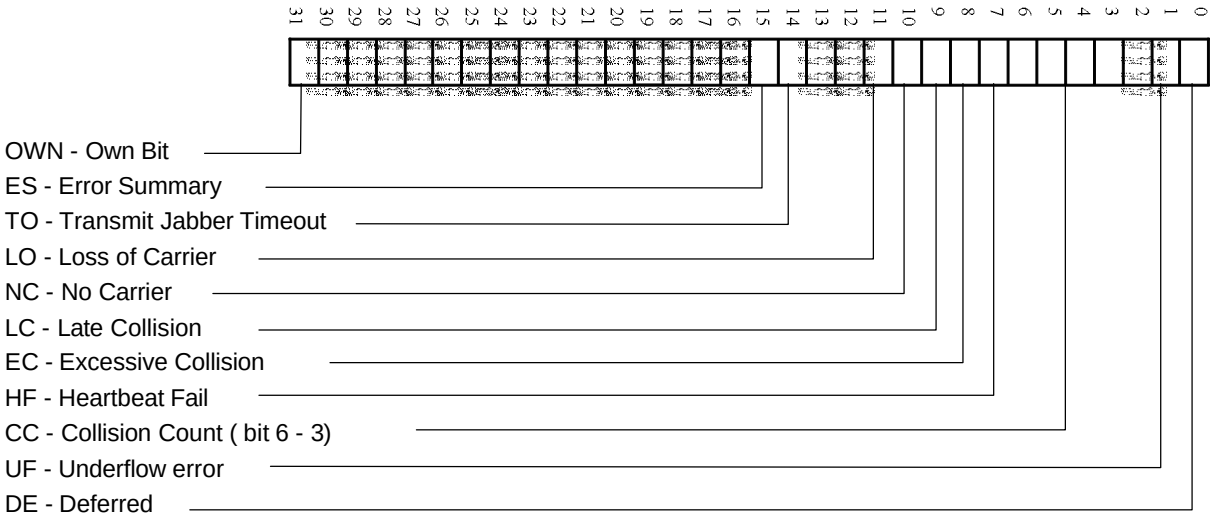

Fig. 20 -- TDES0 Transmit Descriptor 0

Table 13 -- TDES0 Transmit Descriptor 0

Field	Name	Description
31	OWN Bit	When reset indicates that the host has the ownership of the descriptor. When set indicates that the PMAC owns the descriptor. The driver needs to clear this bit during initialization.The PMAC clears the bit when it completes the frame transmission. It should be noted that the ownership bit of the first descriptor of the frame should be set after the subsequent descriptors of the same frame have been set. This avoids the contention that the PMAC is fetching the descriptor and the host is setting the ownership bit.
15	ES	Error Summary Indicates any one of the following transmit errors: Underflow error - TDES0<1> Excessive collision - TDES0<8> Late collision - TDES0<9> No carrier - TDES0<10> Loss of carrier - TDES0<11> Transmit jabber timeout - TDES0<14>
14	TO	Transmit Jabber Timeout When set indicates that the transmit jabber timer timed out and that the

		PMAC transmitter is still active. The transmit jabber timeout interrupt CSR5<3> is set. The transmission process is aborted and placed in the STOPPED state.
11	LO	Loss of Carrier When set indicates loss of carrier during transmission. It is not valid in internal loopback mode when CSR6<11>10> = 01.
10	NC	No Carrier When set indicates no carrier signal present during transmission. It is not valid in internal loopback mode CSR6<11:10> = 01.
9	LC	Late Collision When set indicates that the transmission is aborted due to collision occurring after the collision window of 64 bytes. It is not valid if the underflow error TDES0<1> is set.
8	EC	Excessive Collision When set indicates that the tansmission is aborted due to 16 successive collisions occurring while attempting to transmit the frame.
7	HF	Heartbeat Fail The bit is useful only in 10Mbps operating mode. When set indicates a heartbeat collision check failure (the transceiver fails to return a collision pulse as a chek after a transmission).
6:3	CC	Collision Count The 4-bit counter indicates the number of collisions occurred before the frame is transmitted.
1	UF	Underflow Error When set indicates that the PMAC encountered an empty transmit FIFO because the data was received late from the host while a frame was transmitting. The PMAC transmission process enters suspended state and sets both the transmit underflow CSR5<5> and the transmit interrupt CSR5<0>.
0	DE	Defer Error When set indicates that the PMAC has to defer the frame transmission because the carrier is asserted.

5.4.4.3. TRANSMIT DESCRIPTORS 1 FORMAT

TDES1 contains the control bits and two byte count buffers. Fig. 21 shows the TDES1 bit map and the bit field is described in Table 14.

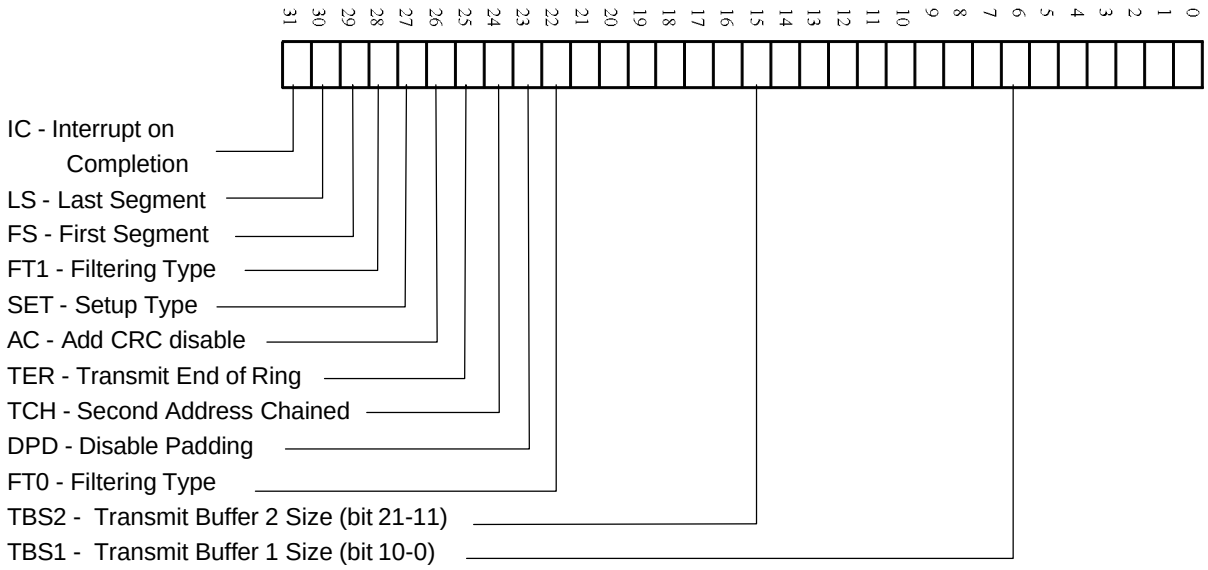

Fig. 21 TDES1 Transmit Descriptor 1

Table 14 -- TDES1 Transmit Descriptor 1

Field	Name	Description
31	IC	Interrupt on Completion When set the PMAC sets the transmit interrupt CSR5<0> after the present frame has been transmitted. It is valid only when the last segment TDES1<30> is set.
30	LS	Last Segment When set indicates that the buffer contains ths last segment of a frame.
29	FS	First Segment When set indicates that the buffer contains the first segment of a frame.
28	FT1	Filtering Type The filtering type is list in Table 15.
27	SET	Setup Packet When set indicates that the current descriptor is a setup frame descriptor.

26	AC	Add CRC Disable When set the cyclic redundancy check (CRC) will not be appended to the end of the transmitted frame. It is valid only when the frist segment TDES1<29> is set.
25	TER	Transmit End of Ring When set indicates that the current descriptor is the last one of the descriptor lists, and the PMAC returns to the root address (see CSR4 description). This creates a descriptor ring.
24	TCH	Second Address Chained When set indicates the TDES3 is the next descriptor address, rather than the second buffer address. This is called explicit chained mode. When reset the next descriptor address is the end of the previous descriptor address (i.e., the TDES3 address plus four) plus the skipping length CSR0<6:2>. This is called the implicit chained mode. The TDES1<25> takes precedence over the TDES1<24>.
23	DPD	Disable Padding When set indicates that the PMAC does not automatically add a padding (dummy) field to a packet shorter than 64 bytes. When reset the PMAC automatically adds a padding field and also a CRC to a packet shorter than 64 bytes. Despite the state of the added CRC disable TDES1<26>, the CRC field is appended also.
22	FT0	Filtering Type see Table 15.
21:11	TBS2	Buffer 2 Size Indicates the size in byte of the second data buffer. If the field is 0h, the PMAC ignores this buffer and fetches the next descriptor. It is not valid if the second address chained TDES1<24> is set.
10:0	TBS1	Buffer 1 Size Indicates the size in byte of the second data buffer. If this field is 0h, the PMAC ignores this buffer and used buffer 2.

Table 15 -- Filtering Type

FT<1:0>	Description
00	Perfect Filtering Indicates that the descriptor buffer contains a setup perfect table of 16 addresses, the PMAC sets the filtering mode Table 5.2.5.4 to perfect filtering.
01	Hash Filtering Indicates that the descriptor buffer contains a setup hash table of 512-bit-plus-one perfect address. If an incoming receive packet destination address is a multicast address, the PMAC executes an imperfect address filtering compared with the hash table. Elses, if the incoming receive packet destination address is a physical address, it executes a perfect filtering compared with the perfect address.
10	Inverse Filtering Indicates that the descriptor buffer contains a setup perfect table of 16 addresses and the

PMAC sets the filtering mode Table 5.2.5.4 to inverse filtering. The PMAC receives the incoming frames with destination addresses that does not match the perfect addresses and rejects the frames with destination addresses that matches one of the perfect addresses.

11 Hash-Only Filtering
Indicates that the descriptor buffer contains a setup 512-bit hash table. If an incoming receive packet destination address is multicast or physical, the PMAC executes an imperfect address filtering against the hash table.Note that this field is valid only when setup frame TDES1<27> is set.

5.4.4.4. TRANSMIT DESCRIPTOR 2 FORMAT

Fig. 22 shows the TDES2 bip map and the bit field is described in Table 16.

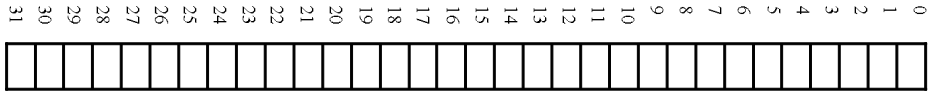

Fig. 22 -- TDES2 Transmit Descriptor 2

Table 16 Tansmit descriptor 2

Field	Name	Description
31:0	Buffer Address 1	Physical address of buffer 1. There is no limitation on the buffer address alignment.

5.4.4.5. TRANSMIT DESCRIPTOR 3 FORMAT

Fig. 23 shows the TDES3 bip map and the bit field is described in Table 17.



Fig. 23 -- TDES3 Transmit Descriptor 3

Table 17 Tansmit descriptor 3

Field	Name	Description
31:0	Buffer Address 2	Physical address of buffer 2. There is no limitation on the buffer address alignment.

5.4.4.6. TRANSMIT OPERATIONS

All fields except the status field in the descriptor and the base list register CSR4 must be initialized before the start transmission command CSR6<13> can be issued. If more than one packet are in queue, the descriptors must be linked together properly. The last descriptor may have TER=1 in TDES1<25> to return to the root address of the list and form a ring structure.

The transmission process is managed by a finite state machine. This state machine can be activated by either the start transmission command CSR6<13>, ST, when the current state is in STOPPED state or the poll command CAR0<18:17>, POLL, when the current state is in SUSPENDED state.

After a valid TX command, ST or POLL is accepted, the PMAC begins to fetch transmit descriptor (load TDES0, TDES1, TDES2 and TDES3). If the ownship of the TDES0 is set, the PMAC copies the buffer data to FIFO based on the buffer address TDES2, and on TDES3 if the descriptor is implicitly chained. The PMAC repeats the descriptor fetching and the data buffering until (1) the complete frame is queued into the transmit FIFO or (2) the byte count of the frame in the transmit FIFO is equal to or greater than the threshold, depending on the setting of the store and forward CSR6<21> and the threshold control bits CSR6<15:14>, and transmits the frame. Before completing the current frame transmission, the PMAC can fetch the next descriptor and queue the data to the transmitting FIFO in advance called pipelined transmission. By means of the pipelined transmission, the fast back-to-back transmission is carried out and the performance is improved.

After transmission, the PMAC closes the current descriptor by clearing the Own bit of TEDSO and simultaneously writing transmit status information to TDES0, and fetches next descriptor. The PMAC will enter either the SUSPEND state when the transmit lists are transmitted completely or a underrun error occurs, or the STOPPED state when a jabber error is detected or the stop transmission command CSR6<13> is issued.

5.4.4.7. UNDERRUN AND TX FIFO CONTROL

The network can't read data in the TXFIFO until the TXFIFO is filled over the threshold level in the normal mode or a frame is filled wholly in the store and forward mode. If the TXFIFO is filled by TXDMA not as quickly as the TXFIFO is read by network, an underflow flag will be set. We don't expect this situation to happen.
If underflow flag is set, an interrupt can be issued depending on CSR7<5>. The TX descriptor will record such status.

5.4.5. DMA ARBITRATION

Arbitration schemes can be chosen by programming the BAR bit of CSR0.1. RX process will have the precedence of TX process during R+ arbitration scheme when the free space in RX FIFO is in critical condition (internally determined). R+ scheme is used when BAR bit is reset. The Round Robin scheme is applied when BAR bit is set to 1 which grants equal access to PCI bus to both TX and RX process.

R+ Arbitration scheme: (BAR = 0, default mode after reset)

This scheme is in favor of RX process when RX FIFO is in critical condition. If both TX and RX FIFOs are not in critical conditions, the Round Robin scheme is applied. This scheme should deliver the best DMA channels utilization.