Industrial Temperature, 3 Volt, MCP Products - Parallel NOR Flash + Pseudo Static RAM (pSRAM)

64Mb Page Mode Flash Memory (4M x 16Bit) and 32Mb pSRAM (2M x 16Bit)

MX69GL642E (Top Boot), MX69GL640E (Uniform Sector),

1. MCP FEATURES

- **Supply Voltage of 2.7 to 3.6 Voltage**

- **Speed**
  - Flash:
    - 64Mb: 70ns
  - pSRAM: 70ns

- **Package**
  - 7x9x1.2mm 56 Ball FBGA

- **Operating Temperature Range**
  - Industrial, -40°C to +85°C

Flash Memory General Features

- Sector architecture
  - MX69GL642E Top Boot:127 x 32Kword(64KB) + 8 x 4Kword(8KB) boot sector
  - MX69GL640E Uniform Sector:128 x 32Kword(64KB)
- 16-byte/8-word page read buffer
- 32-byte/16-word write buffer
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection function (Solid and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode
  - Deep power down current(max): 10uA (except MX69GL642EEXGI-70G/MX69GL640EEXGI-70G)

Pseudo SRAM General Features

- Organization: 2M x 16
- Power Supply Voltage: 2.7~3.6V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by UB#/LB#
- Auto-TCSR for power saving
- 8 page mode & DPD

2. Product Description

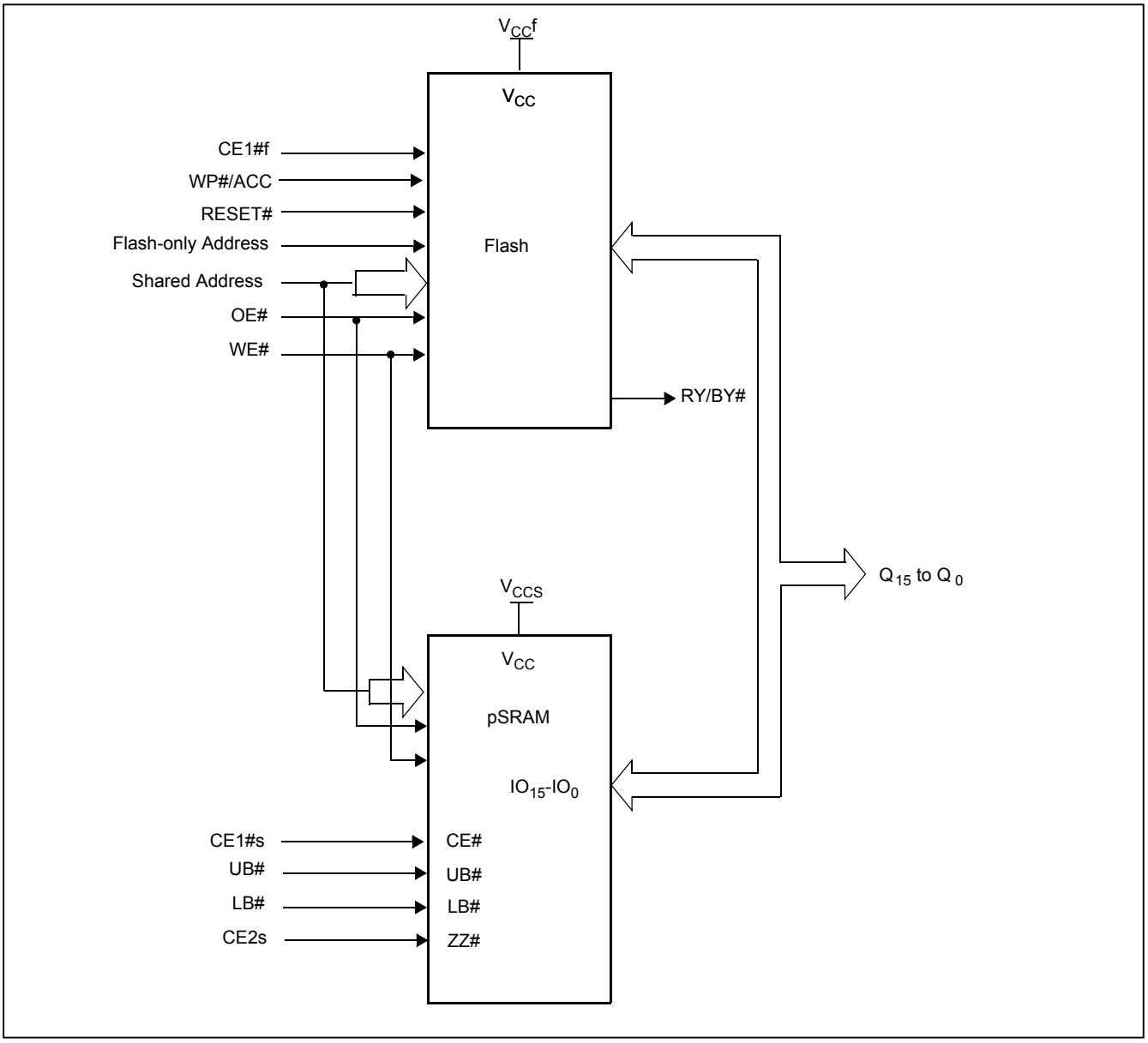
The MX69GL642E/640E-I product series combine MX29GL640E NOR Flash Memory with pSRAM in a Multi-Chip package. For detailed specifications, please refer to the individual datasheet for MX29GL640E flash and pSRAM.

3. Ordering Information

Device	Flash Density	Flash Access Time	pSRAM Density	pSRAM Access Time	Package type	Industrial Grade
MX69GL642EAXGI-70G	64Mb (Top)	70	32Mb	70	7x9 56FBGA	V
MX69GL642EJXGI-70G	64Mb (Top)	70	32Mb	70	7x9 56FBGA	V
MX69GL640EAXGI-70G	64Mb (Uniform Sector)	70	32Mb	70	7x9 56FBGA	V
MX69GL640EJXGI-70G	64Mb (Uniform Sector)	70	32Mb	70	7x9 56FBGA	V
MX69GL642EEXGI-70G	64Mb(Top)	70	32Mb	70	7x9 56FBGA	V
MX69GL640EEXGI-70G*	64Mb (Uniform Sector)	70	32Mb	70	7x9 56FBGA	V

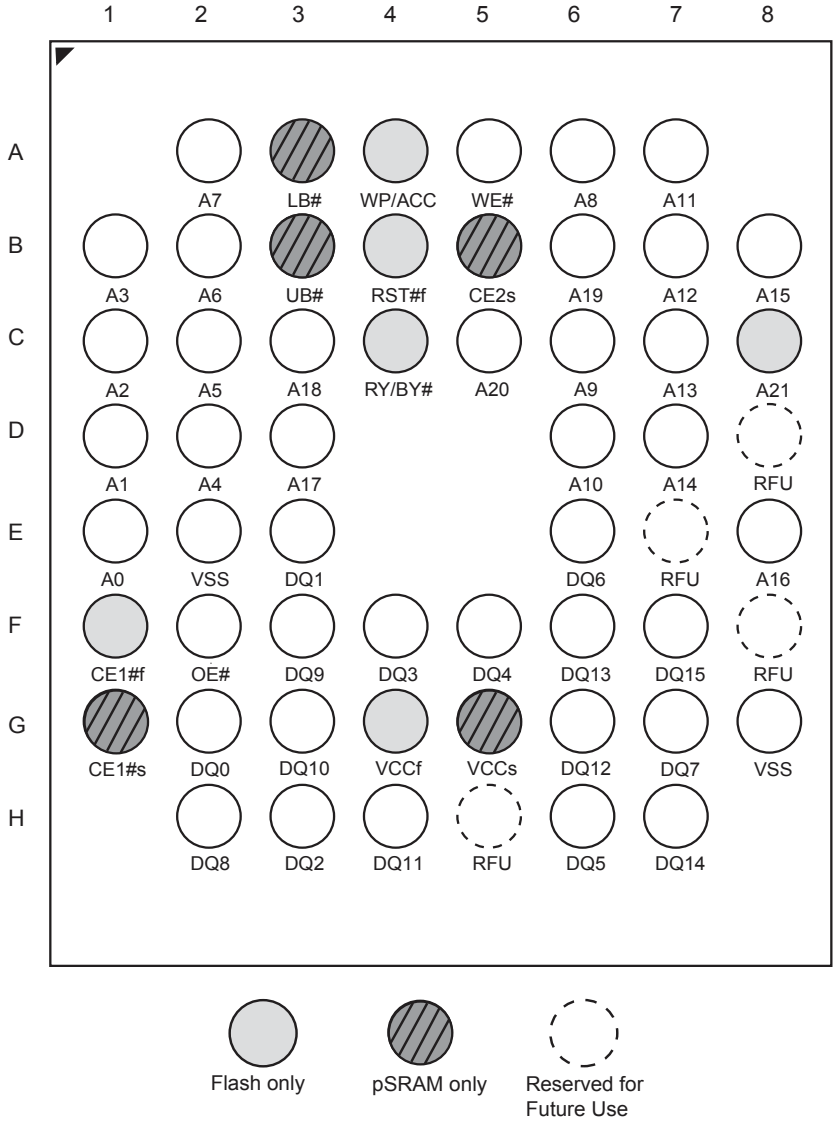
* Advanced Information.

4. BLOCK DIAGRAM



5. PIN CONFIGURATIONS

56-ball Fine-Pitch Ball Grid Array
(Top view through package)



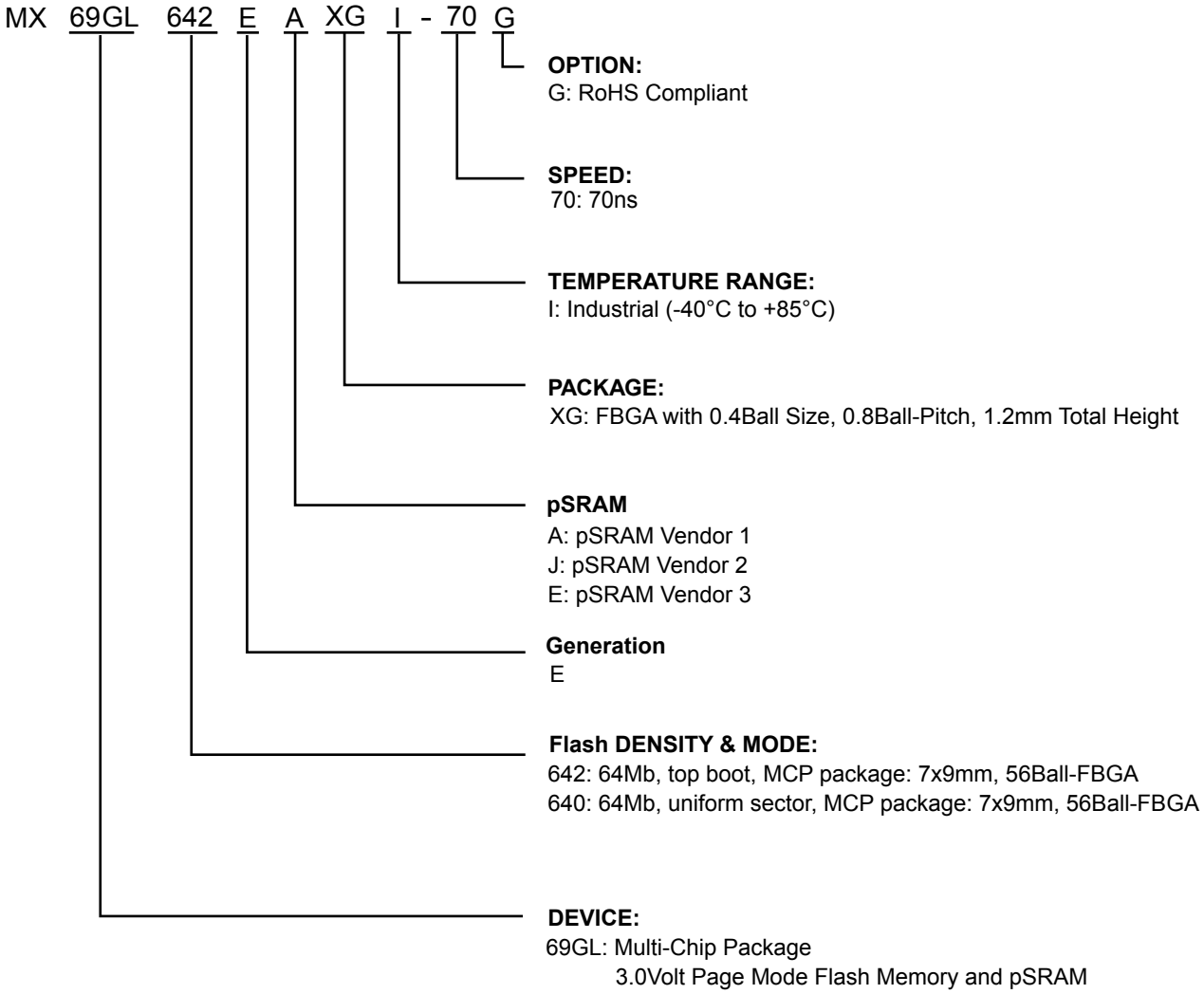
Notes:
1. The addess shared by MCP combination as show in the table below:

MCP	Flash-only Addresses	Shared Addresses
MX69GL642EA	A21	A20~A0
MX69GL642EJ		
MX69GL640EA		
MX69GL640EJ		
MX69GL642EE		
MX69GL640EE		

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A21~A0	22 Address Inputs for Flash 64Mb (A20~A0 are shared with pSRAM)
Q15~Q0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable Input 1 (Flash)
CE1#s	Chip Enable Input 1 (pSRAM)
CE2s	Chip Enable Input 2 (pSRAM)
OE#	Output Enable Input (Common)
WE#	Write Enable Input (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM)
LB#	Lower Byte Control (pSRAM)
RESET#	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
Vccf	Flash 3.0 volt-only single power supply
VCCS	pSRAM Power Supply
VSS	Device Ground (Common)
NC	Pin Not Connected Internally

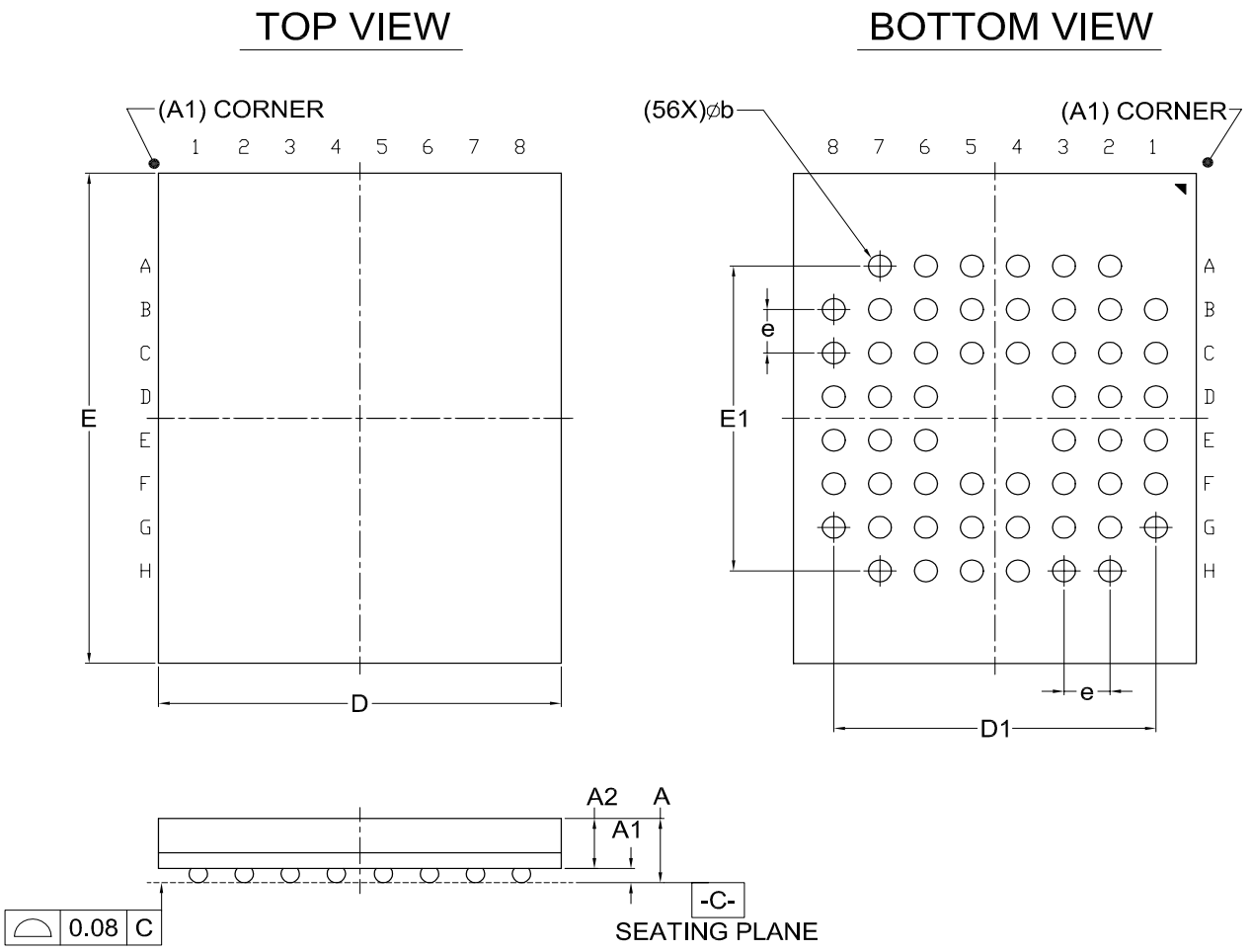
6. PART NAME DESCRIPTION



7. PACKAGE INFORMATION

56 Ball-FBGA

Package Outline for CSP 56BALL(7X9X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	6.90	---	8.90	—	—
	Nom.	---	0.30	—	0.40	7.00	5.60	9.00	5.60	0.80
	Max.	1.20	0.35	—	0.45	7.10	---	9.10	—	—
Inch	Min.	---	0.010	0.026	0.014	0.272	---	0.350	—	—
	Nom.	---	0.012	—	0.016	0.276	0.220	0.354	0.220	0.031
	Max.	0.047	0.014	—	0.018	0.280	---	0.358	—	—

8. REVISION HISTORY

Revision No.	Description	Page	Date
0.00	1. Initial released	All	APR/11/2011
1.0	1. Removed Advanced Information state	P2	APR/19/2011
1.1	1. Removed MX69GL638EAXGI-70G/MX69GL638EJXGI-70G	All	SEP/17/2014
	2. Added MX69GL640EEXGI-70G/MX69GL642EEXGI-70G	All	
1.2	1. Removed Advanced Information state for MX69GL642EEXGI-70G	P3	JAN/09/2015

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