SLC NAND FLASH and LPDDR2 162-Ball MCP (Multi-Chip Package)

Key Features

NAND Flash Features:

- *Low Power Dissipation*
- *High Reliability*

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1. MCP FEATURES

Operation Temperature

- -30°C to +85°C
- -40°C to +85°C

Package

- 162-ball FBGA - 8.0mmx10.5mm, 1.0mm (h) (max), 0.5mm pitch

NAND Flash Features

- **1G-bit/2G-bit/4G-bit SLC NAND Flash**
  - Bus: x8 / x16
  - 8 bit-ECC SLC NAND Flash:
    Page size: (2048+112) byte for x8 bus, (1024+56) word for x16 bus
    Block size: (128K+7K) byte for x8 bus, (64K+2K) word for x16 bus
  - 4 bit-ECC SLC NAND Flash:
    Page size: (2048+64) byte for x8 bus, (1024+32) word for x16 bus
    Block size: (128K+4K) byte for x8 bus, (64K+2K) word for x16 bus
  - Plane size:
    1024-block/plane x 1 for 1Gb
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **User Redundancy**
  - 8 bit-ECC SLC NAND Flash:
    112-byte attached to each page
  - 4 bit-ECC SLC NAND Flash:
    64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 25ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1.0ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 ~ 1.95V
- **Low Power Dissipation**
  - Max. 30mA (1.8V)
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature (5 Cycles)**
- **High Reliability**
  - 8 bit-ECC SLC NAND Flash:
    Endurance: typical 100K cycles (with 8-bit ECC per (512+28) Byte)
  - 4 bit-ECC SLC NAND Flash:
    Endurance: typical 100K cycles (with 4-bit ECC per (512+16) Byte)
  - Data Retention: 10 years

LPDDR2 DRAM Features

- **JEDEC LPDDR2-S4B compliance**
- **DLL is not implemented**
- **Low power consumption**
- **Mobile RAM functions**
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - Deep power-down mode
  - Per Bank Refresh
- **VDD Definition:**

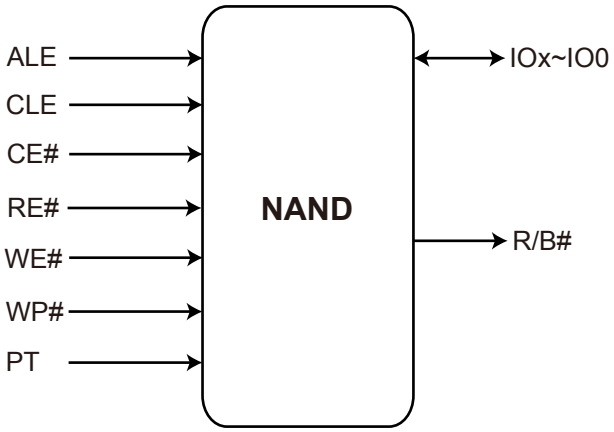
	Typical	Range
VDD1	1.8V	1.7~1.95V
VDD2	1.2V	1.14~1.3V
VDDQ	1.2V	1.14~1.3V

  - Voltage source of VREFCA is VDD2, VREFCA=1/2*VDD2 (from voltage divider)
  - Voltage source of VREFDQ is VDDQ, VREFDQ=1/2*VDDQ (from voltage divider)

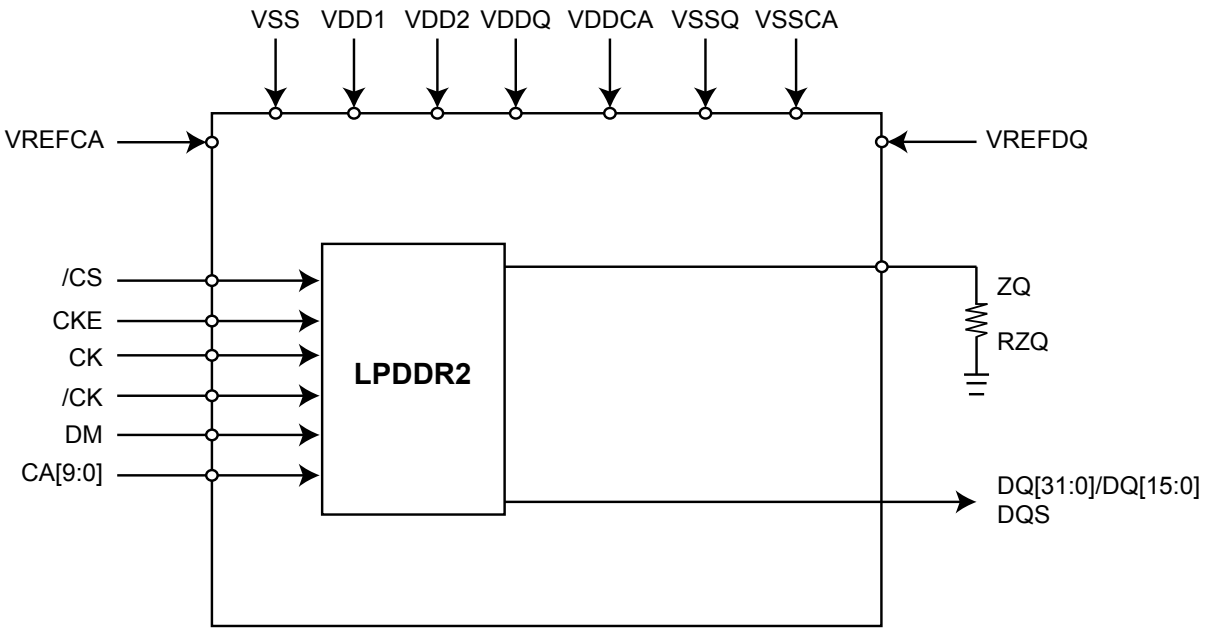
	Min.	Max.
VREFCA	0.49xVDD2	0.51xVDD2
VREFDQ	0.49xVDDQ	0.51xVDDQ

2. BLOCK DIAGRAM

NAND



LPDDR2



3. PART NAME DESCRIPTION

MX63 U 4G A 2G B A XM I 00

Option Code
00: -30°C to +85°C
01: -40°C to +85°C

Product Grade
I: Industrial

Package
XM: 162-Ball FBGA
XN: 130-Ball FBGA

MCP Combinations

Type	CE#	Combination
A	1,1	1 NAND; 1 LPDDR

LPDDR Configuration

Type		Bus	Vcc	Generation	Speed
A	DDR2	x16	1.7-1.95V	3	533MHz
B	DDR2	x32	1.7-1.95V	2	533MHz
C	DDR2	x32	1.7-1.95V	3	533MHz
E	DDR	x16	1.7-1.95V	5	200MHz
F	DDR	x32	1.7-1.95V	5	200MHz
J	DDR	x16	1.7-1.95V	5	200MHz
K	DDR	x32	1.7-1.95V	5	200MHz
G	DDR2	x16	1.7-1.95V	6	533MHz
H	DDR2	x32	1.7-1.95V	6	533MHz

LPDDR Density

256M = 56	2G = 2G
512M = 12	4G = 4G
1G = 1G	8G = 8G

NAND Configuration

Type	Bus	Number of ECC-bit	Generation
A	x8	8	1st
B	x16	8	1st
C	x8	4	1st
D	x16	4	1st
E	x8	4	2nd

NAND Density

512M = 12	8G = 8G
1G = 1G	16G = AG
2G = 2G	32G = BG
4G = 4G	64G = CG

NAND Voltage: 1.8V

Product Family
MX63U : NAND + LPDRAM MCP

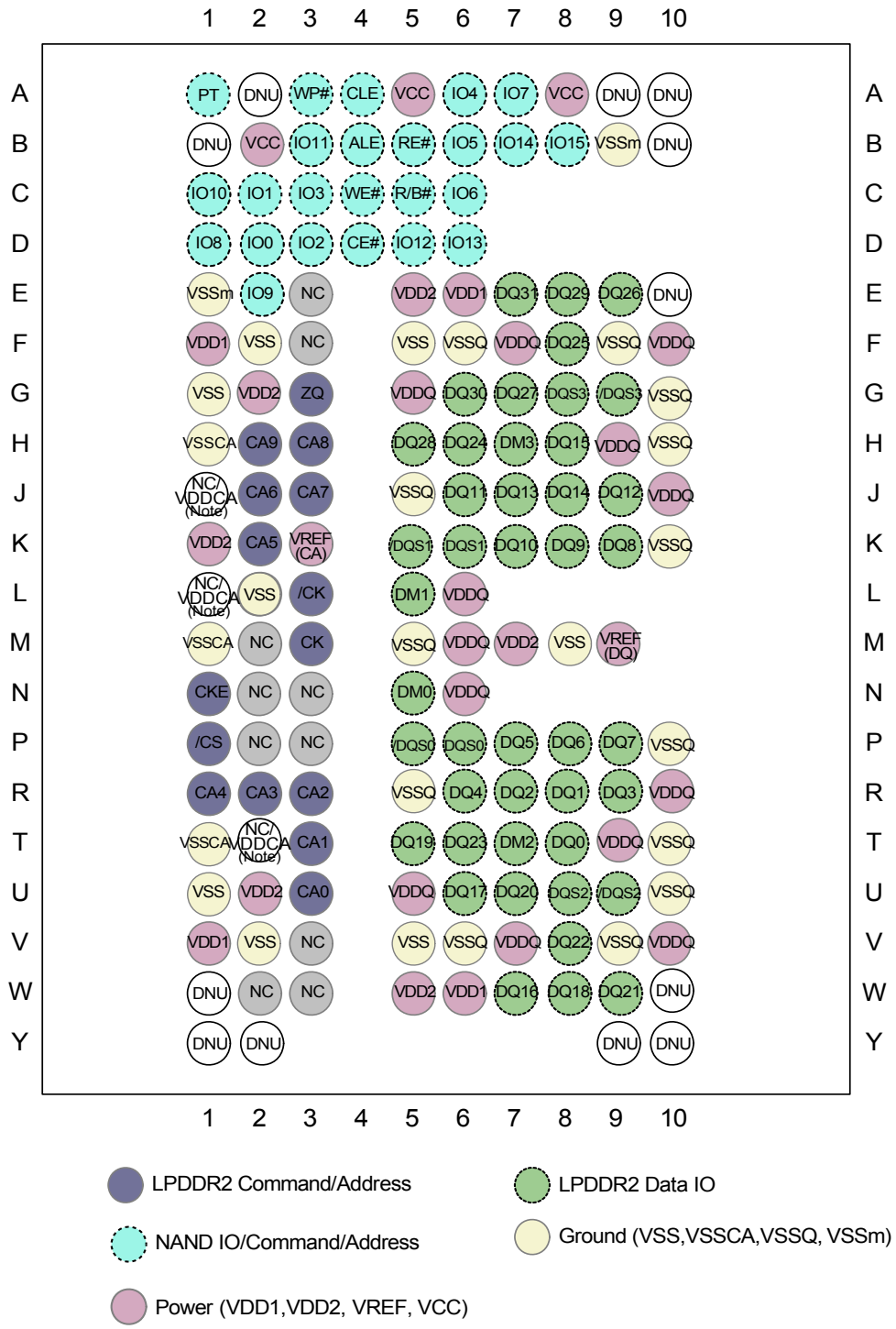
4. PRODUCT SELECTION GUIDE

Please contact our regional sales for the latest product selection and available form factors.

Item No.	Device	NAND Flash	Mobile DRAM	Package Type	VDDCA Pin
1.	MX63U4GA2GBAXMI00	4Gb, x8, 1.8V, 8-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
2.	MX63U4GC2GBAXMI00	4Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
3.	MX63U2GA1GCAXMI00	2Gb, x8, 1.8V, 8-bit ECC	1Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
4.	MX63U2GB1GCAXMI00	2Gb, x16, 1.8V, 8-bit ECC	1Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
5.	MX63U2GC1GCAXMI00	2Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
6.	MX63U2GC1GCAXMI01	2Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
7.	MX63U2GD1GCAXMI01	2Gb, x16, 1.8V, 4-bit ECC	1Gb, LPDDR2, x32, 1.8V	162 Ball BGA	
8.	MX63U1GC1GAAXMI00	1Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR2, x16, 1.8V	162 Ball BGA	
9.	MX63U1GD1GAAXMI00	1Gb, x16, 1.8V, 4-bit ECC	1Gb, LPDDR2, x16, 1.8V	162 Ball BGA	
10.	MX63U1GC1GCAXMI01	1Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR2, x32 1.8V	162 Ball BGA	
11.	MX63U1GC1GAAXMI01	1Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR2, x16, 1.8V	162 Ball BGA	
12.	MX63U4GC2GGAXMI00	4Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x16, 1.8V	162 Ball BGA	Yes
13.	MX63U4GC2GGAXMI01	4Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x16, 1.8V	162 Ball BGA	Yes
14.	MX63U4GC2GHAXMI00	4Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	Yes
15.	MX63U4GC2GHAXMI01	4Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	Yes
16.	MX63U4GA2GHAXMI00	4Gb, x8, 1.8V, 8bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	Yes
17.	MX63U2GE2GGAXMI00	2Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x16, 1.8V	162 Ball BGA	Yes
18.	MX63U2GE2GGAXMI01	2Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x16, 1.8V	162 Ball BGA	Yes
19	MX63U2GE2GHAXMI00	2Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	Yes
20	MX63U2GE2GHAXMI01	2Gb, x8, 1.8V, 4-bit ECC	2Gb, LPDDR2, x32, 1.8V	162 Ball BGA	Yes

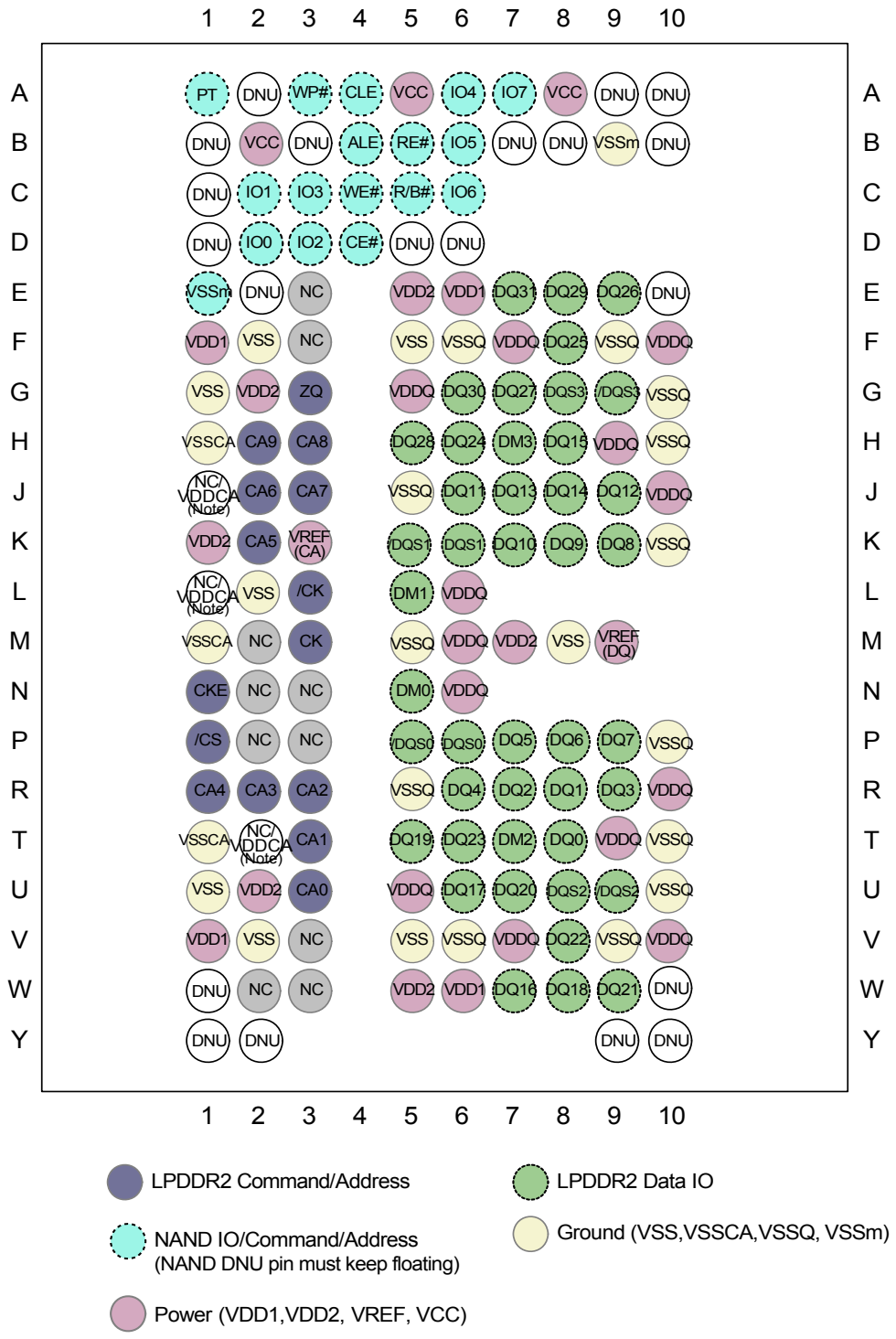
5. PIN CONFIGURATIONS

162-Ball, BGA (NAND x16; LPDDR x32)



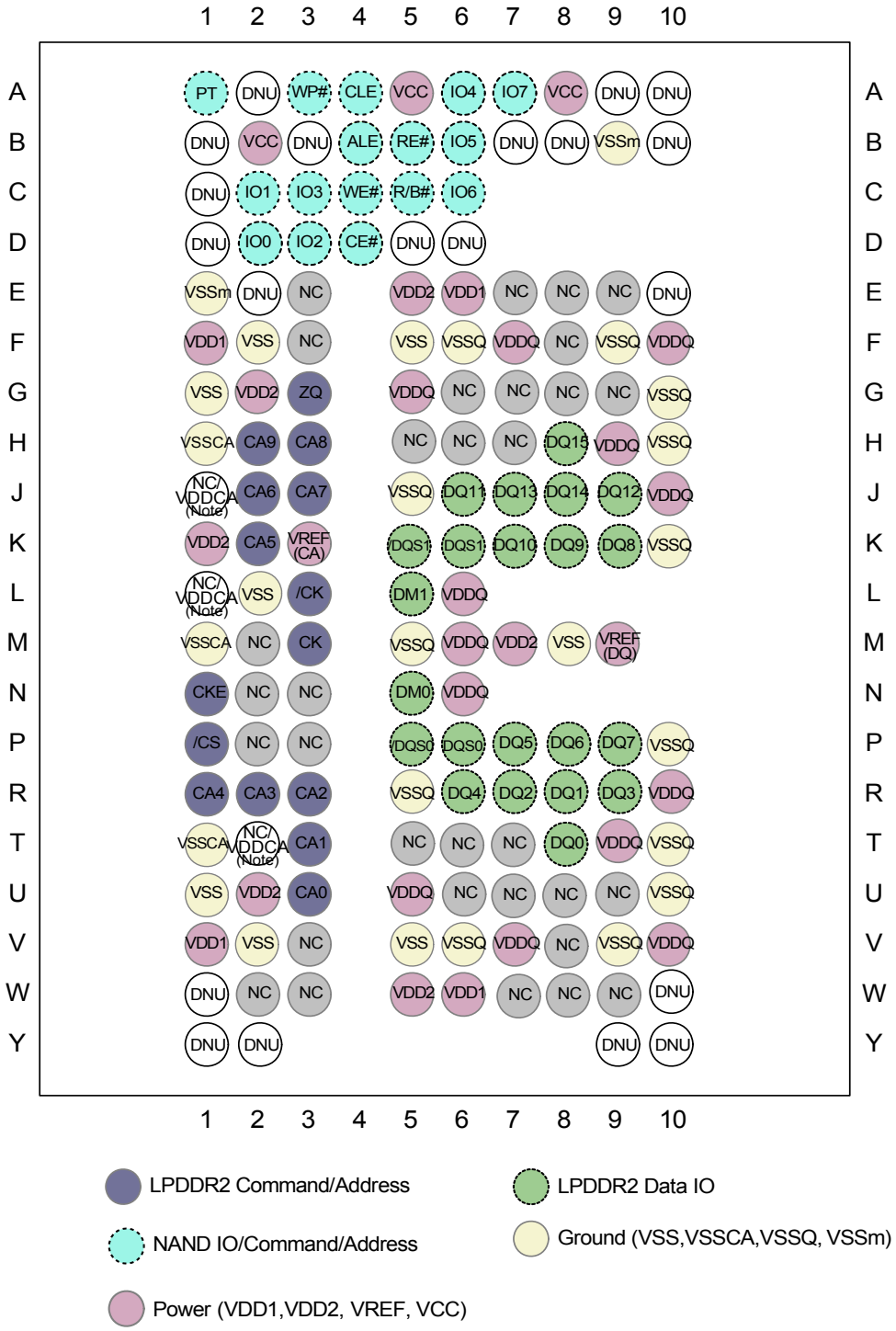
Note: Please check Product Selection Guide for NC pin or VDDCA pin support.

162-Ball, BGA (NAND x8; LPDDR x32)



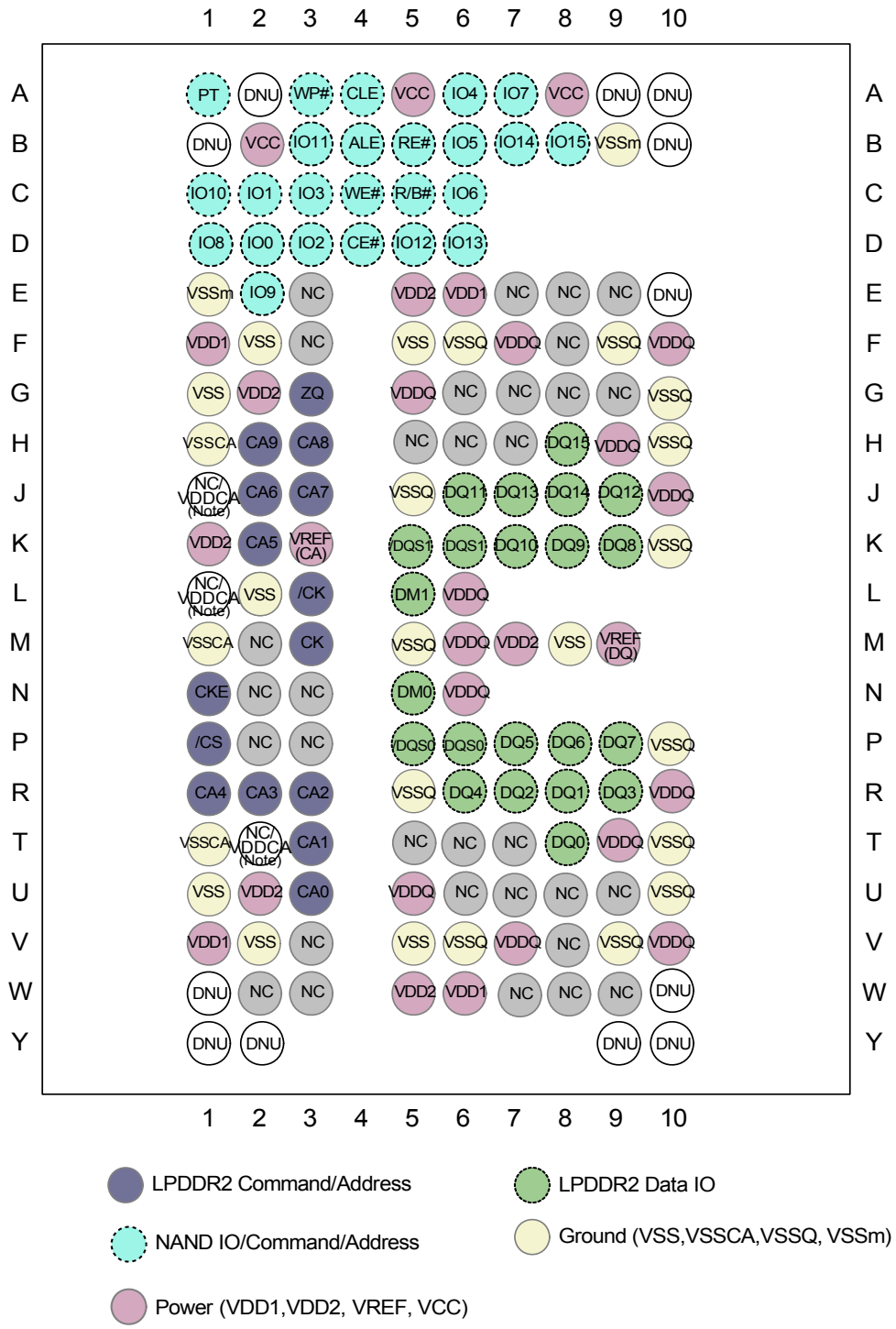
Note: Please check Product Selection Guide for NC pin or VDDCA pin support.

162-Ball, BGA (NAND x8; LPDDR x16)



Note: Please check Product Selection Guide for NC pin or VDDCA pin support.

162-Ball, BGA (NAND x16; LPDDR x16)



Note: Please check Product Selection Guide for NC pin or VDDCA pin support.

6. PIN DESCRIPTION

LPDDR2 x32

SYMBOL	DESCRIPTION	NAND Flash 4Gb (512Mb x8) 2Gb (256Mb x8) 1Gb (128Mb x8)	LPDDR2x32 2Gb (64Mb x32) 1Gb (32Mb x32)
I/O0 ~ I/OX	Data Input / Output	V	
CLE	Command Latch Enable	V	
ALE	Address Latch Enable	V	
CE#	Chip Enable	V	
WE#	Write Enable	V	
RE#	Read Enable	V	
WP#	Write Protect	V	
R/B#	Ready / Busy Out	V	
VCC	Supply Voltage	V	
VSSm	Ground	V	
PT	Chip Protection Enable	V	
/CS	Chip Select		V
CK, /CK	Differential Clocks		V
CKE	Clock Enable		V
CA0 ~ CA9	Command / Address		V
DQ0 ~ DQ31	Data I/O		V
DM0 ~ DM3	Input Data Mask		V
DQS0 ~ DQS3	Differential Data Strobe (rising edge)		V
/DQS0 ~ /DQS3	Differential Data Strobe (falling edge)		V
ZQ	Drive Strength Calibration		V
VREF(DQ)	Reference Voltage		V
VREF(CA)	Reference Voltage		V
VDD1	Core Power Supply		V
VDD2	Core Power Supply		V
VSS, VSSCA, VSSQ	Ground		V
VDDQ	I/O Power Supply		V
VDDCA	CA Power Supply		V
NC	No Connection		V
DNU *	Do Not Use	V	V

* : DNU pin of NAND must keep floating.

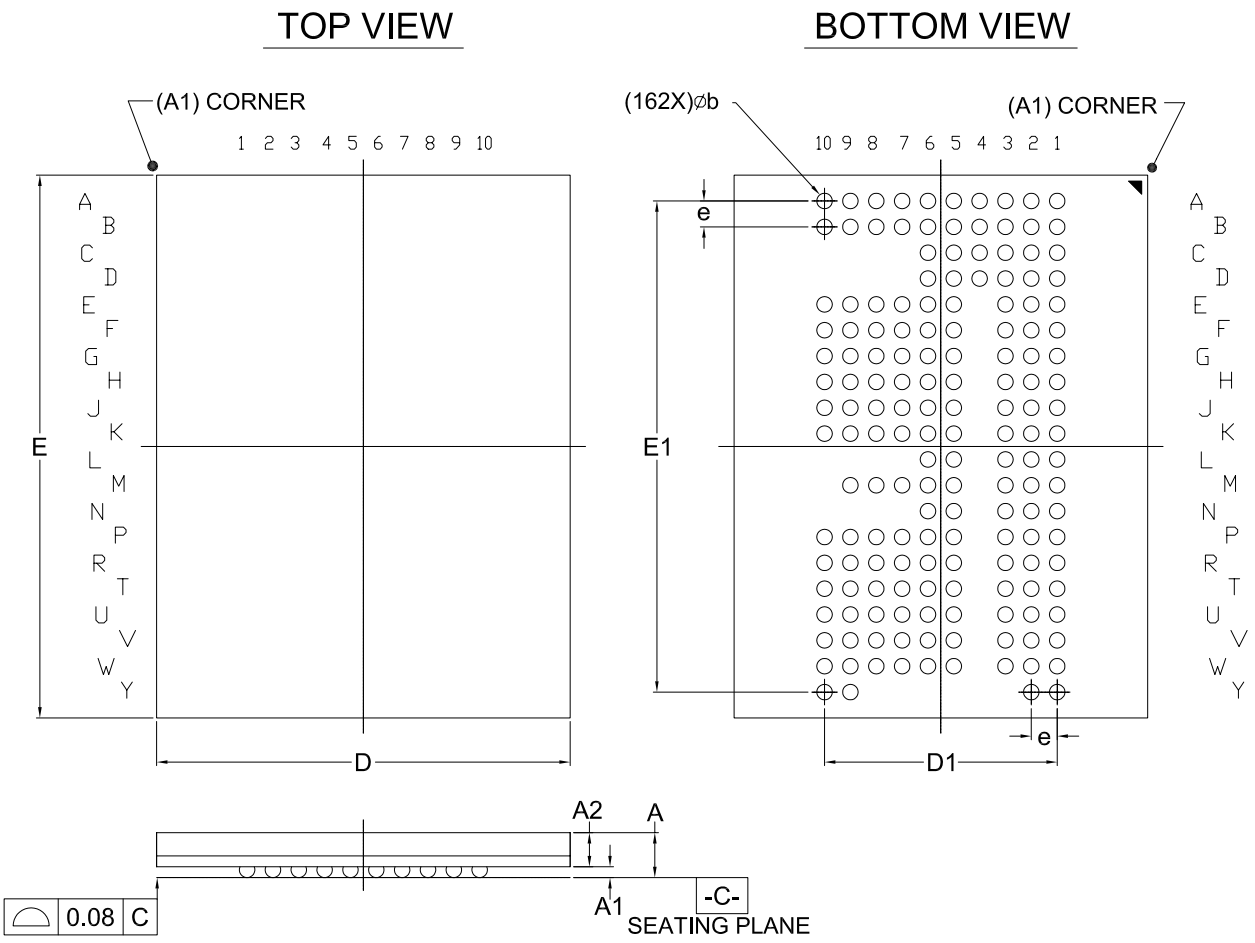
LPDDR2 x16

SYMBOL	DESCRIPTION	NAND Flash 4Gb (512Mb x8) 2Gb (256Mb x8) 1Gb (128Mb x8)	LPDDR2 x16 1Gb(64Mb x16)
I/O0 ~ I/OX	Data Input / Output	V	
CLE	Command Latch Enable	V	
ALE	Address Latch Enable	V	
CE#	Chip Enable	V	
WE#	Write Enable	V	
RE#	Read Enable	V	
WP#	Write Protect	V	
R/B#	Ready / Busy Out	V	
VCC	Supply Voltage	V	
VSSm	Ground	V	
PT	Chip Protection Enable	V	
/CS	Chip Select		V
CK, /CK	Differential Clocks		V
CKE	Clock Enable		V
CA0 ~ CA9	Command / Address		V
DQ0~DQ15	Data I/O		V
DM0~DM1	Input Data Mask		V
DQS0~DQS1	Differential Data Strobe (rising edge)		V
/DQS0~/DQS1	Differential Data Strobe (falling edge)		V
ZQ	Drive Strength Calibration		V
VREF(DQ)	Reference Voltage		V
VREF(CA)	Reference Voltage		V
VDD1	Core Power Supply		V
VDD2	Core Power Supply		V
VSS, VSSCA, VSSQ	Ground		V
VDDQ	I/O Power Supply		V
VDDCA	CA Power Supply		V
NC	No Connection		V
DNU *	Do Not Use	V	V

* : DNU pin of NAND must keep floating.

7. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 162BALL(8X10.5X1.0MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	--	0.16	0.61	0.25	7.90	---	10.40	---	---
	Nom.	--	0.21	---	0.30	8.00	4.5	10.50	9.5	0.50
	Max.	1.00	0.26	---	0.35	8.10	---	10.60	---	---
Inch	Min.	---	0.006	0.024	0.010	0.311	---	0.409	---	---
	Nom.	---	0.008	---	0.012	0.315	0.177	0.413	0.374	0.020
	Max.	0.039	0.010	---	0.014	0.319	---	0.417	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4270	0				

8. REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Modified PART NAME DESCRIPTION	P4	JUL/21/2014
	2. Removed the title "Advanced information"	All	
	3. Revised Bus information, Page program and Block erase time	P2	
	4. Revised block diagram (NAND)	P3	
1.1	1. Added VDD definition	P2	OCT/24/2014
	2. Added two part numbers: MX63U2GC1GCAXMI00 and MX63U4GC2GBAXMI00	P2,4,5	
1.2	1. Added part numbers: MX63U1GC1GAAXMI00, MX63U1GD1GAAXMI00, MX63U1GC1GAAXMI01, MX63U4GC2GBAXMI01,MX63U4GC2GGAXMI00, MX63U2GE2GGAXMI00, MX63U4GC2GGAXMI01 and MX63U2GE2GGAXMI01	P3-6,9, 11-12	APR/22/2015
	2. Modified VDDCA pin	P7-10	
	3. Revised PART NAME DESCRIPTION	P5	
	4. Added PIN CONFIGURATIONS: NAND x16; LPDDR x16	P10	
	5. Content modification	P7-9	
	6. Added Option Code (Operation Temperature)	P3,5	
1.3	1. Added part numbers: MX63U4GC2GHAXMI00, MX63U4GC2GHAXMI01 and MX63U2GE2GHAXMI00	P6	MAY/29/2015
	2. Removed Advanced Information "*" for MX63U4GC2GBAXMI00 and MX63U1GD1GAAXMI00	P6	
1.4	1. Removed two part numbers: MX63U4GB2GBAXMI00 and MX63U4GC2GBAXMI01	P6	JUN/11/2015
	2. Added part number: MX63U4GA2GHAXMI00	P6	
1.5	1. Removed Advanced Information "*" for three part numbers: MX63U2GC1GCAXMI00, MX63U1GC1GAAXMI00 and MX63U1GC1GAAXMI01	P6	OCT/29/2015
1.6	1. Added part number: MX63U2GE2GHAXMI01	P6	NOV/27/2015
1.7	1. Added part number: MX63U2GD1GCAXMI01	P6	DEC/14/2015
1.8	1. Added a statement for product ordering information.	P6	MAR/09/2016
	2. Removed all Advanced Information "*"	P6	
	3. Added two part numbers: MX63U2GC1GCAXMI01 MX63U1GC1GCAXMI01	P6	

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