# SLC NAND FLASH and LPDDR2 162-Ball MCP (Multi-Chip Package)

# 1. MCP FEATURES

## *Operation Temperature*

- -30°C to +85°C

## *Package*

- 162-ball FBGA - 8.0mmx10.5mm, 1.0mm (h) (max), 0.5mm pitch

## *NAND Flash Features*

- 2G-bit/4G-bit SLC NAND Flash
  - Bus: x8 / x16
  - 8 bit-ECC SLC NAND Flash:
    Page size: (2048+112) byte for x8 bus, (1024+56) word for x16 bus
    Block size: (128K+7K) byte for x8 bus, (64K+2K) word for x16 bus
  - 4 bit-ECC SLC NAND Flash:
    Page size: (2048+64) byte for x8 bus, (1024+32) word for x16 bus
    Block size: (128K+4K) byte for x8 bus, (64K+2K) word for x16 bus
  - Plane size:
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **User Redundancy**
  - 8 bit-ECC SLC NAND Flash:
    112-byte attached to each page
  - 4 bit-ECC SLC NAND Flash:
    64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 25ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1.0ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 ~ 1.95V
- **Low Power Dissipation**
  - Max. 30mA (1.8V)
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature (5 Cycles)**
- **High Reliability**
  - 8 bit-ECC SLC NAND Flash:
    Endurance: typical 100K cycles (with 8-bit ECC per (512+28) Byte)
  - 4 bit-ECC SLC NAND Flash:
    Endurance: typical 100K cycles (with 4-bit ECC per (512+16) Byte)
  - Data Retention: 10 years

## *LPDDR2 DRAM Features*

- **JEDEC LPDDR2-S4B compliance**
- **DLL is not implemented**
- **Low power consumption**
- **Mobile RAM functions**
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - Deep power-down mode
  - Per Bank Refresh
- **VDD Definition:**

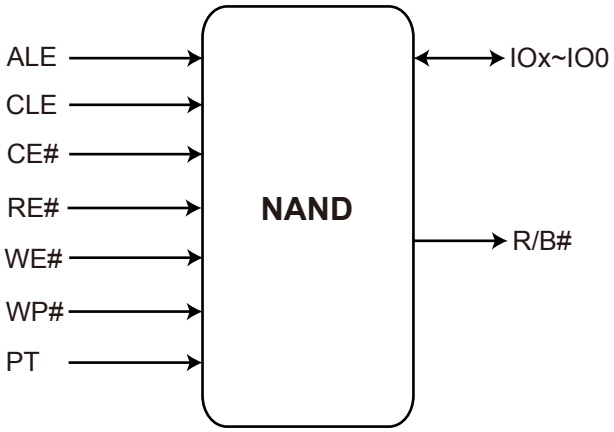
| | Typical | Range |
|---|---|---|
| VDD1 | 1.8V | 1.7~1.95V |
| VDD2 | 1.2V | 1.14~1.3V |
| VDDQ | 1.2V | 1.14~1.3V |

  - Voltage source of VREFCA is VDD2, VREFCA=1/2*VDD2 (from voltage divider)
  - Voltage source of VREFDQ is VDDQ, VREFDQ=1/2*VDDQ (from voltage divider)

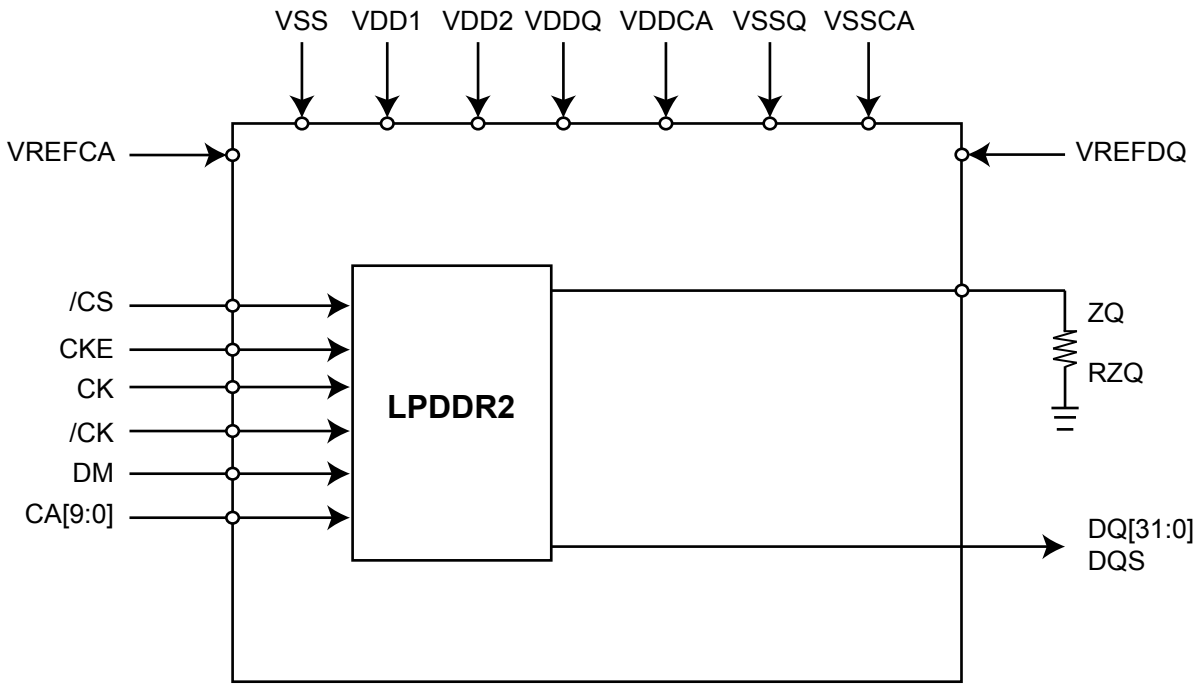
| | Min. | Max. |
|---|---|---|
| VREFCA | 0.49xVDD2 | 0.51xVDD2 |
| VREFDQ | 0.49xVDDQ | 0.51xVDDQ |

## 2. BLOCK DIAGRAM

### *NAND*




### *LPDDR2*



## 3. PART NAME DESCRIPTION

MX63 U 4G A 2G B A XM I 00

**Reserved**

**Product Grade**

I: Industrial

**Package**

**MCP Combinations**

| Type | CE# | Combination |
|---|---|---|
| A | 1,1 | 1 NAND; 1 LPDDR |

**LPDDR Configuration**

| Type | | Bus | Vcc | Generation | Speed |
|---|---|---|---|---|---|
| A | DDR2 | x32 | 1.7-1.95V | 1 | 200MHz |
| B | DDR2 | x32 | 1.7-1.95V | 2 | 533MHz |
| C | DDR2 | x32 | 1.7-1.95V | 3 | 533MHz |

**LPDDR Density**

256M = 56 2G = 2G
512M = 12 4G = 4G
1G = 1G 8G = 8G

**NAND Configuration**

| Type | Bus | Number of ECC-bit | Generation |
|---|---|---|---|
| A | x8 | 8 | 1st |
| B | x16 | 8 | 1st |
| C | x8 | 4 | 1st |
| D | x16 | 4 | 1st |

**NAND Density**

512M = 12 8G = 8G
1G = 1G 16G = AG
2G = 2G 32G = BG
4G = 4G 64G = CG

**NAND Voltage: 1.8V**

**Product Family**

MX63U : NAND + LPDRAM MCP

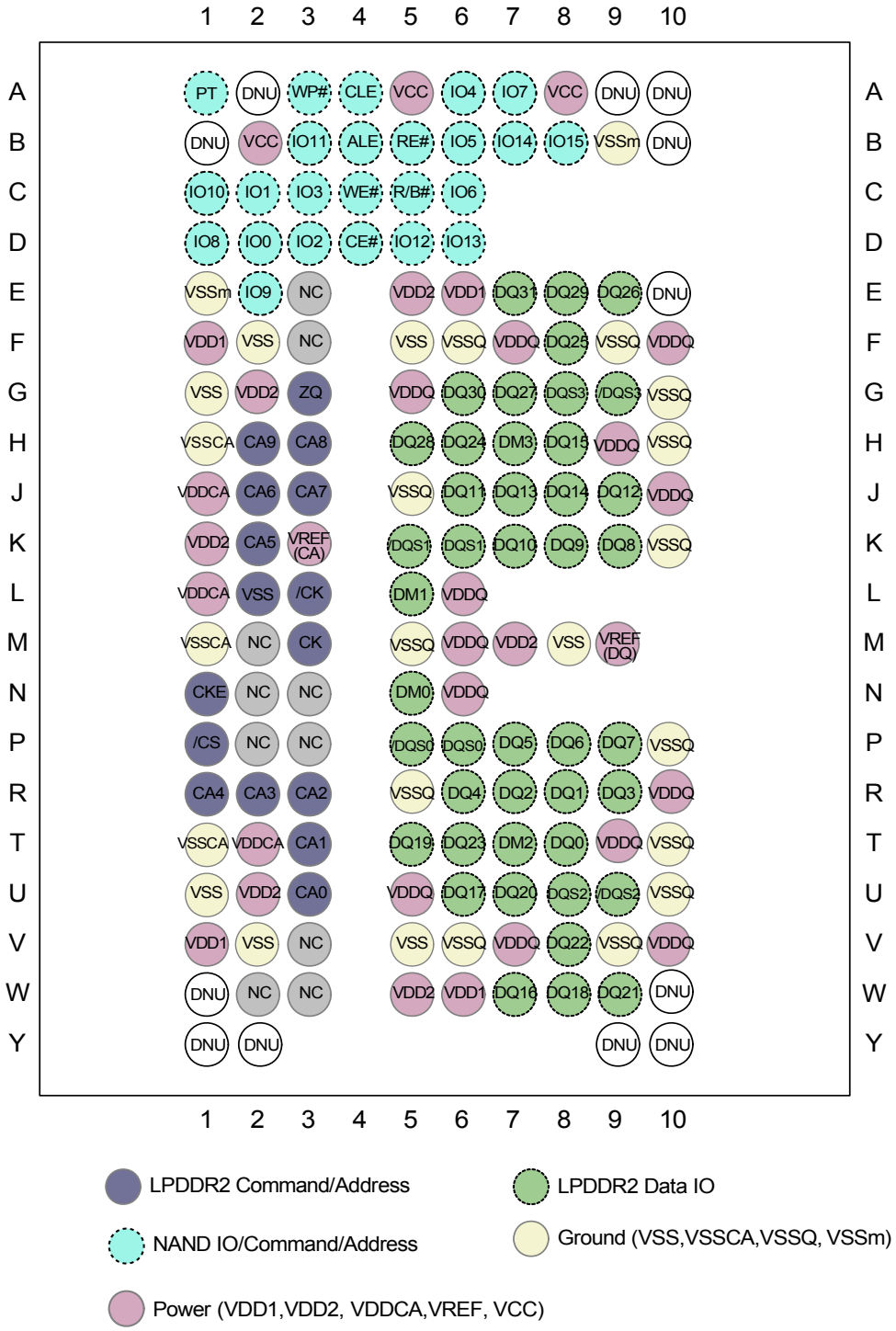
## 4. Product Selection Guide

| Device | NAND Flash | Mobile DRAM | Package Type |
|---|---|---|---|
| MX63U4GA2GBAXMI00 | 4Gb, x8, 1.8V, 8-bit ECC | 2Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |
| MX63U4GB2GBAXMI00 | 4Gb, x16, 1.8V, 8-bit ECC | 2Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |
| MX63U2GA1GCAXMI00 | 2Gb, x8, 1.8V, 8-bit ECC | 1Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |
| MX63U2GB1GCAXMI00 | 2Gb, x16, 1.8V, 8-bit ECC | 1Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |
| MX63U2GC1GCAXMI00 * | 2Gb, x8, 1.8V, 4-bit ECC | 1Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |
| MX63U4GC2GBAXMI00 * | 4Gb, x8, 1.8V, 4-bit ECC | 2Gb, LPDDR2, x32, 1.8V | 162 Ball BGA |

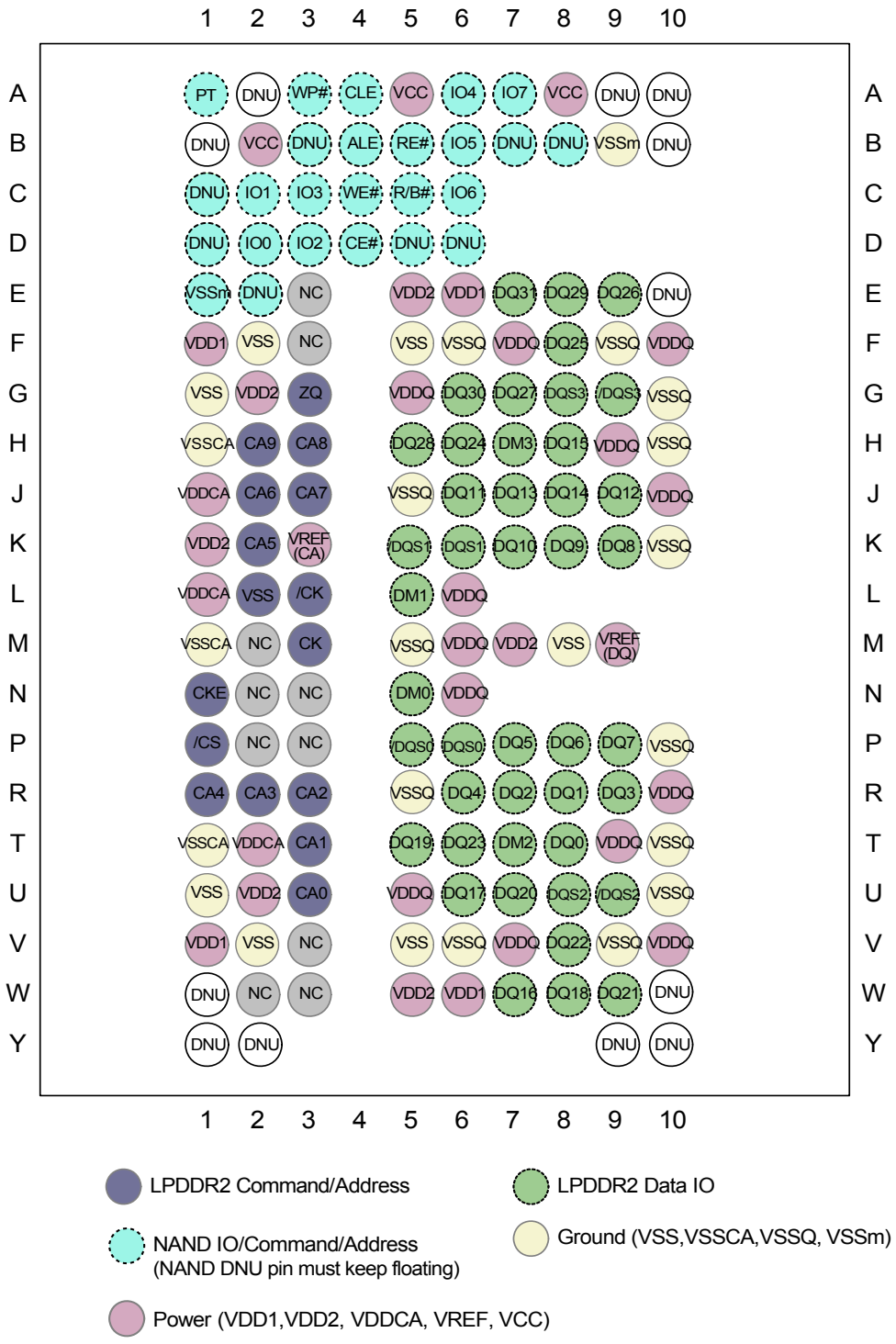
* Advanced Information

## 5. PIN CONFIGURATIONS

### 162-Ball, BGA (NAND x16; LPDDR x32)



**162-Ball, BGA (NAND x8; LPDDR x32)**



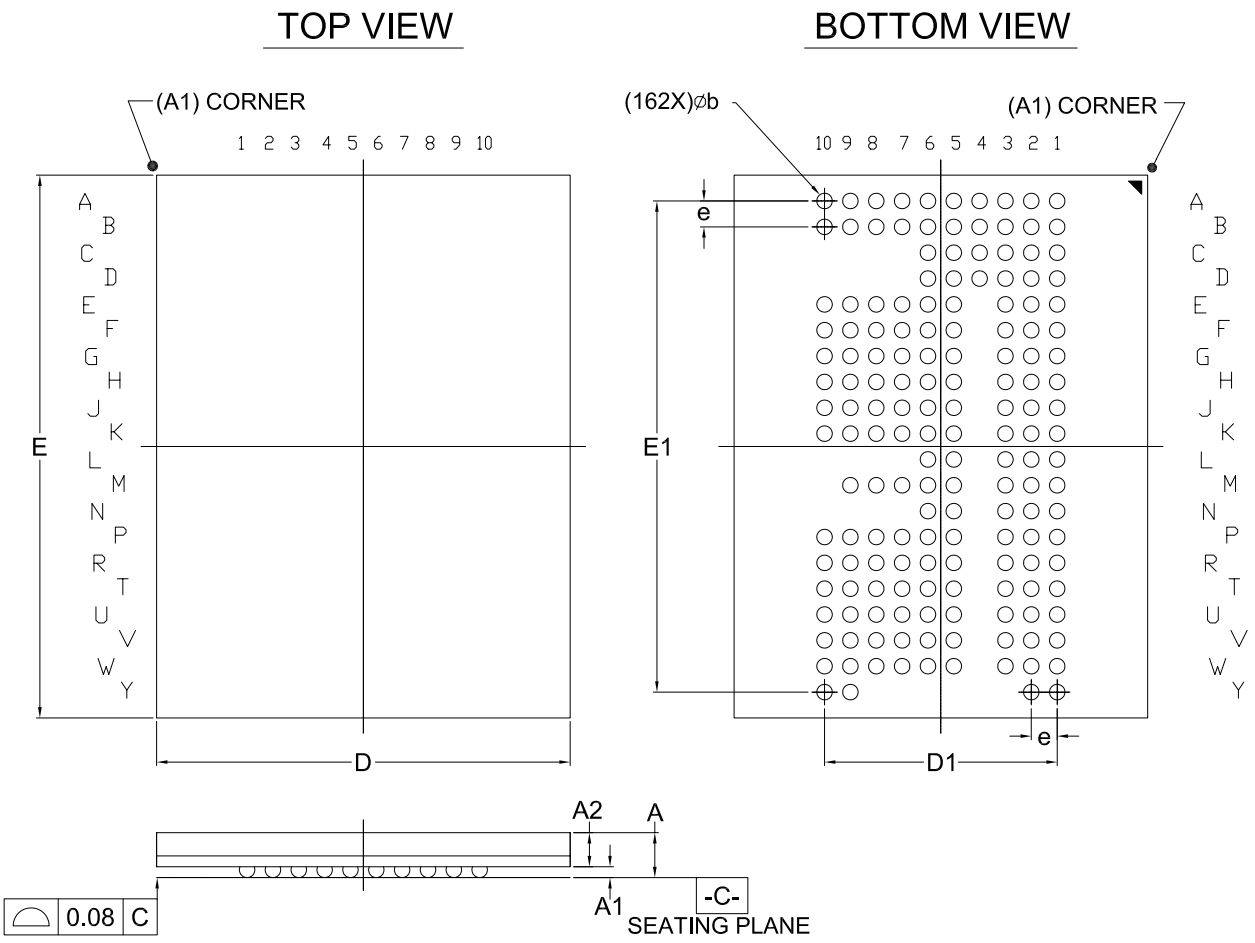
## 6. PIN DESCRIPTION

| SYMBOL | DESCRIPTION | 4Gb (512Mb x8) NAND Flash | 2Gb (64Mb x32) LPDDR2-S4B |
|---|---|---|---|
| I/O0 ~ I/OX | Data Input / Output | V | |
| CLE | Command Latch Enable | V | |
| ALE | Address Latch Enable | V | |
| CE# | Chip Enable | V | |
| WE# | Write Enable | V | |
| RE# | Read Enable | V | |
| WP# | Write Protect | V | |
| R/B# | Ready / Busy Out | V | |
| VCC | Supply Voltage | V | |
| VSSm | Ground | V | |
| PT | Chip Protection Enable | V | |
| /CS | Chip Select | | V |
| CK, /CK | Differential Clocks | | V |
| CKE | Clock Enable | | V |
| CA0 ~ CA9 | Command / Address | | V |
| DQ0 ~ DQ31 | Data I/O | | V |
| DM0 ~ DM3 | Input Data Mask | | V |
| DQS0 ~ DQS3 | Differential Data Strobe (rising edge) | | V |
| /DQS0 ~ /DQS3 | Differential Data Strobe (falling edge) | | V |
| ZQ | Drive Strength Calibration | | V |
| VREF(DQ) | Reference Voltage | | V |
| VREF(CA) | Reference Voltage | | V |
| VDD1 | Core Power Supply | | V |
| VDD2 | Core Power Supply | | V |
| VSS, VSSCA, VSSQ | Ground | | V |
| VDDQ | I/O Power Supply | | V |
| VDDCA | CA Power Supply | | V |
| NC | No Connection | | V |
| DNU * | Do Not Use | V | V |

* : DNU pin of NAND must keep floating.

## 7. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 162BALL(8X10.5X1.0MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | -- | 0.16 | 0.61 | 0.25 | 7.90 | --- | 10.40 | --- | --- |
| | Nom. | -- | 0.21 | --- | 0.30 | 8.00 | 4.5 | 10.50 | 9.5 | 0.50 |
| | Max. | 1.00 | 0.26 | --- | 0.35 | 8.10 | --- | 10.60 | --- | --- |
| Inch | Min. | --- | 0.006 | 0.024 | 0.010 | 0.311 | --- | 0.409 | --- | --- |
| | Nom. | --- | 0.008 | --- | 0.012 | 0.315 | 0.177 | 0.413 | 0.374 | 0.020 |
| | Max. | 0.039 | 0.010 | --- | 0.014 | 0.319 | --- | 0.417 | --- | --- |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4270 | 0 | | | | |

## 8. REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1. Modified PART NAME DESCRIPTION | P4 | JUL/21/2014 |
| | 2. Removed the title "Advanced information" | All | |
| | 3. Revised Bus information, Page program and Block erase time | P2 | |
| | 4. Revised block diagram (NAND) | P3 | |
| 1.1 | 1. Added VDD definition | P2 | OCT/24/2014 |
| | 2. Added two part numbers: MX63U2GC1GCAXMI00 and MX63U4GC2GBAXMI00 | P2,4,5 | |

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