8G-byte e•MMC™ Memory

MX52LM08C31

J Grade

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1. FEATURES

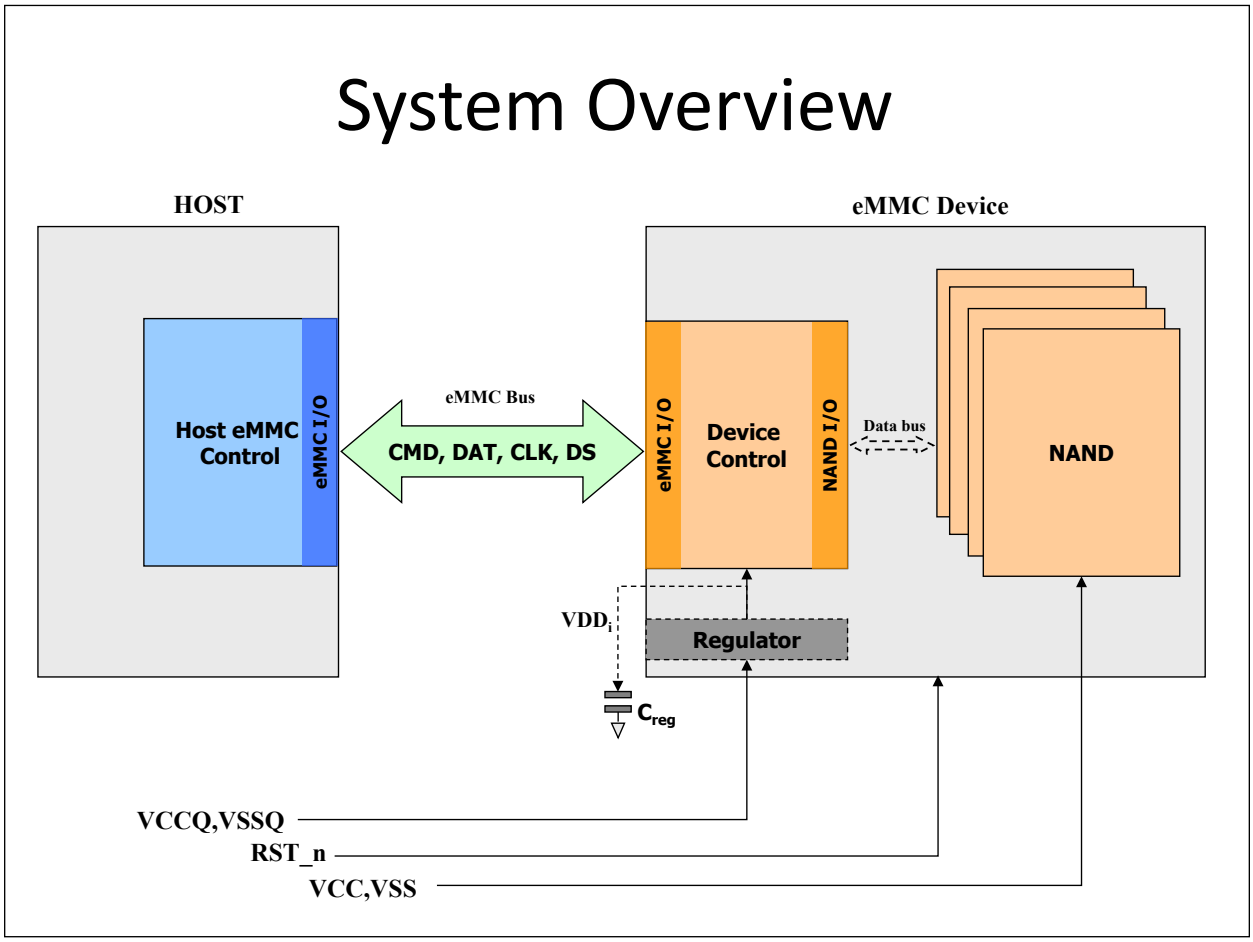
- *e*•MMC™ Ver. 5.1 compatible. Detailed description is referenced by JEDEC Standard
- Supports features of e•MMC™ 5.1 which are defined in JEDEC Standard
  - Packed command, Cache, Discard, Sanitize, Power Off Notification, Data Tag, Partition types, Context ID, Real Time Clock, Dynamic Device Capacity, HS200/400
  - Non-supported Features : Large Sector Size (4KB)
- Host was recommended support "Power Off Notification." This allows the device to better prepare itself for being powered off.
- Additional features of *e*•MMC™ 5.1**:** Field Firmware Update, Device Health Report, Sleep Notification, Production State Awareness
- Fully backward compatible with previous MultiMediaCard system specification
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency: 0 to 200MHz
- MMC I/F Boot Frequency: 0 to 52MHz
- **Operating Voltage Range:**
  - VCC: 2.7 to 3.6V
  - VCCQ: 2.7 to 3.6V/1.7 to 1.95V
- **Operating/Storage Temperature Range**: the 14th letter of Part Name stands for below
  - J : -40°C to +105°C / -40°C to +105°C
- **Package:** 153-FBGA (11.5mmx13mm)

  All packaged devices are RoHS Compliant and Halogen-free.

2. GENERAL DESCRIPTIONS

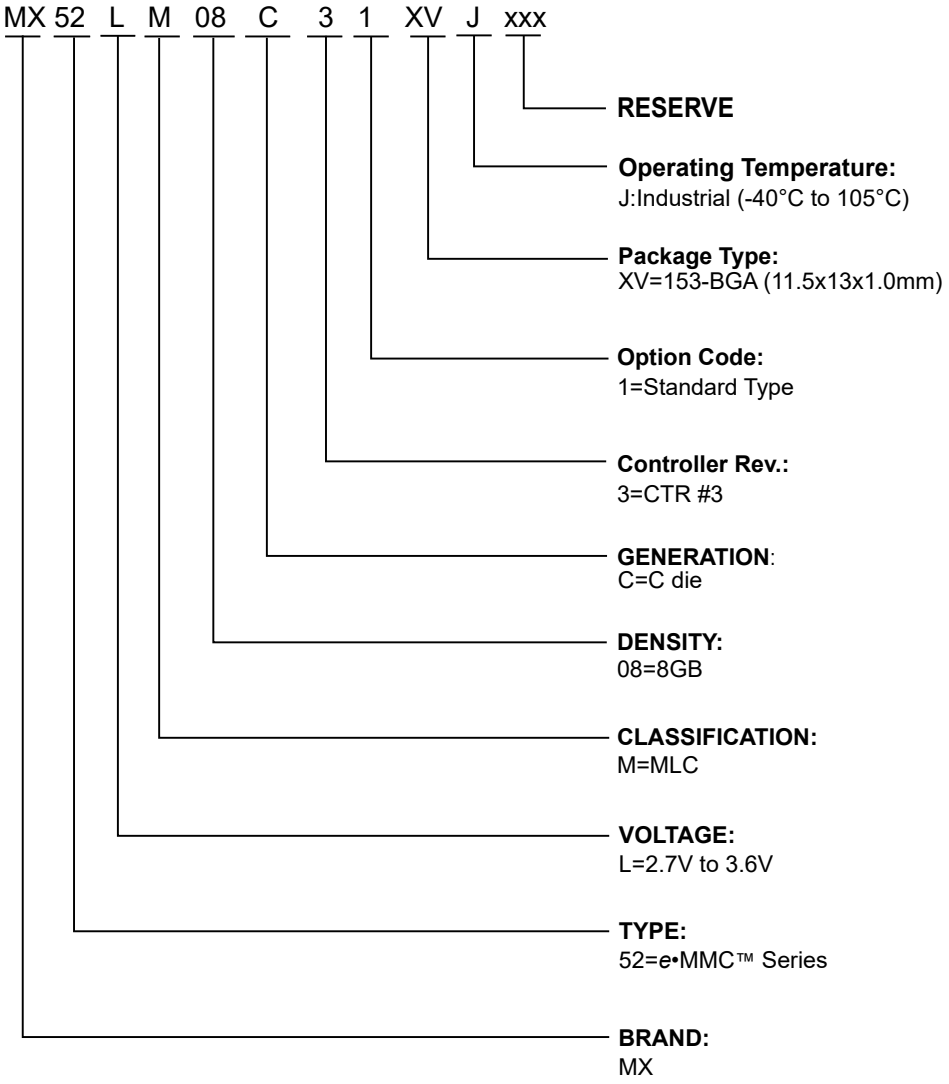
Macronix *e*•MMC™ product family is an embedded flash memory which is fully compatible with the JEDEC *e*•MMC™ 5.1 standard. It is a managed flash solution for variety of electronic devices such as smartphones, tablets, digital TVs, set-top boxes and network devices. The *e*•MMC™ product integrates the Macronix MLC NAND device and controller chip as a multi-chip module, with a standard interface protocol to the host system.

Figure 1. Logic Diagram



2-1. ORDERING INFORMATION

Part Name Description



Please refer to the individual product pages of Macronix Website or contact Macronix regional Sales for the latest Full Part Numbers and available form factor selection.

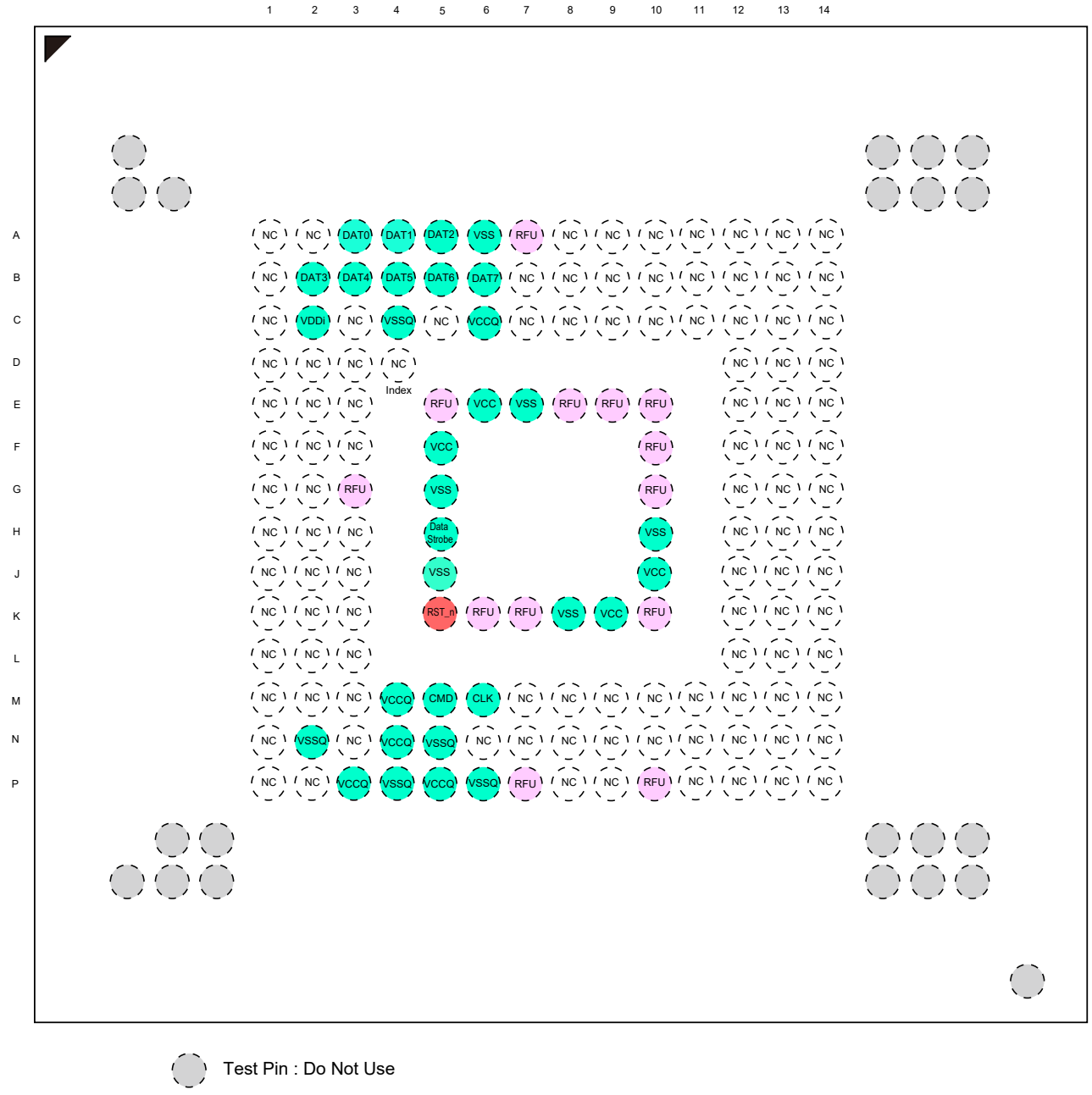
Firmware version [PRV] should be informed along with EPN when ordering.

Part Number	Density	NAND Flash Type	VCC Range	Package	Temperature Grade
MX52LM08C31XVJ	8GB	64Gb x 1	2.7V to 3.6V	153-BGA(11.5x13)	Industrial (-40°C to 105°C)

3. PIN CONFIGURATIONS

3-1. PIN DESCRIPTIONS

The *e*•MMC™ specifications cover the behavior of the interface and the device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces are not fully specified.



Top View: Ball down

Table 1. Pin Descriptions

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	VSS	N4	VCCQ
A4	DAT1	C4	VSSQ	J10	VCC	N5	VSSQ
A5	DAT2	C6	VCCQ	K5	RST_n	P3	VCCQ
A6	VSS	E6	VCC	K8	VSS	P4	VSSQ
B2	DAT3	E7	VSS	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	VSSQ
B4	DAT5	G5	VSS	M5	CMD		
B5	DAT6	H5	Data Strobe	M6	CLK		
B6	DAT7	H10	VSS	N2	VSSQ		

Notes:

1. ***NC:*** *NOT Connected, shall be connected to ground or left floating.*
2. ***RFU:*** *Reserved for Future Use, shall be left floating for future use.*
3. ***VDDi:*** *Internal power pin stabilizes regular output for controller core logics.*

DEVICE OVERVIEW

The *e*•MMC™ device transfers data via a configurable number of data bus signals. The communication signals are:

CLK

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

Data Strobe

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge.

CMD

This signal is a bidirectional command channel used for device initialization and transfer of command. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Command are sent from the *e*•MMC™ host controller to the *e*•MMC™ device and responses are sent from the device to the host.

DAT0-DAT7

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the *e*•MMC™ host controller. The *e*•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the device disconnects the internal pull-ups of lines DAT1–DAT7.

The signals on the *e*•MMC™ interface are described in Table below:

Table 2. *e*•MMC™ Interface

Name	Type	Descriptions
CLK	I	Clock
DS	O/PP	Data Strobe
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware Reset
VCC	S	Supply Voltage for Core
VCCQ	S	Supply Voltage for I/O
VSS	S	Supply Voltage Ground for Core
VSSQ	S	Supply Voltage Ground for I/O
VDDi	S	Internal power pin, it must be added at least 0.1uF capacitor. (1uF is highly recommended) on the system board
Note 1. *I=Input; O=Output; PP=Push-pull; OD=Open-drain; NC=Not connected (or Logical High); S=Power supply*		

Each device has a set of information registers (See the table below):

Table 3. Device Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, and individual number for identification	Mandatory
RCA	2	Relative Device Address, is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operaton Condition Register. Used by a special broadcast command to identify the voltage type of the device	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry that puts the device into a defined state after the power-on.
- A reset signal
- Sending a special command

4. FUNCTIONAL DESCRIPTION

4-1. *e*•MMC™ Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

Five operation modes are defined for the *e*•MMC™ system (hosts and devices):

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

4-2. Boot Operation Mode

In boot operation mode, the master (*e*•MMC™ host) can read boot data from the slave (*e*•MMC™ device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B51.

4-3. Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only.

For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B51.

4-4. Data Transfer Mode

When the Device is in Stand-by mode, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B51.

4-4-1. Data Read

The DAT0-DAT7 bus line levels are high when no data is transmitted. For more details, refer to section 6.6.7 of the JEDEC Standard Specification No.JESD84-B51.

4-4-2. Data Write

The data transfer format of write operation is similar to the data read. For more details, refer to section 6.6.8 of the JEDEC Standard Specification No.JESD84-B51.

4-4-3. Erase

In addition to the implicit erase executed by the Device as part of the write operation, provides a host explicit erase function. For more details, refer to section 6.6.9 of the JEDEC Standard Specification No.JESD84-B51.

4-4-4. TRIM

The TRIM operation is similar to the default erase operation described (See Section 6.6.12 of JESD84-B51). The TRIM function applies the erase operation to write blocks instead of erase groups. The TRIM function allows the host to identify data that is no longer required so that the Device can erase the data if necessary during background erase events. For more details, refer to section 6.6.10 of the JEDEC Standard Specification No.JESD84-B51.

4-4-5. Sanitize

The Sanitize operation is a feature, in addition to TRIM and Erase that is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. For more details, refer to section 6.6.11 of the JEDEC Standard Specification No.JESD84-B51.

4-4-6. Discard

The Discard is similar operation to TRIM. The Discard function allows the host to identify data that is no longer required so that the device can erase the data if necessary during background erase events. For more details, refer to section 6.6.12 of the JEDEC Standard Specification No.JESD84-B51.

4-4-7. Write Protect Management

In order to allow the host to protect data against erase or write, the *e*•MMC™ shall support two levels of write protect command. For more details, refer to section 6.6.15 of the JEDEC Standard Specification No.JESD84-B51.

4-4-8. Application-Specific Command

The *e*•MMC™ system is designed to provide a standard interface for a variety applications types. In this environment, it is anticipated that there will be a need for specific customers/applications features. For more details, refer to section 6.6.20 of the JEDEC Standard Specification No.JESD84-B51.

4-4-9. Sleep (CMD5)

A Device may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. For more details, refer to section 6.6.21 of the JEDEC Standard Specification No.JESD84-B51.

4-4-10. Replay Protected Memory Block

A signed access to a Replay Protected Memory Block is provided. This function provides means for the system to store data to the specific memory area in an authenticated and replay protected manner. For more details, refer to section 6.6.22 of the JEDEC Standard Specification No.JESD84- B51.

4-4-11. Dual Data Rate Mode Selection

After the host verifies that the Device complies with version 4.4, or higher, of this standard, and supports dual data rate mode, it may enable the dual data rate data transfer mode in the Device. For more details, refer to section 6.6.23 of the JEDEC Standard Specification No.JESD84-B51.

4-4-12. Dual Data Rate Mode Operation

After the Device has been enabled for dual data rate operating mode, the block length parameter of CMD17, CMD18, CMD24, CMD25 and CMD56 automatically default to 512 bytes and cannot be changed by CMD16 (SET_BLOCKLEN) command which becomes illegal in this mode. For more details, refer to section 6.6.24 of the JEDEC Standard Specification No.JESD84-B51.

4-4-13. Background Operations

Devices have various maintenance operations need to perform internally. In order to reduce latencies during time critical operations like read and write, it is better to execute maintenance operations in other times – when the host is not being serviced. For more details, refer to section 6.6.25 of the JEDEC Standard Specification No.JESD84-B51.

4-4-14. High Priority Interrupt (HPI)

In some scenarios, different types of data on the device may have different priorities for the host. For example, writing operation may be time consuming and therefore there might be a need to suppress the writing to allow demand paging requests in order to launch a process when requested by the user. For more details, refer to section 6.6.26 of the JEDEC Standard Specification No.JESD84-B51.

4-4-15. Context Management

To better differentiate between large sequential operations and small random operations, and to improve multitasking support, contexts can be associated with groups of read or write command. Associating a group of command with a single context allows the device to optimize handling of the data. For more details, refer to section 6.6.27 of the JEDEC Standard Specification No.JESD84-B51.

4-4-16. Data Tag Mechanism

The mechanism permits the device to receive from the host information about specific data types(for instance file system metadata, time-stamps, configuration parameters, etc.). The information is conveyed before a write multiple blocks operation at well-defined addresses. By receiving this information the device can improve the access rate during the following read and update operations and offer a more reliable and robust storage. For more details, refer to section 6.6.28 of the JEDEC Standard Specification No.JESD84-B51.

4-4-17. Packed Command

Read and write command can be packed in groups of command (either all read or all write) that transfer the data for all command in the group in one transfer on the bus, to reduce overheads. For more details, refer to section 6.6.29 of the JEDEC Standard Specification No.JESD84-B51.

4-4-18. Real Time Clock Information

Providing real time clock information to the device may be useful for internal maintenance operations. Host may provide either absolute time (based on UTC) if available, or relative time. This feature provides a mechanism for the host to update both real time clock and relative time updates (see CMD49). For more details, refer to section 6.6.35 of the JEDEC Standard Specification No.JESD84-B51.

4-4-19. Power Off Notification

The host is recommended notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. For more details, refer to section 6.6.36 of the JEDEC Standard Specification No.JESD84-B51.

4-5. Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to Pre-idle state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

4-6. Clock Control

The *e*•MMC™ bus clock signal can be used by the host to put the Device into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For more details, refer to section 6.7 of the JEDEC Standard Specification No.JESD84-B51.

4-7. Error Conditions

Refer to section 6.8 of the JEDEC Standard Specification No.JESD84-B51.

4-8. Minimum Performance

Refer to section 6.9 of the JEDEC Standard Specification No.JESD84-B51.

4-9. Command

Refer to section 6.10 of the JEDEC Standard Specification No.JESD84-B51.

4-10. Device State Transition Table

Refer to section 6.11 of the JEDEC Standard Specification No.JESD84-B51.

4-11. Responses

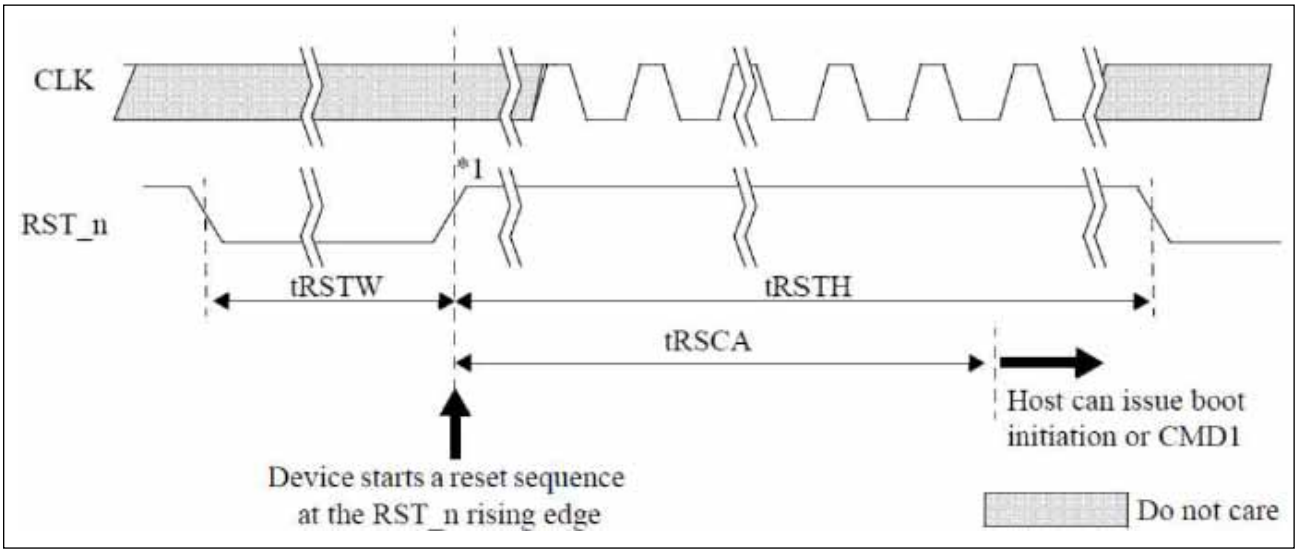
Refer to section 6.12 of the JEDEC Standard Specification No.JESD84-B51.

4-12. Timings

Refer to section 6.15 of the JEDEC Standard Specification No.JESD84-B51.

4-13. H/W Reset Operation

Figure 1. H/W Reset Waveform



Note 1: *Device will detect the rising edge of RST_n signal to trigger internal reset sequence.*

Table 4. H/W Reset Timing Parameters

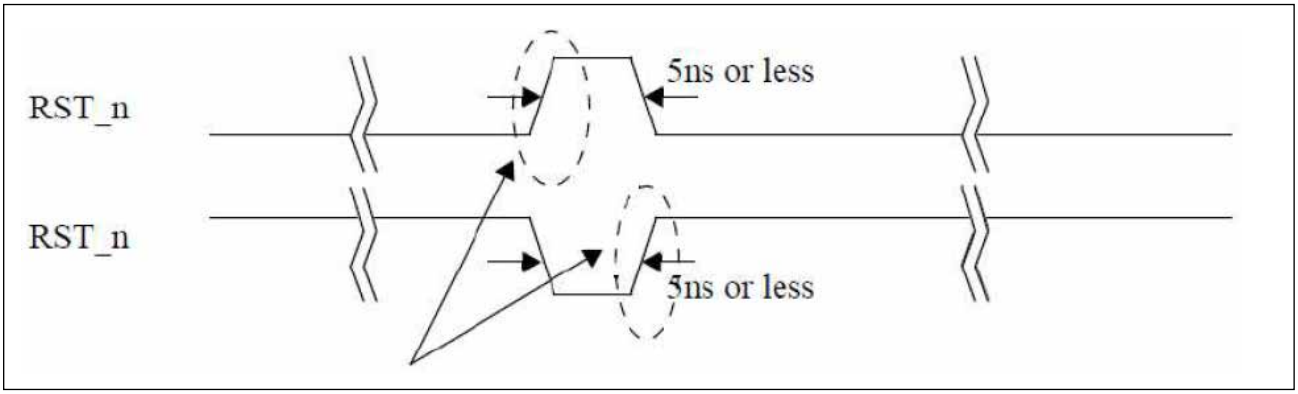
Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1		[us]
tRSCA	RST_n to Command time	200[1]		[us]
tRSTH	RST_n high period (interval time)	1		[us]

***Note 1**: 74 cycles of clock signal are required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA*

4-14. Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity.

Figure 2. Noise Filtering Timing for H/W Reset



Device must not detect these rising edge.

Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

4-15. Field Firmware Update(FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the *e*•MMC™ device and, following a successful download, instructs the *e*•MMC™ device to install the new downloaded firmware into the device.

For more details, refer to section 6.6.18 of the JEDEC Standard Specification No.JESD84-B51.

4-16. Device Life time

4-16-1. DEVICE LIFE TIME SET TYP B

This field provides an estimated indication about the device life time which is reflected by the averaged wear out of memory of Type B relative to its maximum estimated device life.

Value	Description
0x00	Not defined
0x01	0% - 10% device life time used
0x02	10% -20% device life time used
0x03	20% -30% device life time used
0x04	30% - 40% device life time used
0x05	40% - 50% device life time used
0x06	50% - 60% device life time used
0x07	60% - 70% device life time used
0x08	70% - 80% device life time used
0x09	80% - 90% device life time used
0x0A	90% - 100% device life time used
0x0B	Exceeded its maximum estimated device life time
Others	Reserved

4-16-2. DEVICE LIFE TIME SET TYP A

This field provides an estimated indication about the device life time which is reflected by the averaged wear out of memory of Type A relative to its maximum estimated device life time

Value	Description
0x00	Not defined
0x01	0% - 10% device life time used
0x02	10% -20% device life time used
0x03	20% -30% device life time used
0x04	30% - 40% device life time used
0x05	40% - 50% device life time used
0x06	50% - 60% device life time used
0x07	60% - 70% device life time used
0x08	70% - 80% device life time used
0x09	80% - 90% device life time used
0x0A	90% - 100% device life time used
0x0B	Exceeded its maximum estimated device life time
Others	Reserved

4-17. Pre EOL Information

This field provides indication about device life time reflected by average reserved blocks.

Table 5. Pre EOL Infor. Value

Value	Pre-EOL Info.	Description
0x00	Not Defined	
0x01	Normal	Normal
0x02	Warning	Consumed 80% of reserved block
0x03	Urgent	
0x04 ~ 0xFF	Reserved	

4-18. Optimal Size

4-18-1. Optimal Read Size

This field provides the minimum optimal (for the device) read unit size for the different partitions.

Table 6. Optimal Read Size Value

Value	Optimal Read Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB

0xFF	4KB x 255 = 1020KB

4-18-2. Optimal Write Size

This field provides the minimum optimal (for the device) write unit size for the different partitions. “Optimal” relates to the minimum wear-out done by the device. The *e*•MMC follows logical address of write command to assign user data area (i.e., MLC mode) or enhanced data area (i.e., SLC mode). For more details, refer to section 6.2 of the JEDEC Standard Specification No.JESD84-B51.

Table 7. Optimal Write Size Value

Value	Optimal Write Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB

0xFF	4KB x 255 = 1020KB

4-18-3. Optimal Trim Unit Size

This field provides the minimum optimal (for the device) trim unit size for the different partitions. “Optimal” relates to the minimum wearout done by the device.

Table 8. Optimal Trim Size Value

Value	Optimal Trim Unit Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB
0x03	4KB x 4 = 16KB

0x15	4KB x 2^20 = 4GB
Reserved	

4-19. Production State Awareness

e•MMC™ device utilizes the information of whether it is in production environment and operate differently than it operates in the field.

For example, content which is loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The *e*•MMC™ device uses “special” internal operations for loading content prior to device soldering which would reduce production failures and use “regular” operations post-soldering.

Once the eMMC device needs to restart production during PRE_SOLDERING_WRITES, please set the PRODUCTION_STATE_AWARENESS to NORMAL and then reset the power cycle of this eMMC device. It will be ready to restart production after reset or power cycle.

For more details, refer to section 6.6.17 of the JEDEC Standard Specification No.JESD84-B51.

Strongly recommend to follow Production State Awareness Flow when the pre-soldering data loading is needed.

5. Register Value

5-1. OCR Register Information

Table 9. OCR Register

OCR bit	VDD Voltage Window	Value
[31]	Card power up status bit (busy)[Note 1]	
[30:29]	Access Mode	08GB: 10b
[28:24]	Reserved	0 0000b
[23:15]	2.7-3.6	1 1111 1111b
[14:8]	2.0-2.6	000 0000b
[7]	1.70-1.95	1b
[6:0]	Reserved	000 0000b

Note: *This bit is set to LOW if the Device has not finished the power.*

5-2. CID Register Information

Table 10. CID Register

CID Slice	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	11000010b
[119:114]	Bank Index Number	BIN	6	000000b
[113:112]	Device/BGA	CBX	2	01b
[111:104]	OEM/Application ID	OID	8	0x01
[103:56]	Product name	PNM	48	0x4D 30 38 43 33 31 (M08C31)
[55:48]	Product revision	PRV	8	Firmware revision
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	See-JEDEC Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always ‘1’	-	1	1b

5-3. CSD Register Information

Table 11. CSD Register

CSD-Slice	Name	Field	Width	Cell Type	Value
[127:126]	CSD structure	CSD_STRUCTURE	2	R	0x3
[125:122]	System specification version	SPEC_VERS	4	R	0x4
[121:120]	Reserved	-	2	R	0x0
[119:112]	Data read access-time 1	TAAC	8	R	0xFF
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0xFF
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32
[95:84]	Device command classes	CCC	12	R	0x1F5
[83:80]	Max. read data block length	READ_BL_LEN	4	R	08GB: 0x9
[79:79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0x0
[78:78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0x0
[77:77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0x0
[76:76]	DSR implemented	DSR_IMP	1	R	0x0
[75:74]	Reserved	--	2	R	0x0
[73:62]	Device size	C_SIZE	12	R	08GB: 0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	0x3
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	0x7
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	0x3
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	0x7
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	08GB: 0x0F
[31:31]	Write protect group enable	WP_GRP_ENABLE	1	R	0x1
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	0x0
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x2
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9
[21:21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0x0
[20:17]	Reserved	-	4	R	0x0
[16:16]	Content protection application	CONTENT_PROT_APP	1	R	0x0
[15:15]	File format group	FILE_FORMAT_GRP	1	R/W	0x0
[14:14]	Copy flag (OTP)	COPY	1	R/W	0x0
[13:13]	Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0x0
[12:12]	Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0x0
[11:10]	File format	FILE_FORMAT	2	R/W	0x0
[9:8]	ECC code	ECC	2	R/W/E	0x0
[7:1]	CRC	CRC	7	R/W/E	CRC
[0]	Not used, always ‘1’	--	1	--	0x1

5-4. Extended CSD Register Information

Table 12. Extended CSD Register

CSD-Slice	Name	Field	Size (Bytes)	Cell Type	Value
[511:506]	Reserved	-	6	-	0x00
[505]	Extended Security Commands Error	EXT_SECURITY_ERR	1	R	0x00
[504]	Supported Command Sets	S_CMD_SET	1	R	0x01
[503]	HPI features	HPI_FEATURES	1	R	0x01
[502]	Background operations support	BKOPS_SUPPORT	1	R	0x01
[501]	Max_packed read commands	MAX_PACKED_READS	1	R	0x20
[500]	Max_packed write commands	MAX_PACKED_WRITES	1	R	0x20
[499]	Data Tag Support	DATA_TAG_SUPPORT	1	R	0x01
[498]	Tag Unit Size	TAG_UNIT_SIZE	1	R	0x03
[497]	Tag Resource Size	TAG_RES_SIZE	1	R	0x00
[496]	Context management capabilities	CONTEXT_CAPABILITIES	1	R	0x05
[495]	Large Unit size	LARGE_UNIT_SIZE_M1	1	R	0x0B
[494]	Extended partitions attribute support	EXT_SUPPORT	1	R	0x03
[493]	Supported modes	SUPPORTED_MODES	1	R	0x01
[492]	FFU features	FFU_FEATURES	1	R	0x00
[491]	Operation codes timeout	OPERATION_CODES_TIMEOUT	1	R	0x00
[490:487]	FFU Argument	FFU_ARG	4	R	0x6C6F5341
[486]	Barrier Support	BARRIER_SUPPORT	1	R	0x00
[485:309]	Reserved	-	177	-	0x00
[308]	CMD Queuing Support	CMDQ_SUPPORT	1	R	0x00
[307]	CMD Queuing Depth	CMDQ_DEPTH	1	R	0x1F
[306]	Reserved	-	1	-	0x00
[305:302]	Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	0x00
[301:270]	Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	0x00
[269]	Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	0x01
[268]	Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	0x01
[267]	Pre EOL information	PRE_EOL_INFO	1	R	0x00
[266]	Optimal read size	OPTIMAL_READ_SIZE	1	R	0x08
[265]	Optimal write size	OPTIMAL_WRITE_SIZE	1	R	0x08
[264]	Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	0x04
[263:262]	Device version	DEVICE_VERSION	2	R	0x011D
[261:254]	Firmware version	FIRMWARE_VERSION	8	R	0x00
[253]	Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	0x00
[252:249]	Cache size	CACHE_SIZE	4	R	0x00000400
[248]	Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	0x32
[247]	Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	0x64
[246]	Background operations status	BKOPS_STATUS	1	R	0x00
[245:242]	Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	0x00
[241]	1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	0x1E
[240]	Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	0x01
[239]	Power class for 52MHz, DDR @ 3.6V	PWR_CL_DDR_52_360	1	R	0x00
[238]	Power class for 52MHz, DDR @ 1.95V	PWR_CL_DDR_52_195	1	R	0x00
[237]	Power class for 200MHz @ 3.6V	PWR_CL_200_360	1	R	0x00

CSD-Slice	Name	Field	Size (Bytes)	Cell Type	Value
[236]	Power class for 200MHz @ 1.95V	PWR_CL_200_195	1	R	0x00
[235]	Minimum Write Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0x00
[234]	Minimum Read Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	0x00
[233]	Reserved	-	1	-	0x00
[232]	TRIM Multiplier	TRIM_MULT	1	R	0x02
[231]	Secure Feature support	SEC_FEATURE_SUPPORT	1	R	0x55
[230]	Secure Erase Multiplier	SEC_ERASE_MULT	1	R	0xC0
[229]	Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	0xC0
[228]	Boot information	BOOT_INFO	1	R	0x07
[227]	Reserved	-	1	R	0x00
[226]	Boot partition size	BOOT_SIZE_MULT	1	R	08GB: 0x20
[225]	Access size	ACC_SIZE	1	R	0x07
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x01
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x05
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x01
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	08GB: 0x10
[220]	Sleep current (VCC)	S_C_VCC	1	R	0x07
[219]	Sleep current (VCCQ)	S_C_VCCQ	1	R	0x07
[218]	Production state awareness timeout	PRODUCTION_STATE _AWARENESS_TIMEOUT	1	R	0x0D
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x13
[216]	Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	0x07
[215:212]	Sector Count	SEC_COUNT	4	R	08GB: 0x00E90000
[211]	Secure Write Protect Information	SECURE_WP_INFO	1	R	0x00
[210]	Minimum Write Performance for 8bit@52MHz	MIN_PERF_W_8_52	1	R	0x00
[209]	Minimum Read Performance 8bit@ 52MHz	MIN_PERF_R_8_52	1	R	0x00
[208]	Minimum Write Performance for 8bit@26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x00
[207]	Minimum Read Performance for 8 bit@26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x00
[206]	Minimum Write Performance for 4bit@26MHz	MIN_PERF_W_4_26	1	R	0x00
[205]	Minimum Read Performance for 4bit@26MHz	MIN_PERF_R_4_26	1	R	0x00
[204]	Reserved	-	1	-	0x00
[203]	Power class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	0x00
[202]	Power class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	0x00
[201]	Power class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	0x00
[200]	Power class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	0x00
[199]	Partition switching timing	PARTITION_SWITCH_TIME	1	R	0x01
[198]	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	0x19

CSD-Slice	Name	Field	Size (Bytes)	Cell Type	Value
[197]	I/O Driver Strength	DRIVER_STRENGTH	1	R	0x1F
[196]	Device Type	DEVICE_TYPE	1	R	0x57
[195]	Reserved	-	1	-	0x00
[194]	CSD structure version	CSD_STRUCTURE	1	R	0x02
[193]	Reserved	-	1	-	0x00
[192]	Extended CSD revision	EXT_CSD_REV	1	R	0x08
[191]	Command Set	CMD_SET	1	R/W/E_P	0x00
[190]	Reserved	-	1	-	0x00
[189]	Command set revision	CMD_SET_REV	1	R	0x00
[188]	Reserved	-	1	-	0x00
[187]	Power class[1]	POWER_CLASS	1	R/W/E_P	0x00
[186]	Reserved	-	1	-	0x00
[185]	High-speed interface timing	HS_TIMING	1	R/W/E_P	0x00 note: base on eMMC Host
[184]	Strobe Support	STROBE_SUPPORT	1	R	0x01
[183]	Bus width mode	BUS_WIDTH	1	W/E_P	0x00 note: base on eMMC Host
[182]	Reserved	-	1	-	0x00
[181]	Erased memory content	ERASED_MEM_CONT	1	R	0x00
[180]	Reserved	-	1	-	0x00
[179]	Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0x00
[178]	Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0x00
[177]	Boot bus width	BOOT_BUS_WIDTH	1	R/W/E	0x00
[176]	Reserved	-	1	-	0x00
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0x00
[174]	Boot write protection status registers	BOOT_WP_STATUS	1	R	0x00
[173]	Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	0x00
[172]	Reserved	-	1	-	0x00
[171]	User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0x00
[170]	Reserved	-	1	-	0x00
[169]	FW configuration	FW_CONFIG	1	R/W	0x00
[168]	RPMB Size	RPMB_SIZE_MULT	1	R	08GB: 0x20
[167]	Write reliability setting register	WR_REL_SET	1	R/W	0x1F
[166]	Write reliability parameter register	WR_REL_PARAM	1	R	0x15
[165]	Start Sanitize operation	SANITIZE_START	1	W/E_P	0x00
[164]	Manually start background operations	BKOPS_START	1	W/E_P	0x00
[163]	Enable background operations handshake	BKOPS_EN	1	R/W/E	0x02
[162]	H/W reset function	RST_n_FUNCTION	1	R/W	0x00
[161]	HPI management	HPI_MGMT	1	R/W/E_P	0x00
[160]	Partitioning Support	PARTITIONING_ SUPPORT	1	R	0x07
[159:157]	Max Enhanced Area Size[2]	MAX_ENH_SIZE_MULT	3	R	08GB: 0x0001D2
[156]	Partitions attribute	PARTITIONS_ ATTRIBUTE	1	R/W	0x00

CSD-Slice	Name	Field	Size (Bytes)	Cell Type	Value
[155]	Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	0x00
[154:143]	General Purpose Partition Size[3]	GP_SIZE_MULT	12	R/W	0x00
[142:140]	Enhanced User Data Area Size[4]	ENH_SIZE_MULT	3	R/W	0x00
[139:136]	Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0x00
[135]	Reserved	-	1	-	0x00
[134]	Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0x00
[133]	Production state awareness[5]	PRODUCTION_STATE _AWARENESS	1	R/W/E	0x00
[132]	Package Case Temperature is controlled[1]	TCASE_SUPPORT	1	W/E_P	0x00
[131]	Periodic Wake-up[1]	PERIODIC_WAKEUP	1	R/W/E	0x00
[130]	Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	R	0x01
[129:128]	Reserved	-	2	-	0x00
[127:64]	Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	-	-
[63]	Native sector size	NATIVE_SECTOR_SIZE	1	R	0x00
[62]	Sector size emulation	USE_NATIVE_SECTOR	1	R/W	0x00
[61]	Sector size	DATA_SECTOR_SIZE	1	R	0x00
[60]	1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	0x00
[59]	Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	0x00
[58]	Number of addressed group to be Released	DYNCAP_NEEDED	1	R	0x00
[57:56]	Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	0x00
[55:54]	Exception events status	EXCEPTION_EVENTS_STATUS	2	R	0x00
[53:52]	Extended partitions attribute[1]	EXT_PARTITIONS_ATTRIBUTE	2	R/W	0x00
[51:37]	Context configuration	CONTEXT_CONF	15	R/W/E_P	0x00
[36]	Packed command status	PACKED_COMMAND_STATUS	1	R	0x00
[35]	Packed command failure index	PACKED_FAILURE_INDEX	1	R	0x00
[34]	Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	0x00
[33]	Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	0x00
[32]	Flushing of the cache	FLUSH_CACHE	1	W/E_P	0x00
[31]	Reserved	-	1	-	0x00
[30]	Mode config	MODE_CONFIG	1	R/W/E_P	0x00
[29]	Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	0x00
[28:27]	Reserved	-	2	R	0x00
[26]	FFU status	FFU_STATUS	1	R	0x00
[25:22]	Pre loading data size[5]	PRE_LOADING_DATA_SIZE	4	R/W/E_P	0x00
[21:18]	Max pre loading data size	MAX_PRE_LOADING_DATA_ SIZE	4	R	08GB: 0x00747FFF
[17]	Product state awareness enablement[5]	PRODUCT_STATE _AWARENESS_ENABLEMENT	1	R/W/E&R	0x02
[16]	Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	0x19
[15]	Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	0x00
[14:0]	Reserved	-	15	-	0x00

Notes:

1. *Although these fields can be re-written by host, Macronix e•MMC™ does not support.*
2. *Max Enhanced Area Size (MAX_ENH_SIZE_MULT [159:157]) has to be calculated by following formula.*

Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes

$$\sum_{i=1}^{4} \text{Enhanced general partition size(i)} + \text{Enhanced user data area} \leq \text{Max enhanced area}$$

3. *General Purpose Partition Size (GP_SIZE_MULT_GP0 - GP_SIZE_MULT_GP3 [154:143]) has to be calculated by following formula.*

   General_Purpose_Partition_X Size = (GP_SIZE_MULT_X_2 x 2^{16} + GP_SIZE_MULT_X_1 x 2^{8}

   + GP_SIZE_MULT_X_0 x 2^{0}) x HC_WP_GRP_SIZE

   x HC_ERASE_GRP_SIZE x 512kBytes

4. *Enhanced User Data Area Size (ENH_SIZE_MULT [142:140]) has to be calculated by following formula.*

   Enhanced User Data Area x Size = (ENH_SIZE_MULT_2 x 2^{16} + ENH_SIZE_MULT_1 x 2^{8}

   + ENH_SIZE_MULT_0 x 2^{0}) x HC_WP_GRP_SIZE

   x HC_ERASE_GRP_SIZE x 512kBytes

5. *Pre-loading data size = PRE_LOADING_DATA_SIZE x Sector Size*

   Pre-loading data size should be multiple of 4KB and the pre-loading data should be written by multiple of 4KB chunk size, aligned with 4KB address. This is because the valid data size will be treated as 4KB when host writes data less than 4KB.

   - If the host continues to write data in Normal state (after it writes PRE_LOADING_DATA_SIZE amount of data) and before soldering, the pre-loading data might be corrupted after soldering.

   - If a power cycle is occurred during the data transfer, the amount of data written to device is not clear.

   Therefore in this case, host should erase the entire pre-loaded data and set again

   PRE_LOADING_DATA_SIZE[25:22], PRODUCTION_STATE_AWARENESS[133], and

   PRODUCT_STATE_AWARENESS_ENABLEMENT[17].

   Remarks on the value of EXT_CSD_REV[192] in EXT_CSD register:

   Linux kernel might check if the value of EXT_CSD_REV[192] is suitable for the kernel itself or not and return the initialize error when the device indicates JEDEC/MMCA V5.1 or later.

   In case of V5.1 device, EXT_CSD_REV[192] indicates 0x07.

   If the Host could not initialize the V5.1 device, Host should modify the treatment of EXT_CSD_ REV[192].

6. *Register values may vary due to firmwave migration, will be described in the register supplemental document.*

7. *BOOT_SIZE_MULT[226], RPMB_SIZE_MULT[168], SEC_COUNT[215:212] can be used to calculate the capacity of Boot partition, RPMB partition & user area, an example is shown as table below:*

Density	08GB
Boot Partition	4,096KB
RPMB Partition	4,096KB
User Area	7,634,944KB

6. ELECTRICAL CHARACTERISTICS

6-1. DC Characteristics

6-1-1. Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Table 13. Absolute Maximum Ratings

Parameters	Min	Max	Unit
VCC Supply	-0.5	4.1	V
VCCQ Supply	-0.5	4.1	V
Voltage Input	-0.5	VCCQ+0.5(≤4.1)	V

Table 14. General Parameters

Parameters	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
All Inputs			
Input Leakage Current (Before initialization sequence[1] and/or the internal pull up resistors connected)	-100	100	µA
Input Leakage Current (After initialization sequence and the internal pull up resistors disconnected)	-2	2	µA
All Outputs			
Output Leakage Current (before initialization sequence)	-100	100	µA
Output Leakage Current (after initialization sequence)	-2	2	µA

Note 1. *Initialization sequence is defined in Power-Up chapter of JEDEC/MMCA Standard*

Table 15. Supply Voltage Range

Parameters	Min	Max	Unit
VCC Supply	2.7	3.6	V
VCCQ Supply	1.7	1.95	V
	2.7	3.6	V

Note: *Once the power supply VCC or VCCQ falls below the minimum guaranteed voltage (for example, upon sudden power fail), the voltage level of VCC or VCCQ shall be kept less than 0.5 V for at least 1ms before it goes beyond 0.5 V again.*

Table 16. Active Power Consumption (RMS)

Parameters		Mode	Max		Unit
			Iccq	Icc	
08GB	Read	52MHz/SDR (1.8V)	68	9	mA
		52MHz/SDR (3.3V)	72	9	mA
		52MHz/DDR (1.8V)	72	13	mA
		52MHz/DDR (3.3V)	78	13	mA
		HS200 (1.8V)	85	26	mA
		HS400 (1.8V)	63	31	mA
	Write	52MHz/SDR (1.8V)	67	8	mA
		52MHz/SDR (3.3V)	68	8	mA
		52MHz/DDR (1.8V)	70	12	mA
		52MHz/DDR (3.3V)	71	12	mA
		HS200 (1.8V)	68	39	mA
		HS400 (1.8V)	75	42	mA

Note: *Not 100% tested.*

Table 17. Standby Power Consumption

Parameters		Typ.		Unit
		Iccq	Icc	
Standby Mode	8GB	145	69	uA

Note: *The conditions of typical values are 25˚C and VCCQ = 3.3V or 1.8V*

Table 18. Sleep Power Consumption

Parameters		Typ.		Unit
		Iccq	Icc	
Sleep Mode	8GB	140	56	uA

Note: *The conditions of typical values are 25˚C and VCCQ = 3.3V or 1.8V*

Table 19. Internal Resistance and Device Capacitance

Parameters		Symbol	Min	Max	Normal	Unit
Single device capacitance		C_{Device}	--	6	--	pF
Internal pull up resistance DAT1 – DAT7		R_{INT}	10	150	--	kΩ
RST_n Internal pull up resistance	3.3V	--	44	106	61	kΩ
	1.8V	--	95	233	147	kΩ

Figure 3. Bus Signal Levels

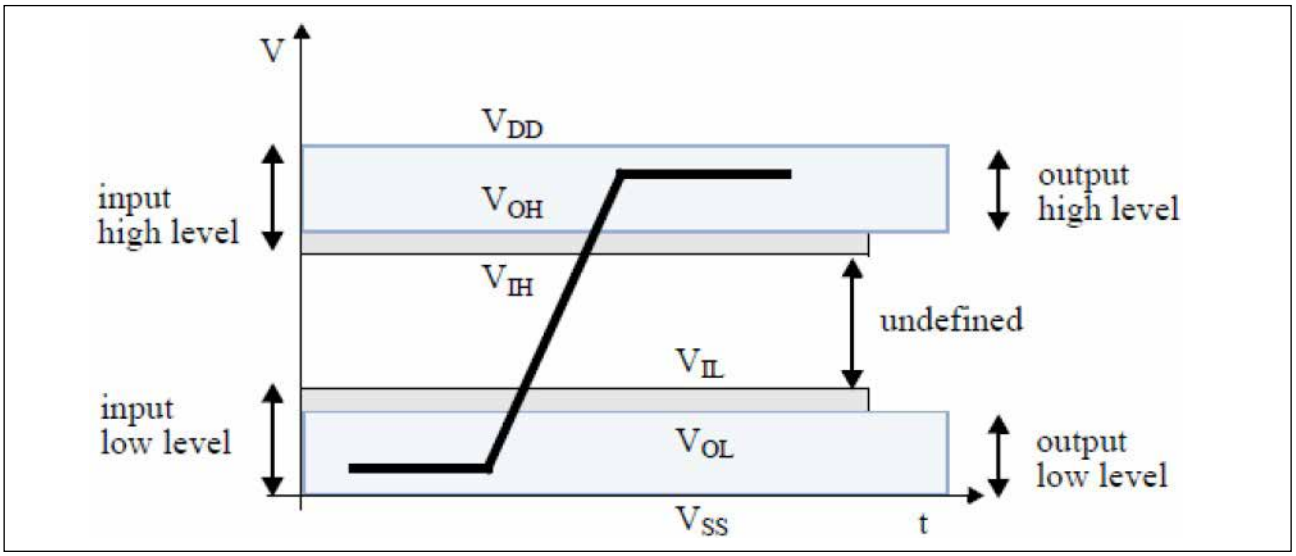


Table 20. Open-Drain Mode Bus Signal Level

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH Voltage	VOH	IOH = -100μA	VCCQ - 0.2	--	V
Output LOW Voltage	VOL	IOL = 2mA	--	0.3	V

Table 21. Push-Pull Mode Bus Signal Level (High-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	VOH	IOH = -100μA @ VDD min	0.75 * VCCQ	--	V
Output LOW voltage	VOL	IOL = 100μA @ VDD min	--	0.125 * VCCQ	V
Input HIGH voltage	VIH		0.625* VCCQ	VCCQ + 0.3	V
Input LOW voltage	VIL		VSS - 0.3	0.25 * VCCQ	V

Table 22. Push-Pull Mode Bus Signal Level (Dual-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	VOH	IOH = -2mA @ VDD min	VCCQ - 0.45	--	V
Output LOW voltage	VOL	IOL = 2mA @ VDD min	--	0.45	V
Input HIGH voltage	VIH		0.65* VCCQ	VCCQ + 0.3	V
Input LOW voltage	VIL		VSS - 0.3	0.35 * VCCQ	V

6-2. Driver Types Definition

The *e*•MMC™ device provides Dirver Type-0 as default, and four additional Driver Type options (1,2,3 &4) to support HS200 & HS400 for wider Host loads. The Host may select the most appropriate Driver Type of the Device (if supported) to achieve optimal signal integrity performance.

Driver Type-0 is targeted for transmission line, based distributed system with 50Ω nominal line impedance. Therefore, it is defined as 50Ω nominal driver.

For HS200, when tested with CL = 15pF Driver Type-0 shall meet all AC characteristics and HS200 Device output timing requirements. The test circuit defined in section 10.5.4.3 of JEDEC/MMCA Standard Ver. 5.1 is used for testing of Driver Type-0.

For HS400, when tested with the reference load defined in Figure 14, HS400 reference load figure, Driver Type-0 or Driver Type-1 or Driver-4 shall meet all AC characteristics and HS400 Device output timing requirements. The Optional Driver Types are defined with reference to Driver Type-0.

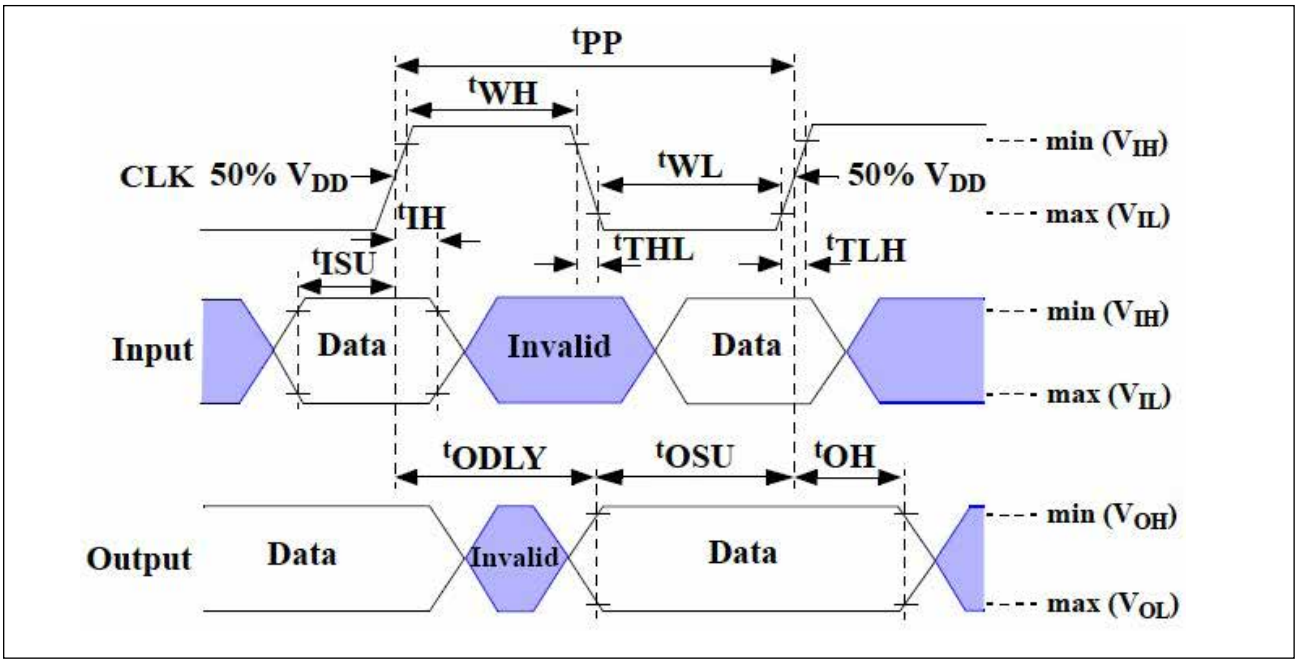
Table 23. Driver Type Value

Driver Type Value	Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0x0	YES	50 Ω	x1	Default Driver Type Support up to 200MHz operation.
0x1	YES	33 Ω	x1.5	Supports up to 200MHz operation.
0x2	YES	66 Ω	x0.75	The weakest driver that supports up to 200MHz operation.
0x3	YES	100 Ω	x0.5	For low noise and low EMI systems.Maximal operating frequency is decided by Host design.
0x4	YES	40 Ω	x1.2	

Note: *Nominal impedance is defined by I-V characteristics of output driver at 0.9V when VCCQ = 1.8V.*

The Driver Type setting should be selected based on the Host system load at desired operating frequency with minimal noise generated. Driver Type-1 or Type-4 is highly recommended for HS200 & HS400 operation.

Figure 4. Bus Timing



Note: *Data must always be sampled on the rising edge of the clock.*

Table 24. Device Interface Timings (High-speed interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	fPP	CL <= 30pF Tolerance: +100KHz	0	52[3]	MHz
Clock frequency Identification Mode (OD)	fOD	Tolerance: +20KHz	0	400	KHz
Clock high time	tWH	CL <= 30pF	6.5	--	ns
Clock low time	tWL	CL <= 30pF	6.5	--	ns
Clock rise time[4]	tTLH	CL <= 30pF	--	3	ns
Clock fall time	tTHL	CL <= 30pF	--	3	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	tISU	CL <= 30pF	3	--	ns
Input hold time	tIH	CL <= 30pF	3	--	ns
Outputs CMD,DAT (referenced to CLK)					
Output Delay time during Data Transfer	tODLY	CL <= 30pF	--	13.7	ns
Output hold time	tOH	CL <= 30pF	2.5	--	ns
Signal rise time[5]	tRISE	CL <= 30pF	--	3	ns
Signal fall time	tFALL	CL <= 30pF	--	3	ns

Notes:

1. *CLK timing is measured at 50% of VCCQ*
2. *Supports the full frequency range from 0-26MHz, or 0-52MHz*
3. *e-MMC can operate as high-speed interface timing at 26MHz clock frequency.*
4. *CLK rise and fall times are measured by min(VIH) and max(VIL).*
5. *Inputs CMD,DAT rise and fall times area measured by min(VIH) and max(VIL), and outputs CMD, DAT rise and fall times are measured by min(VOH) and max(VOL).*

Table 25. Device Interface Timing Waveforms (Backward-compatible interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	fPP	CL <= 30pF	0	26	MHz
Clock frequency Identification Mode (OD)	fOD	Tolerance: +20KHz	0	400	KHz
Clock high time	tWH	CL <= 30pF	10	--	ns
Clock low time	tWL	CL <= 30pF	10	--	ns
Clock rise time[4]	tTLH	CL <= 30pF	--	10	ns
Clock fall time	tTHL	CL <= 30pF	--	10	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	tISU	CL <= 30pF	3	--	ns
Input hold time	tIH	CL <= 30pF	3	--	ns
Outputs CMD,DAT (referenced to CLK)					
Output set-up time [5]	tOSU	CL <= 30pF	11.7	--	ns
Output hold time [5]	tOH	CL <= 30pF	8.3	--	ns

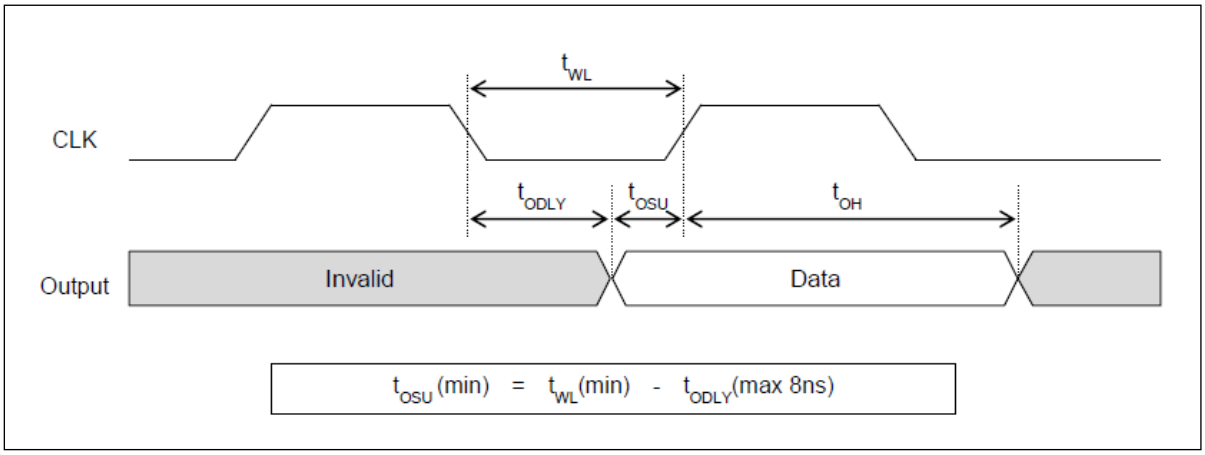
Notes:

1. *The e-MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.*
2. *CLK timing is measured at 50% of VCCQ*
3. *For compatibility with e-MMCs that support the v4.2 standard or earlier, host should not use >26MHz before switching to high-speed interface timing.*
4. *CLK rise and fall times are measured by min(VIH) and max(VIL).*
5. *tOSU and tOH are defined as values from clock rising edge. However, the e-MMC device will utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set tWL value as long as possible within the range which will not go over tCK - tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for the device.*

   e-MMC device utilizes clock falling edge to output data in backward compatibility mode.

   Host should optimize the timing in order to have data set up margin as follows.

Figure 5. Output Timing Waveform



6-2-1. Bus Timing for DAT signals for during 2x data rate operation

These timings applied to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in High-speed interface timing or Backward-compatible interface timing.

Figure 6. Bus Timing Waveform (DAT signals for during 2x data rate operation)

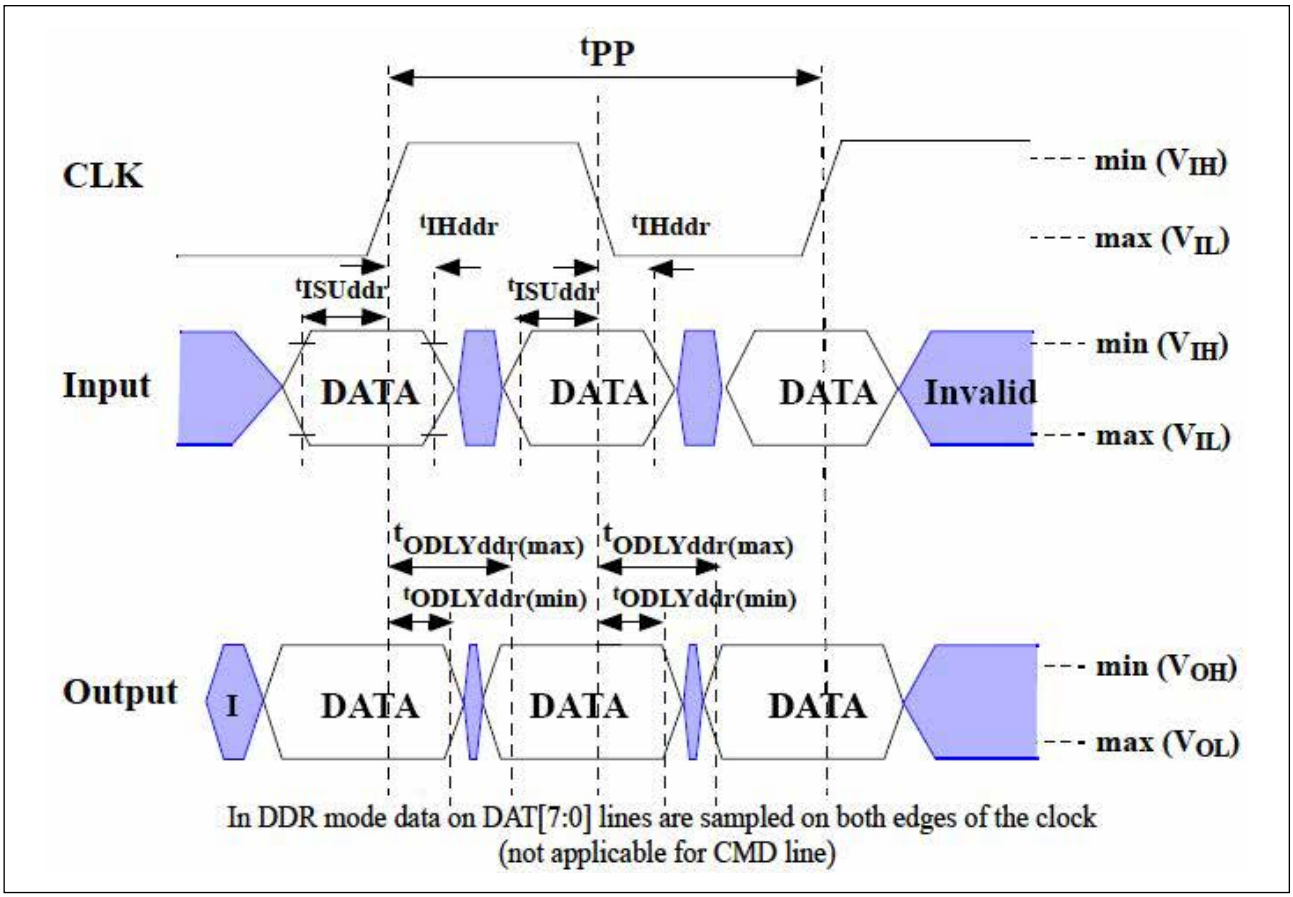


Table 26. High-speed Dual Data-rate interface timings

Parameter	Symbol	Min	Max	Unit	Remark[1]
Input CLK [1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Clock rise time	tTLH		3	ns	CL ≤ 30pF
Clock fall time	tTHL		3	ns	CL ≤ 30pF
Input CMD(referenced to CLK-SDR mode)					
Input setup time	tISUddr	3	--	ns	CL ≤ 20pF
Input hold time	tIHddr	3	--	ns	CL ≤ 20pF
Output CMD (Referenced to CLK-SDR mode)					
Output delay time during data transfer	tODLY	--	13.7	ns	CL ≤ 20pF
Output hold time	tOH	2.5	--	ns	CL ≤ 20pF
Signal rise time	tRISE	--	3	ns	CL ≤ 20pF
Signal fall time	tFALL	--	3	ns	CL ≤ 20pF

Parameter	Symbol	Min	Max	Unit	Remark[1]
Input DAT (Referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5	--	ns	CL ≤ 20pF
Input hold time	tIHddr	2.5	--	ns	CL ≤ 20pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20pF
Signal rise time (all signals) [2]	tRISE	--	2	ns	CL ≤ 20pF
Signal fall time (all signals)	tFALL	--	2	ns	CL ≤ 20pF

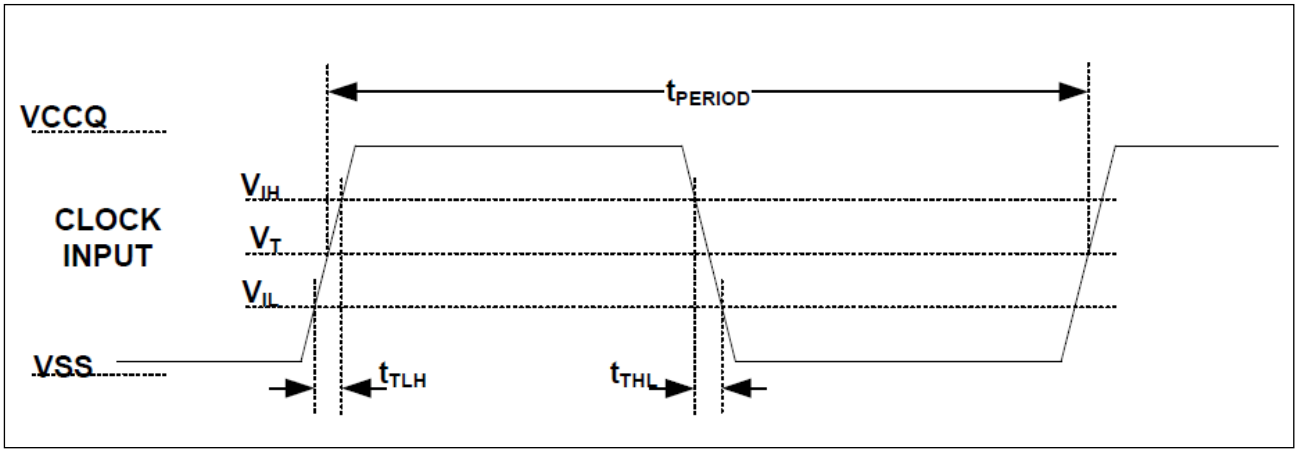
Notes:

1. *CLK timing is measured at 50% of VCCQ.*
2. *Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).*

6-2-2. Bus Timing Specification in HS200 mode

Figure 7. HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in following figure and Table. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device. The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.



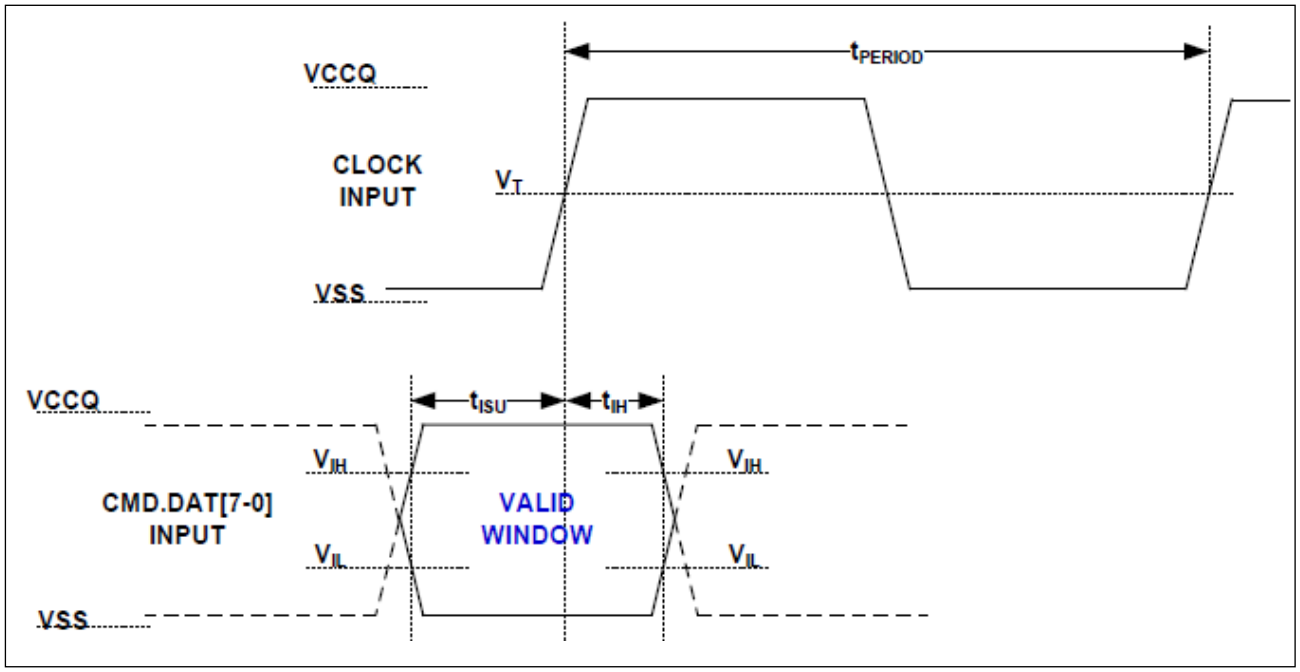
Notes:

1. VIH denote VIH(min.) and VIL denotes VIL(max.).

2 VT = 50% of VCCQ, indicates clock reference point for timing measurements.

Symbol	Min	Max	Unit	Remark
tPERIOD	5	--	ns	200MHz (max.), between rising edges
tTLH, tTHL	--	0.2 * tPERIOD	ns	tTLH, tTHL < 1ns (max.) at 200MHz, CDEVICE=6pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Figure 8. HS200 Device Input Timing



Notes:

1. tISU and tIH are measured at VIL(max) and VIH(min).

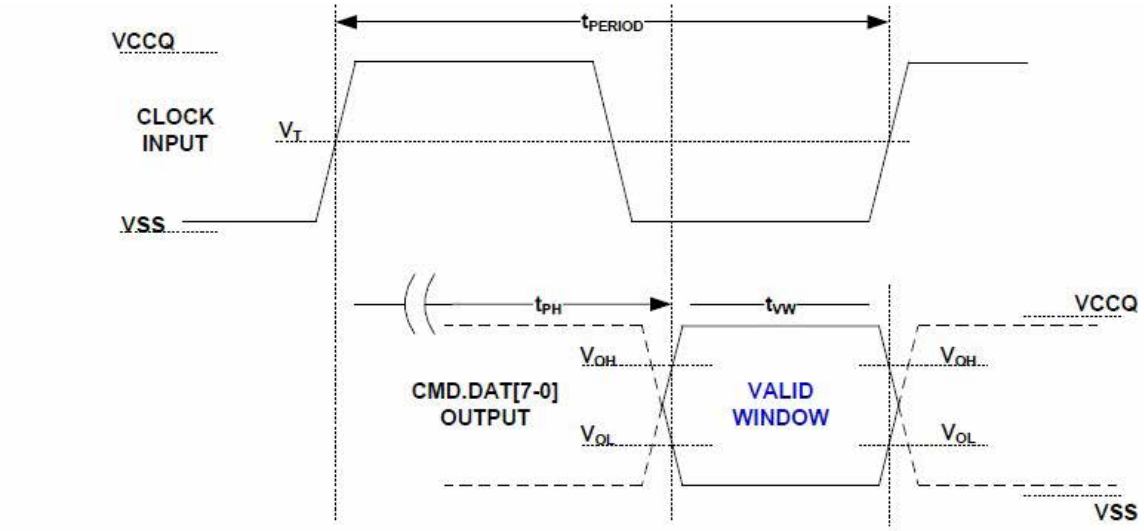
2. VIH denote VIH(min) and VIL denotes VIL(max).

Symbol	Min	Max	Unit	Remark
tISU	1.40	--	ns	CDEVICE <= 6pF
tIH	0.8	--	ns	CDEVICE <= 6pF

Figure 9. HS200 Device Output Timing

tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization, the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔTPH) but position of data window varies by the drift.

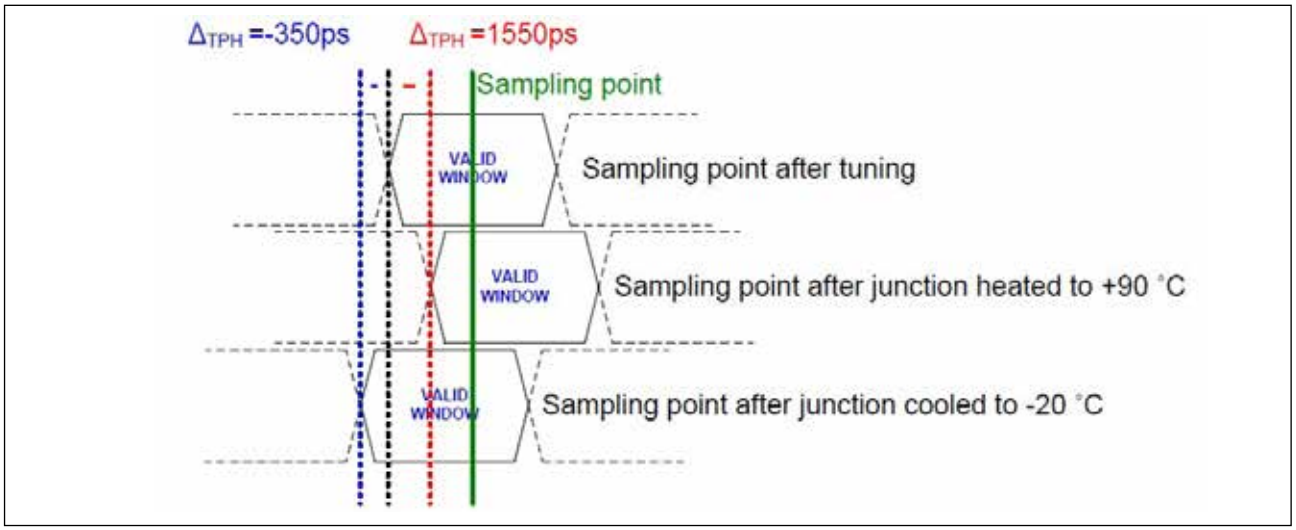


Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Symbol	Min	Max	Unit	Remark
tPH	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift
ΔTPH	-350 (ΔT = -20deg.C)	+1550 (ΔT = 90deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25 deg. C to 125 deg.C during operation.
tVW	0.575	--	UI	tVW =2.88ns at 200MHz Using test circuit in following figure including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected tVW at Host input is larger than 0.475UI.

Note: *Unit Interval (UI) is one bit nominal time. For example, UI = 5ns at 200MHz.*

Figure 10. ΔTPH Consideration



Implementation Guide:

Host should design to avoid sampling errors that may be caused by the ΔTPH drift.

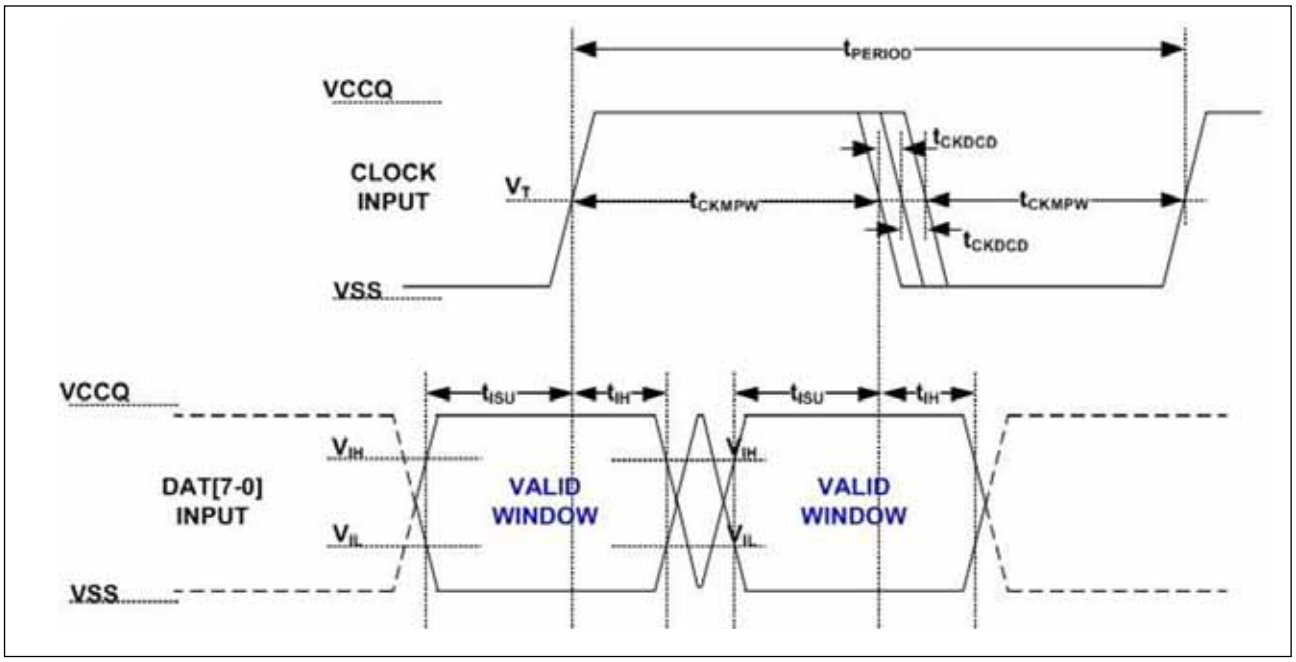
It is recommended to perform tuning procedure while Device wakes up, after sleep.

One simple way to overcome the ΔTPH drift is by reduction of operating frequency.

6-2-3. Bus Timing Specification in HS400 mode

Figure 11. HS400 Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



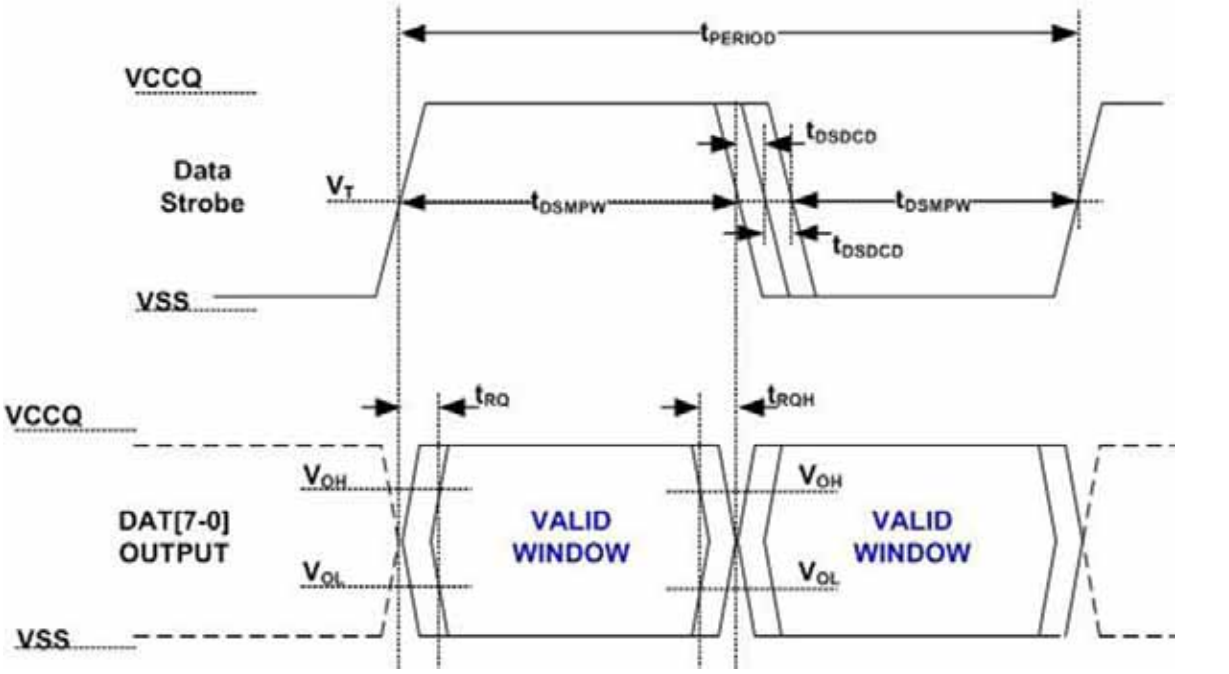
Note: *VT = 50% of VCCQ, indicates clock reference point for timing measurements.*

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VIH /VIL
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT
Input DAT(Referenced to CLK)					
Input setup time	tISUddr	0.4		ns	CDevice<=6pF With respect to VIH /VIL
Input hold time	tIHddr	0.4		ns	CDevice<=6pF With respect to VIH /VIL
Slew rate	SR	1.125		V/ns	With respect to VIH /VIL

Note: *Not 100% tested. Characterization only.*

Figure 12. HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



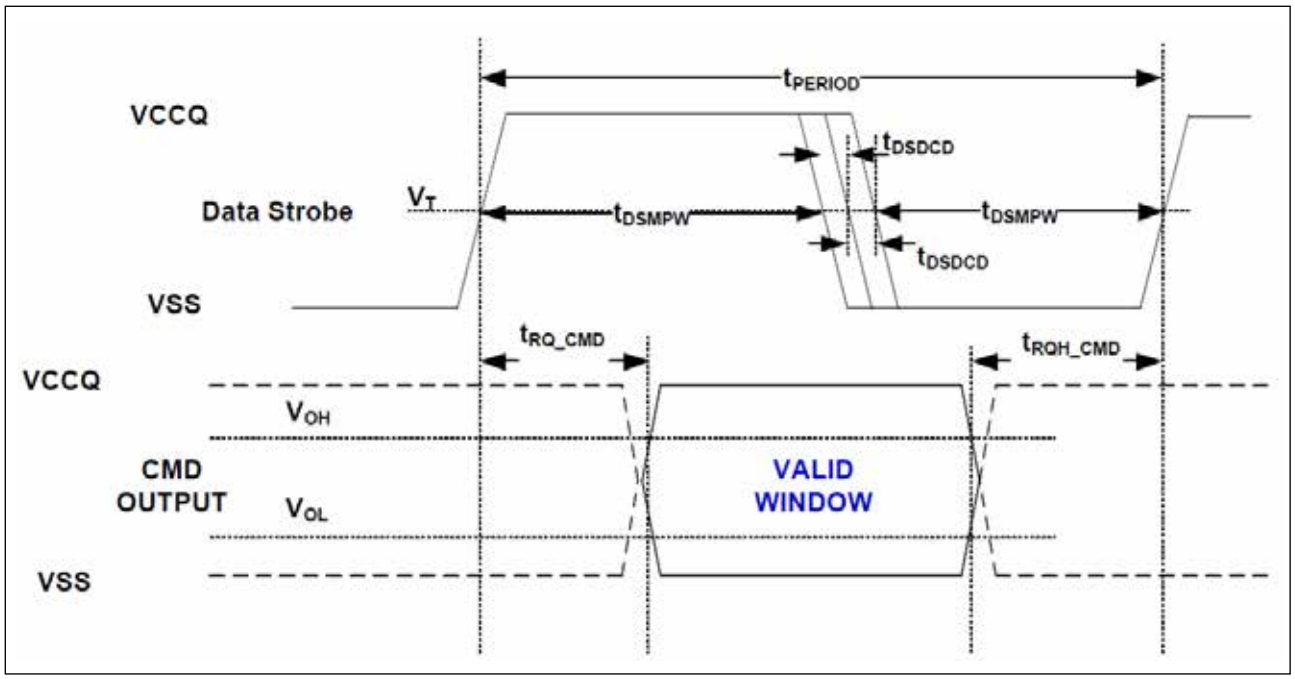
Note: *VT = 50% of VCCQ; indicates clock reference point for timing measurements.*

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion(tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max Value is specified by manufacture. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max Value is specified by manufacture. Value up to infinite is valid
Output DAT(referenced to Data Strobe)					
Output skew	tRQ		0.4	ns	With respect to VOH /VOL and HS400 reference load
Output hold skew	tRQH		0.4	ns	With respect to VOH /VOL and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to VOH /VOL and HS400 reference load

Note: *Not 100% tested. Characterization only.*

Figure 13. HS400 Device Command Output Timing

The Data Strobe is used to response of any command in HS400 mode.



Note: *VT = 50% of VCCQ, indicates clock reference point for timing measurements.*

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion(tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max Value is specified by manufacture. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max Value is specified by manufacture. Value up to infinite is valid
Output DAT(referenced to Data Strobe)					
Output skew	tRQ_CMD		0.4	ns	With respect to VOH /VOL and HS400 reference load
Output hold skew	tRQH_CMD		0.4	ns	With respect to VOH/VOL and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to VOH /VOL and HS400 reference load

Note: *Not 100% tested. Characterization only.*

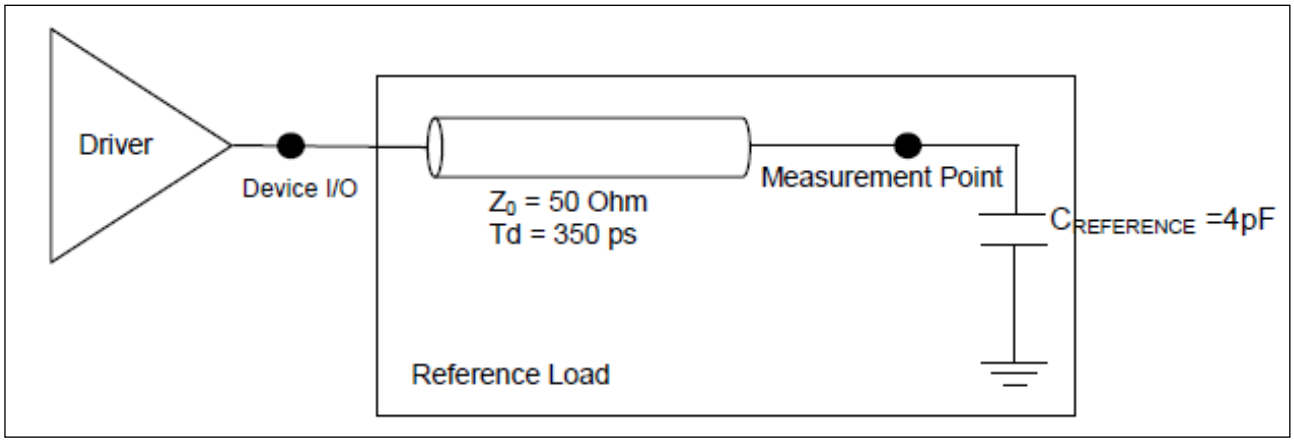
Table 27. HS400 Capacitance and Resistors

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7	100	kΩ	
Pull-up resistance for DAT0-7	RDAT	10	100	kΩ	
Pull-down resistance for Data Strobe	RDS	10	100	kΩ	
Internal pull up resistance DAT1-DAT7	Rint	10	150	kΩ	
Single Device capacitance	CDEVICE		6	pF	

Note: *1. Recommended maximum value is 50 kΩ for 1.8V interface supply voltages.*

2. Not 100% tested. Characterization only.

Figure 14. HS400 reference load



The circuit shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the CREFERENCE capacitance.

Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

Table 28. Overshoot/Undershoot Specifications

		VCCQ		Unit
		2.7V-3.6V	1.70V-1.95V	
Maximum peak amplitude allowed for overshoot area. (Refer to *"Figure 15. Overshoot/Undershoot Definition"*)	Max.	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area. (Refer to *"Figure 15. Overshoot/Undershoot Definition"*)	Max.	0.9	0.9	V
Maximum area above VCCQ (Refer to *"Figure 15. Overshoot/Undershoot Definition"*)	Max.	1.5	1.5	V-ns
Maximum area below VSSQ (Refer to *"Figure 15. Overshoot/Undershoot Definition"*)	Max.	1.5	1.5	V-ns

Note: *Not 100% tested. Characterization only.*

Figure 15. Overshoot/Undershoot Definition

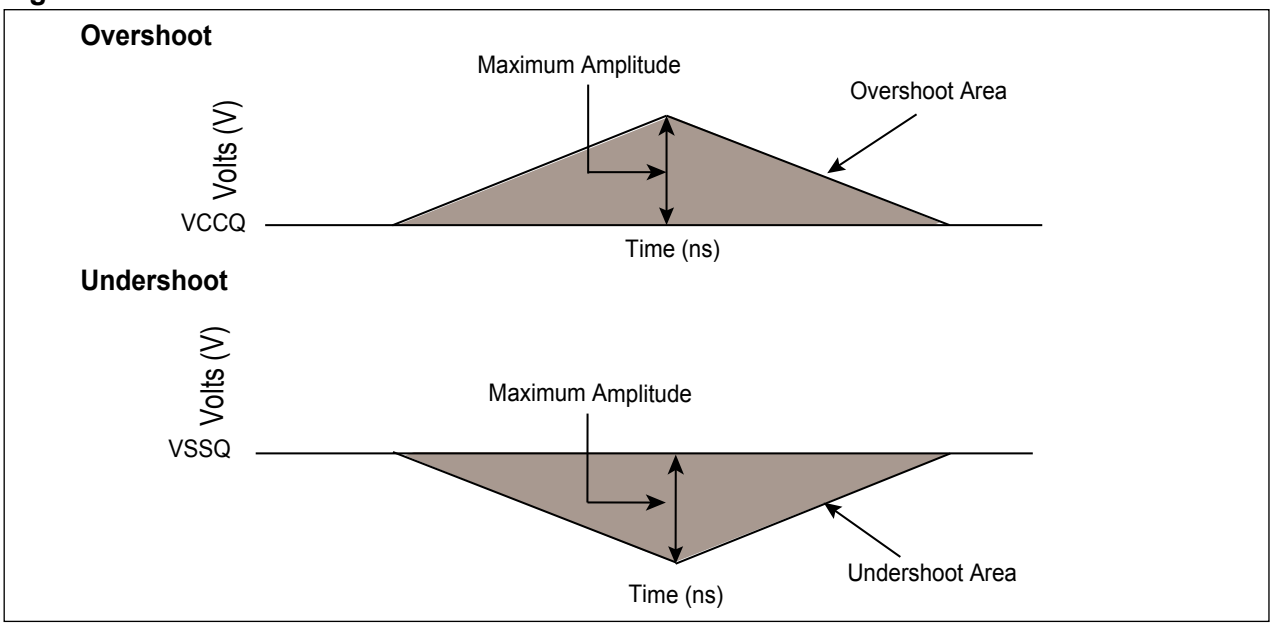
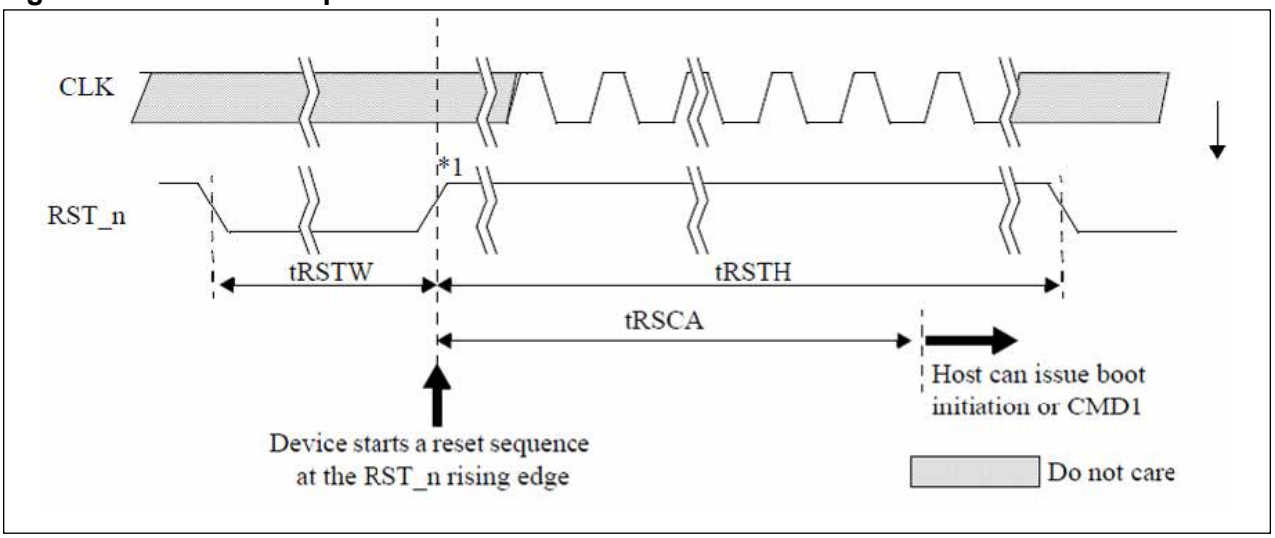


Figure 16. H/W Reset Operation



Note 1: *Device will detect the rising edge of RST_n signal to trigger internal reset sequence.*

Table 29. H/W Reset Timings

Parameter	Symbol	Min	Max	Unit
RST_n pulse width	tRSTW	1	--	µs
RST_n to Command time	tRSCA	200 [1]	--	µs
RST_n high period (interval time)	tRSTH	1	--	µs

Notes:

1. 74 cycles of clock signal are required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

2. During the device internal initialization sequence right after power on, device may not be able to detect RST_n signal, because the device may not complete loading RST_n_ENABLE bits of the extended CSD register into the controller yet.

3. Not 100% tested. Characterization only.

Figure 17. Power up Sequence

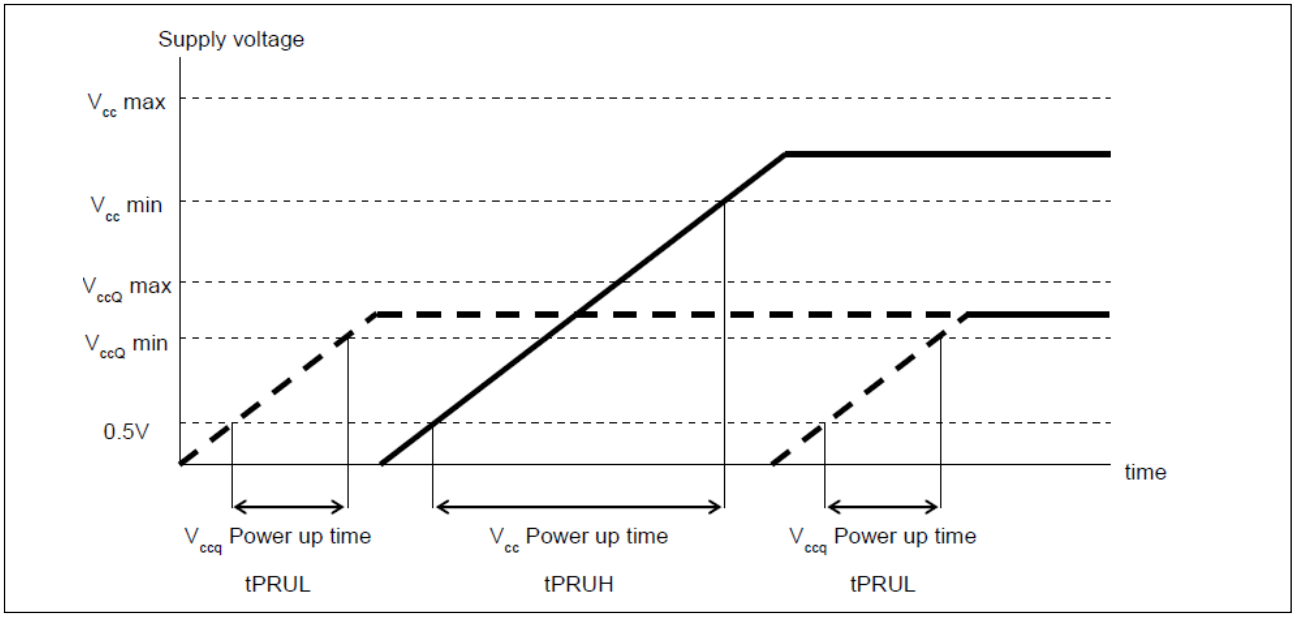


Table 30. Power-up Parameters

Parameter	Symbol	Min	Max	Unit
Supply power-up for 3.3V	tPRUH	5 µs	35 ms	
Supply power-up for 1.8V	tPRUL	5 µs	25 ms	

Notes:

1. 74 cycles of clock signal are required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

2. During the device internal initialization sequence right after power on, device may not be able to detect RST_n signal, because the device may not complete loading RST_n_ENABLE bits of the extended CSD register into the controller yet.

3. During the power-up sequence (VCC ramp up), the power supply voltage of Vcc should ramp up in a monotonic non-decreasing fashion. The VCC waveform should not have a dip during the rising phase. The voltage drop before reaching VCCmin may cause errorneous device operation.

4. Not 100% tested. Characterization only.

6-3. System Performance

Table 31. Sequential Performance

Frequency/Mode		Typ. Performance [MB/Sec]	
		Read	Write
08GB	HS200	175	150
	HS400	320	165

Notes: *x8 Mode*

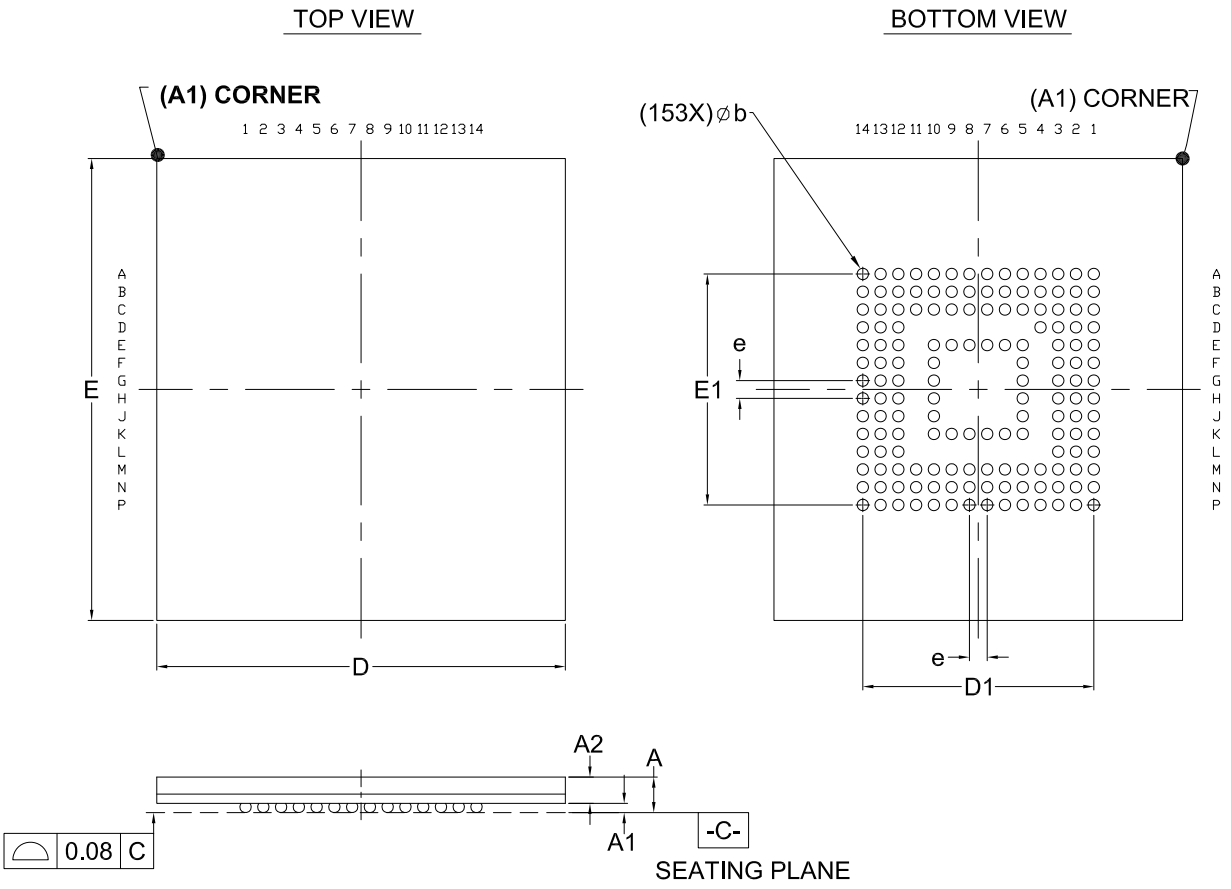
Test data size: 100MB

Chunk size: 4MB

Tested under U-boot/Cache on/packed on/Clean condition/Room temperature(25°C)

7. PACKAGE INFORMATION

7-1. Package Outline 153 BALLS LFBGA (11.5 x 13 x 1.0mm, Ball pitch: 0.5mm)



Note:
Test pads may be present but are not shown. They are for internal use only and are not solder balls.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.66	0.25	11.4	---	12.9	---	---
	Nom.	---	0.21	---	0.30	11.5	6.5	13.0	6.5	0.50
	Max.	1.0	0.26	---	0.35	11.6	---	13.1	---	---
Inch	Min.	---	0.006	0.026	0.010	0.449	---	0.508	---	---
	Nom.	---	0.008	---	0.012	0.453	0.256	0.512	0.256	0.0197
	Max.	0.039	0.010	---	0.014	0.457	---	0.516	---	---

8. REVISION HISTORY

Revision	Descriptions	Page
May 11, 2026		
0.00	Initial Release.	ALL
August 21, 2026		
1.0	1. Removed "Advanced Information" to align with the product status.	ALL
	2. Modified *"Table 10. CID Register"*.	P21
	3. Updated [21:18] values of CSD Register Table.	P26
	4. Modified *"Table 31. Sequential Performance".*	P47
	5. Content modification.	P6,19,30

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