*1.8V 1G-bit/2G-bit/4G-bit Serial NAND Flash Memory*

# MX35UFxGE4AD

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# 1. FEATURES

- **1Gb, 2Gb, 4Gb Serial Flash**
  - Bus: x4
  1Gb/2Gb: page size: (2048+64) byte, block size: (128K+4K) byte[Note1]
  4Gb: page size: (4096+128) byte, block size: (256K+8K) byte[Note1]
- **Fast Read Access**
  - Supports Random data read out by x1 x2 & x4 modes, (1-1-1,1-1-2, 1-1-4, 1-2-2, 1-4-4)[Note 2]
  - Latency of array to register: 80us for 1Gb/2Gb, 110us for 4Gb
  - Frequency: 133MHz[Note3]
  - Continuous read supported
- **Page Program Operation**
  - Page program time: 360us(typ.) for 1Gb/2Gb, 400us(typ.) for 4Gb
- **Block Erase Operation**
  - Block erase time: 4ms(typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 to 1.95V
- **BP bits for block group protection**
- **Unique ID Read with PUF type code structure**
- **Low Power Dissipation**
  - Max 40mA
  Active current (Read/Program/Erase)
- **Standby Mode**
  - 110uA (Max) standby current
- **High Reliability**
  - Special Read for data recovery : Enabled by Set Feature
  - Program / Erase Endurance: Typical 60K cycles with 8-bit ECC per (512+32) Byte
  - Flexible ECC Bit Flip Threshold Setting by user
  - Data Retention: 10 years
- **BBM Table (Bad Block Table) supported**
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  1) 8-WSON (8mm x 6mm)
  2) 24-Ball BGA (6x8mm, 5x5 ball array)
  All packaged devices are RoHS Compliant and Halogen-free.

***Note 1.*** *When internal ECC is disable, the page size and block size will be extended to 2KB+128B per page and 128KB+8KB per block (for 1Gb/2Gb), 4KB+256B per page and 256KB+16KB per block (for 4Gb)*

***Note 2.*** *Which indicates the number of I/O for command, address and data.*

***Note 3.*** *fC=133MHz max. for non-continuous read operation.*

# 2. GENERAL DESCRIPTIONS

The MX35UFxGE4AD is a 1.8V 1Gb/2Gb/4Gb SLC NAND Flash memory device with Serial interface.

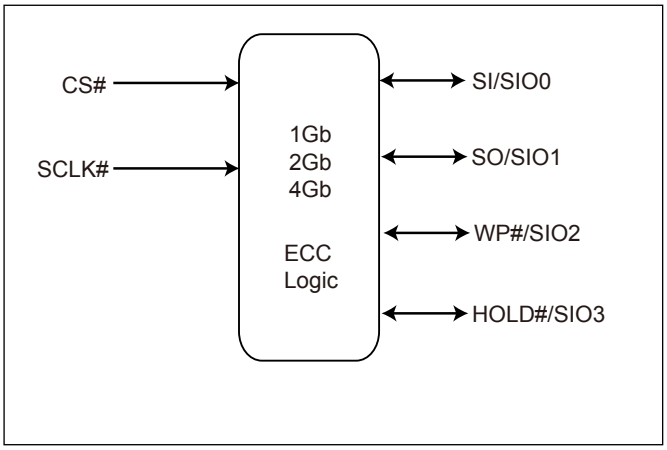
The memory array of this device adopted the same cell architecture as the parallel NAND, however implementing the industry standard serial interface.

An internal 8-bit ECC logic is implemented in the chip, which is enabled by default. The internal ECC can be disabled or enabled again by command. When the internal 8-bit ECC logic is disabled, the host side needs to handle the 8-bit ECC by host micro controller.

The device supports conventional read mode and continuous read modes. If the configuration register bit "CONT" = 0, the device is in conventional read mode which user cannot read across a page without page read command. If the configuration register bit "CONT" = 1, the device is in continuous read mode which user can read consecutive page across page boundary without next page read command.

Considering user effort reduction, the device provides 40 links of BBM (Bad Block Management), which can provide the continuous good blocks to save software effort and increase read throughput. Moreover, user may enhance the P/E endurance cycle of single block by using more than one BBM links for block replacement to same single block. For example, using two BBM links for same single block replacement which may double the P/E cycle of the same single block, using three BBM links may get triple P/E cycle and so on.

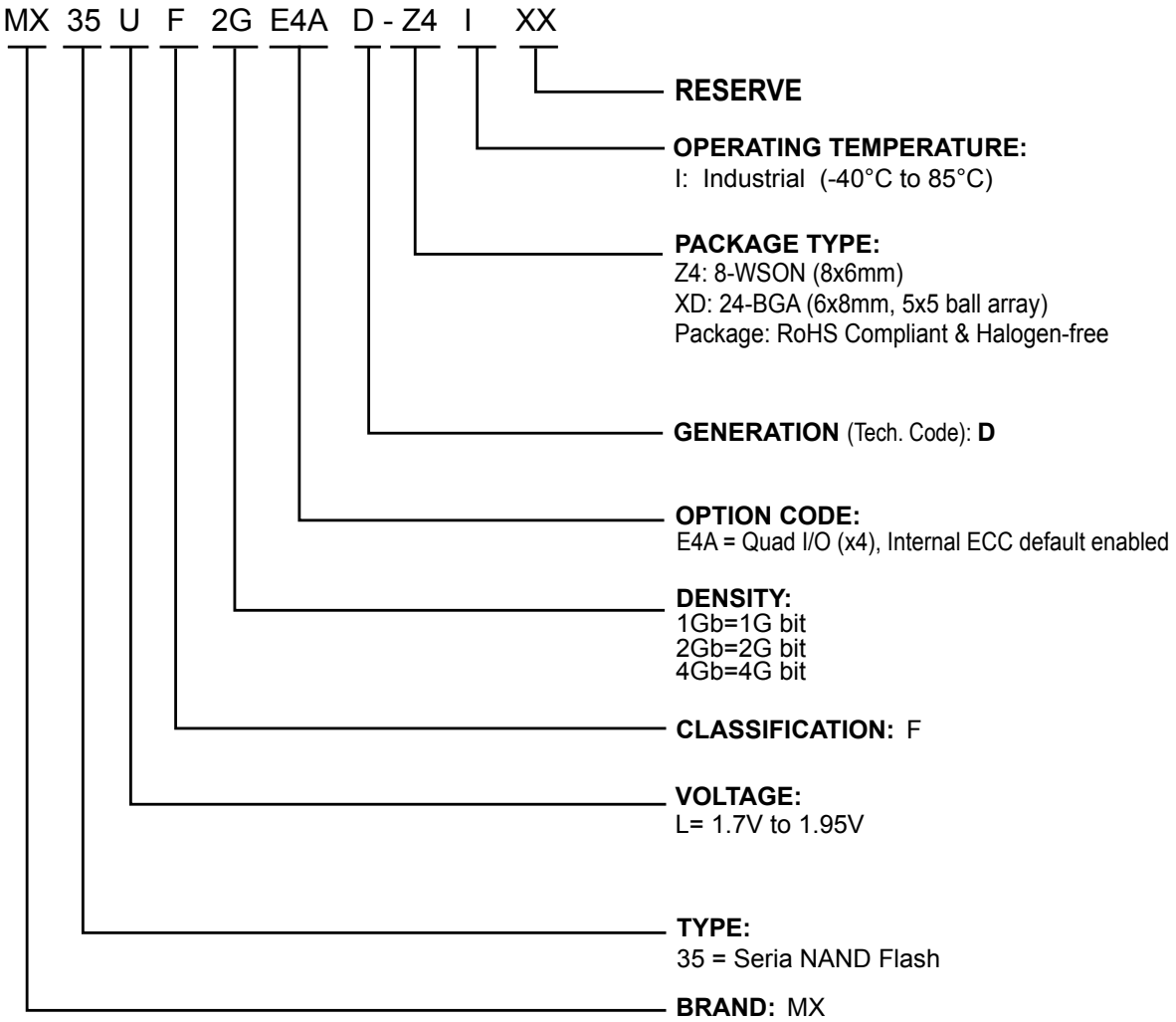
**Figure 1. Logic Diagram**



# 3. ORDERING INFORMATION

**Part Name Description**

Macronix New Serial Flash devices are available in different configurations and densities. Verify valid part numbers by using Macronix's product search at http://www.Macronix.com. Contact Macronix sales for devices not found.




Please contact our regional sales for the latest product selection and available form factors.

| Part Number | Density | Organization | VCC Range | Package | Temperature Grade |
|---|---|---|---|---|---|
| MX35UF4GE4AD-Z4I | 4Gb | x4 | 1.8V | 8-WSON | Industrial |
| MX35UF4GE4AD-XDI | 4Gb | x4 | 1.8V | 24-BGA | Industrial |
| MX35UF2GE4AD-Z4I | 2Gb | x4 | 1.8V | 8-WSON | Industrial |
| MX35UF2GE4AD-XDI | 2Gb | x4 | 1.8V | 24-BGA | Industrial |
| MX35UF1GE4AD-Z4I | 1Gb | x4 | 1.8V | 8-WSON | Industrial |
| MX35UF1GE4AD-XDI | 1Gb | x4 | 1.8V | 24-BGA | Industrial |

# 4. BALL ASSIGNMENT AND DESCRIPTIONS

**Figure 2. 8-WSON (8x6mm)**

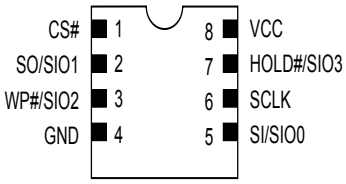
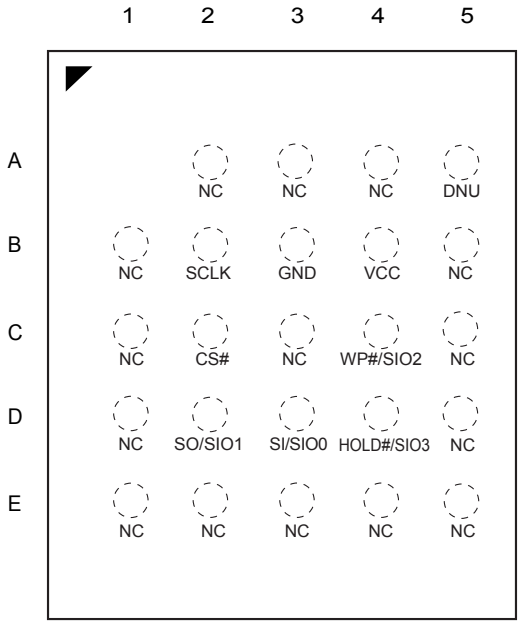



**Figure 3. 24-Ball BGA (5x5 Ball Array)**




# 5. PIN DESCRIPTIONS

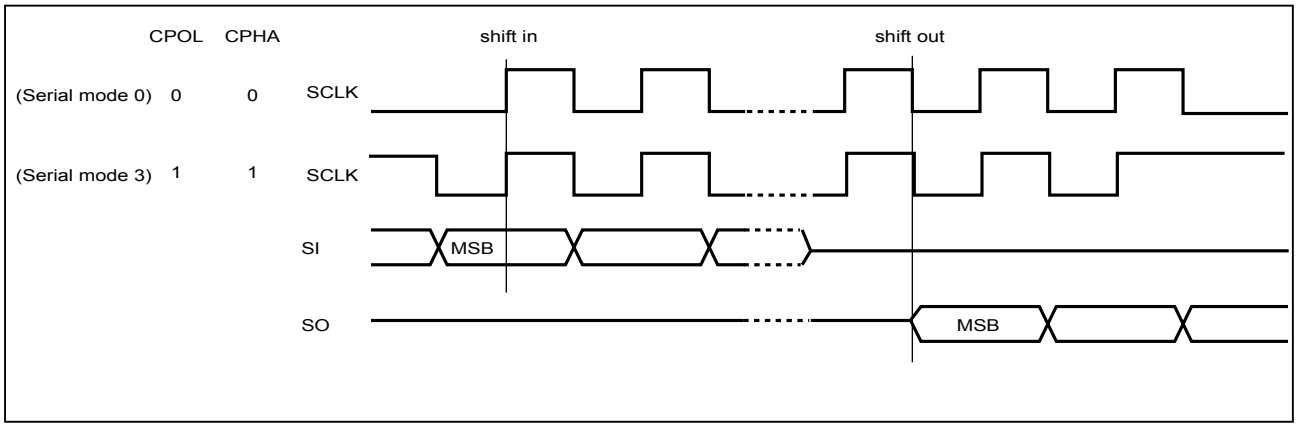
| SYMBOL | DESCRIPTION |
|---|---|
| **CS#** | Chip Select |
| **SI/SIO0** | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode) |
| **SO/SIO1** | Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode) |
| **SCLK** | Clock Input |
| **WP#/SIO2** | Write protection: connect to GND or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode) |
| **HOLD#/ SIO3** | Hold or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode) |
| **VCC** | + 1.8V Power Supply |
| **GND** | Ground |
| **DNU** | Do Not Use |

***Note 1**. Which indicates the number of I/O for command, address, and data.*

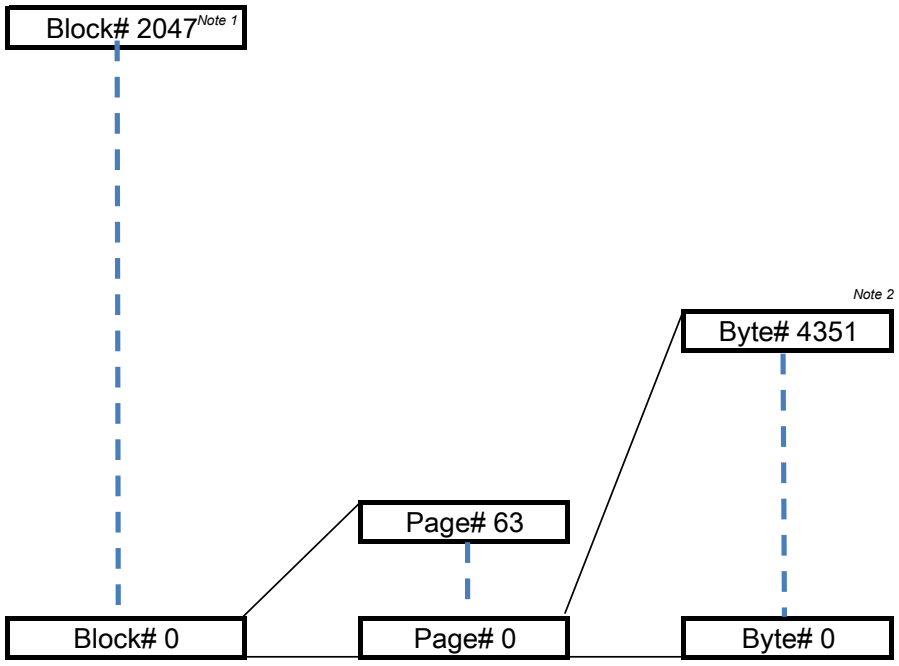
# 6. DEVICE OPERATION

1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When an incorrect command is written to this device, it enters standby mode and stays in the standby mode until the next CS# falling edge. In standby mode, the device's SO pin should be High-Z.
3. When an correct command is written to this device, it enters active mode and stays in the active mode until the next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as **"Figure 4. Serial Mode Supported"**.
5. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

**Figure 4. Serial Mode Supported**



# 7. ADDRESS MAPPING




| Block address | Page address | Byte address |
|---|---|---|
| 2Gb/4Gb: RA [16:6]<br>1Gb: RA[15:6] | RA [5:0] | CA [12:0]Note 3 |

***Note 1:*** *2048 for 2Gb/4Gb, 1023 for 1Gb*

***Note 2:*** *Byte#=2175 for 1Gb/2Gb*

***Note 3:*** *CA[11:0] for 1Gb/2Gb*

# 8. COMMAND DESCRIPTION

**Table 1. Command Set - Standard Operation**

(SPI_NOR_EN = 0, CONT = 0)[Note1]

| Mode | 1st Byte | 2nd Byte | 3rd Byte | 4th Byte | 5th Byte | 6th Byte | 7th Byte | 8th Byte |
|---|---|---|---|---|---|---|---|---|
| **Get Feature** | 0Fh | ADD | Data | | | | | |
| **Read Status** | 05h | Data | | | | | | |
| **Set Feature** | 1Fh | ADD | Data | | | | | |
| **Page Read** | 13h | RADD2 | RADD1 | RADD0 | | | | |
| **Page Read Cache Random** | 30h | RADD2 | RADD1 | RADD0 | | | | |
| **Page Read Cache Sequential** | 31h | | | | | | | |
| **Page Read Cache End** | 3Fh | | | | | | | |
| **Read From Cache x1** | 03h | CADD1 | CADD0 | DUMMY | DATA~ | | | |
| **Read From Cache x1 (Alternative)** | 0Bh | CADD1 | CADD0 | DUMMY | DATA~ | | | |
| **Read From Cache x2**[Note4] | 3Bh | CADD1 | CADD0 | DUMMY | DATA~[*2] | | | |
| **Read From Cache x4**[Note4] | 6Bh | CADD1 | CADD0 | DUMMY | DATA~[*4] | | | |
| **Read From Cache Dual IO 1-2-2**[Note4] | BBh | CADD1[*2] | CADD0[*2] | DUMMY[*2] | DATA~[*2] | | | |
| **Read From Cache Quad IO 1-4-4**[Note4] | EBh | CADD1[*4] | CADD0[*4] | DUMMY[*4] | DUMMY[*4] | DATA~[*4] | | |
| **Read ID** | 9Fh | DUMMY | MID | DID1 | DID2 | | | |
| **Block Erase** | D8h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Execute** | 10h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Load x1** | 02h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load Random Data x1** | 84h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load x4**[Note4] | 32h | CADD1 | CADD0 | DATA~[*4] | | | | |
| **Program Load Random Data x4**[Note4] | 34h | CADD1 | CADD0 | DATA~[*4] | | | | |
| **Write Enable** | 06h | | | | | | | |
| **Write Disable** | 04h | | | | | | | |
| **Reset** | FFh | | | | | | | |
| **Read ECCSR** | 7Ch | DUMMY | SR_ECC | | | | | |
| **Write BBM** | A1h | LBA | LBA | PBA | PBA | | | |
| **Read BBM**[Note2] | A5h | DUMMY | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1~ |
| **ECC Warning Page Address**[Note3] | A9h | DUMMY | RADD2_L | RADD1_L | RADD0_L | RADD2_F | RADD1_F | RADD0_F |

***Notes:***

1. *The device supports different feature configurations by configuration register bits. This command table is for standard operation (SPI_NOR_EN = 0, CONT = 0); for details of SPI_NOR_EN, CONT bits, please refer to the relative sections.*
2. *A5h command may read the 40 links of BBM_table (LBAx/PBAx)*
3. *RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address*
4. **2 stands for the dual I/O phase and *4 for quad I/O mode.*

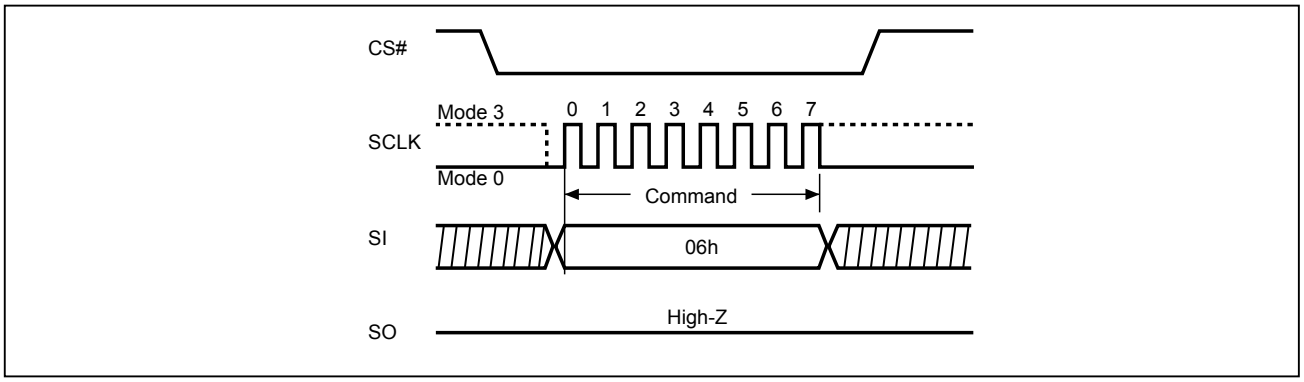
## 8-1. WRITE Operations

### 8-1-1. Write Enable

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit. Instructions like Page Program, Secure OTP program, Block erase, and Write BBM that are intended to change the device content, should be preceded by the WREN instruction.

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

**Figure 5. Write Enable (WREN) Sequence**



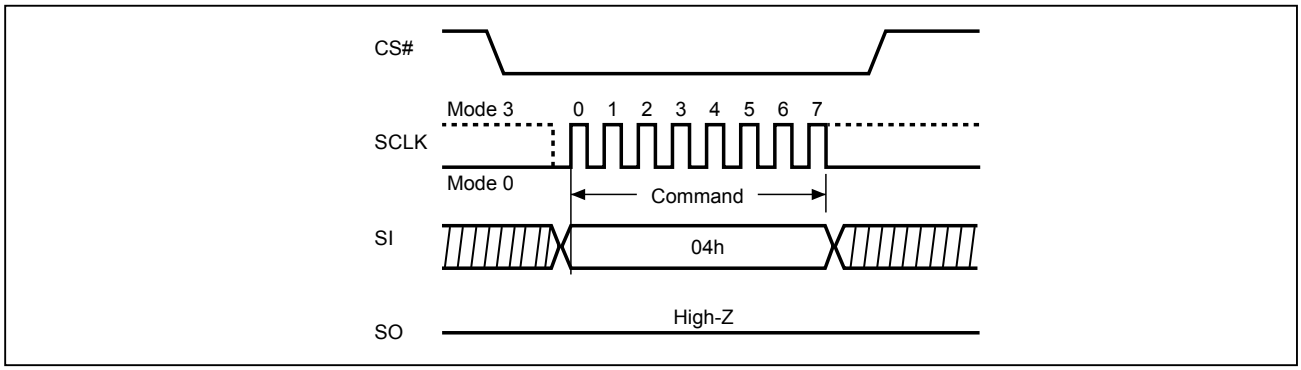

### 8-1-2. Write Disable (04h)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high. It disables the following operations:

- Block Erase
- Secure OTP program
- Page program
- Write BBM

**Figure 6. Write Disable (WRDI) Sequence**



## 8-2. Feature Operations

### 8-2-1. GET Feature (0Fh) and SET Feature (1Fh)

By issuing a one byte address into the feature address, the device may then decide if it's a feature read or feature modification. (0Fh) is for the "GET FEATURE"; (1Fh) is for the "SET FEATURE".

The RESET command (FFh) will clear the status and special read for data recovery registers, the other feature registers remain until the power is being cycled or modified by the settings in the table below. After a RESET command (FFh) is issued, the Status register OIP bit0 or CRBSY will go high. These bits can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the RESET command (FFh) has no effect on the Block Protection and Configuration registers.

The Block Protection and Configuration registers will return to their default state after a power cycle, and can also be changed using the Set Feature command. Issuing the Get Feature command to read the selected register value will not affect register content.

**Table 2. Configuration Registers**

| ADD | Register | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Factory Default Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10h | Configuration | bit name | BFT3 | BFT2 | BFT1 | BFT0 | | | | ENPGM | F0h |
| | | Type | V2 | V2 | V2 | V2 | | | | V | |
| 60h | Configuration | bit name | | | | | | | SPI_NOR_EN | OTPRWSP | 00h |
| | | Type | | | | | | | OTP | OTP | |
| 70h | Special Read for Data Recovery | bit name | | | | | | SPEC_RD2 | SPEC_RD1 | SPEC_RD0 | 00h |
| | | Type | | | | | | V | V | V | |
| A0h | Block Protection | bit name | BPRWD[Note1] | | BP2 | BP1 | BP0 | Invert | Comp. | SP[Note2] | 38h |
| | | Type | V | | V | V | V | V | V | V | |
| B0h | Configuration | bit name | OTP_PROT | OTPEN | | ECC_EN | | CONT | | QE | 10h |
| | | Type | V | V | | V | | V2 | | V | |
| C0h | Status | bit name | CRBSY | BBMT_F | ECC_S1 | ECC_S0 | P-FAIL | E_FAIL | WEL | OIP | 00h |
| | | Type | V | V | V | V | V | V | V | V | |
| E0h | Configuration | bit name | DS_IO[1] | DS_IO[0] | | | | | | | 00h |
| | | Type | V2 | V2 | | | | | | | |

V2: Volatile, The default value of these volatile feature bits can be changed once by Special OTP Configuration Register Program Operation.

V: Volatile.

OTP: one time setting.

***Note1:*** *If BPRWD is enabled and WP# is LOW, then the block protection register can not be changed.*

***Note 2:*** SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of protection bits (BPx bits, invert bits, complementary bits) cannot be changed during the current power cycle.

***Note 3:*** This is the shipment power on default value, user can change the default value of registers of OTP/V2 type by Special OTP Configuration Register Program Operation.

***Note 4:*** All the reserved bits must keep low including the undefined register.

**Table 3. I/O Strength Feature Table**

| DS_IO[1] | DS_IO[0] | Drive Strength |
|---|---|---|
| 0 | 0 | normal (defaul, 25 ohm typical) |
| 0 | 1 | underdrive 1 (35 ohm typical) |
| 1 | X | underdrive 2 (85 ohm typical) |

**Figure 7. GET FEATURE (0Fh) Timing**

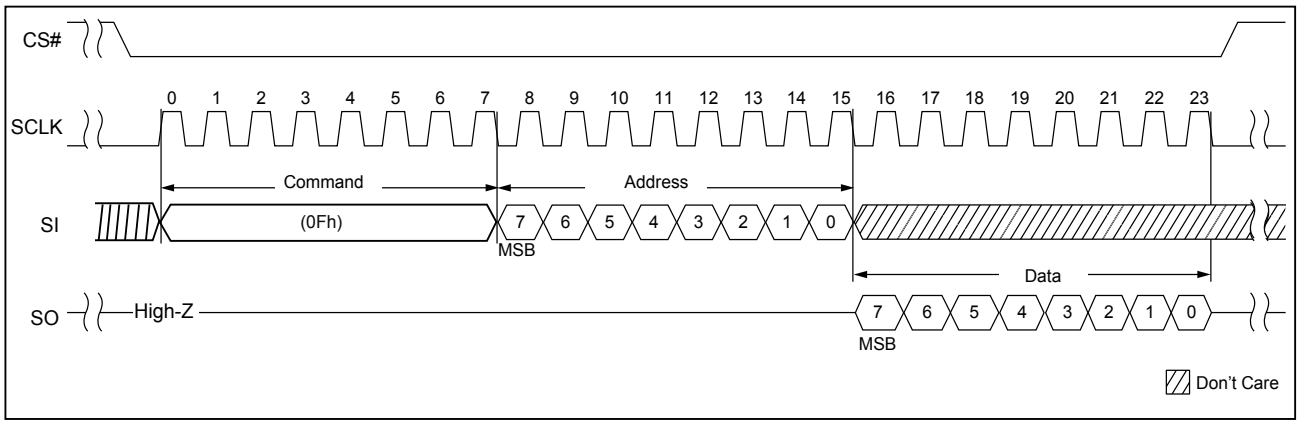
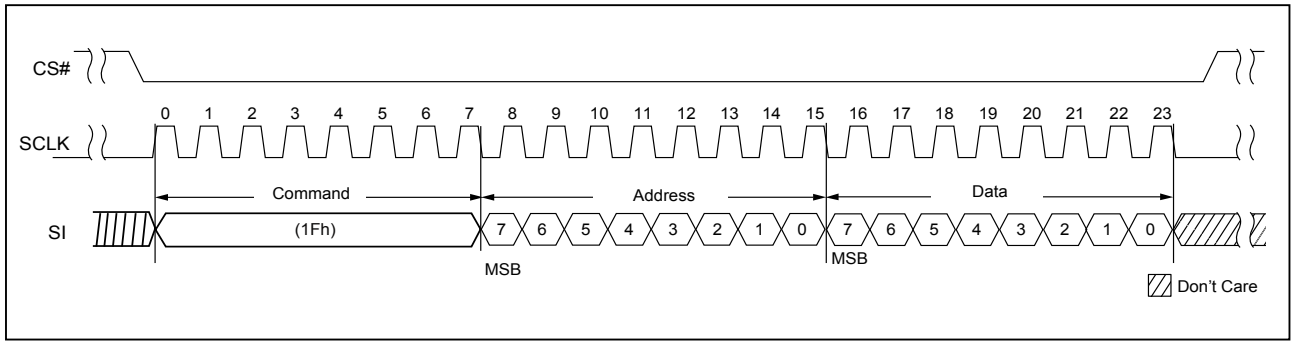



**Figure 8. SET FEATURE (1Fh) Timing**



## 8-3. READ Operations

The device supports "Power-on Read" function, after power up, host may issue the Read From Cache command, and the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the data from the cache buffer.

The device supports conventional read mode and continuous read modes.

If the configuration register bit “CONT” = 0, the device is in conventional read mode. The page read operation and page read cache Random/sequential operation is supported in the conventional read mode. If the configuration register bit “CONT” = 1, the device is in continuous read mode and only continuous read operation is supported. During the continuous read mode, the page read cache related commands are not supported (Page Cache Sequential (31h), Page Read Cache Random (30h) and Page Read Cache End (3Fh)).

**Table 4. Supported Read Command Table for Different Modes**

| Read command | Command Code | Read Mode | |
|---|---|---|---|
| | | Conventional Read Mode | Continuous Read Mode |
| Page Read | 13h | V | V |
| Page Read Cache Random | 30h | V | |
| Page Read Cache Sequential | 31h | V | |
| Page Read Cache End | 3Fh | V | |

**Table 5. Data Output Range Per Page**

| Configuration Register Bit "CONT" | Read Mode | Data Length per Page | | | |
|---|---|---|---|---|---|
| | | ECC Enabled | | ECC Disabled | |
| | | 1Gb/2Gb | 4Gb | 1Gb/2Gb | 4Gb |
| CONT=0 | Conventional Read mode | 2048+64 | 4096+128 | 2048+128 | 4096+256 |
| CONT=1 | Continuous Read mode | 2048 | 4096 | - | - |

### 8-3-1. PAGE READ (13h)

The page read operation transfers data from array to cache by issuing the page read (13h)command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) or 05h (RDSR) may be used to poll the operation status.

After read operation is completed, the Read from Cache (03H or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh), read from cache dual IO (1-2-2) (BBh) and Read from cache Qual IO (1-4-4) (EBh) may be issued to fetch the data.

### 8-3-2. QE bit

The Quad Enable (QE) bit, volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the feature of Hardware Protection Mode(HPM) and HOLD# will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

**Figure 9. PAGE READ (13h) Timing x1**

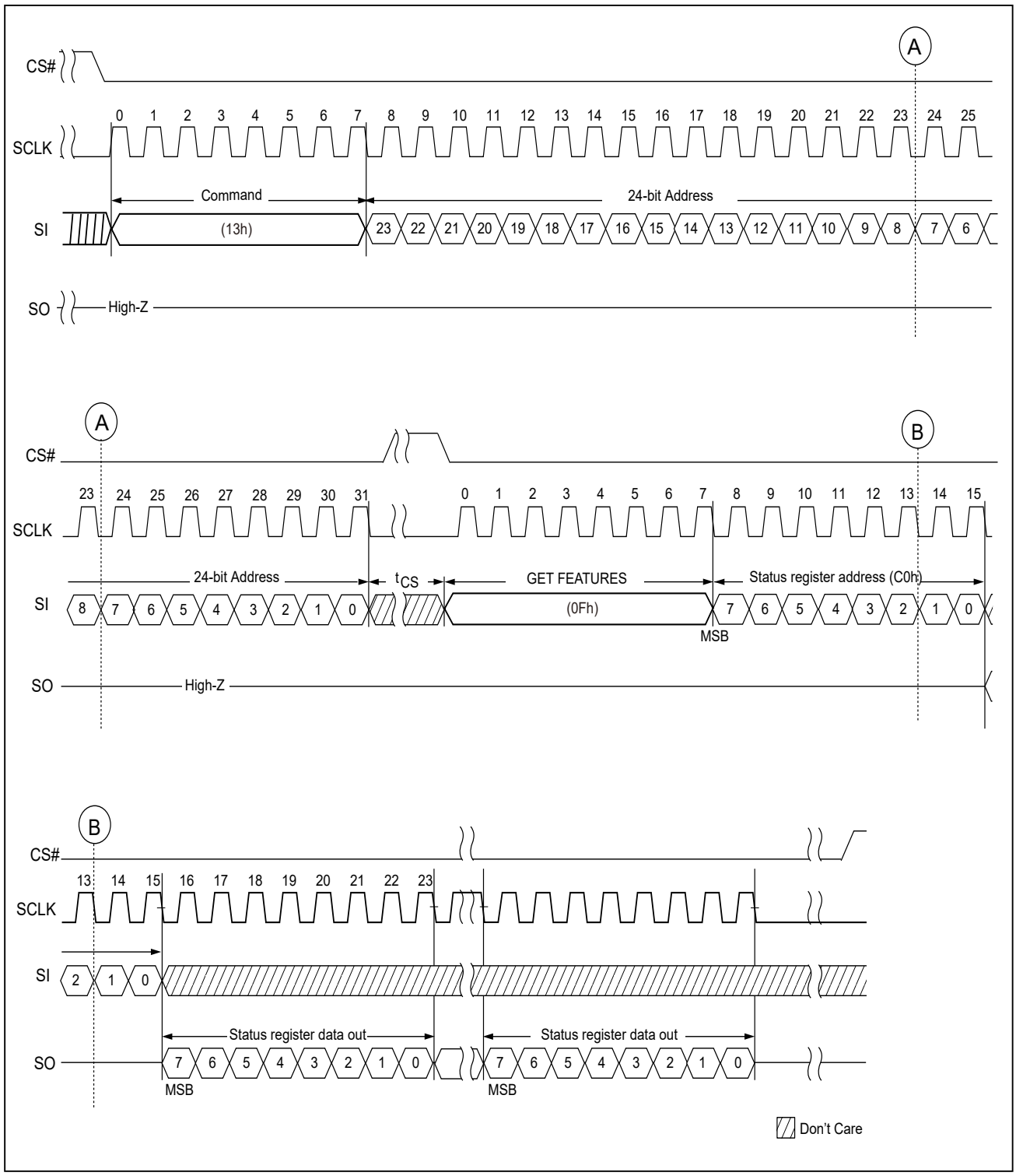
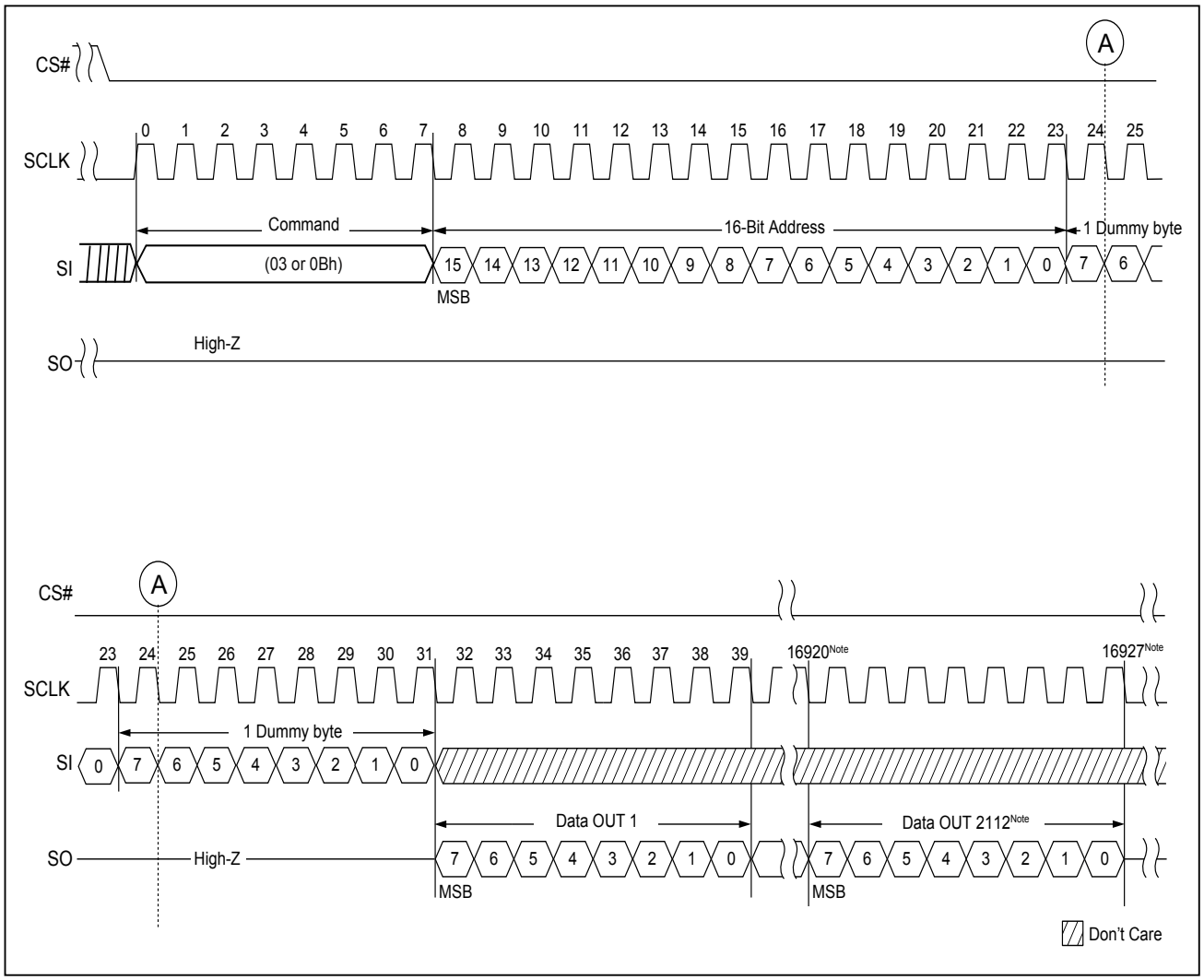
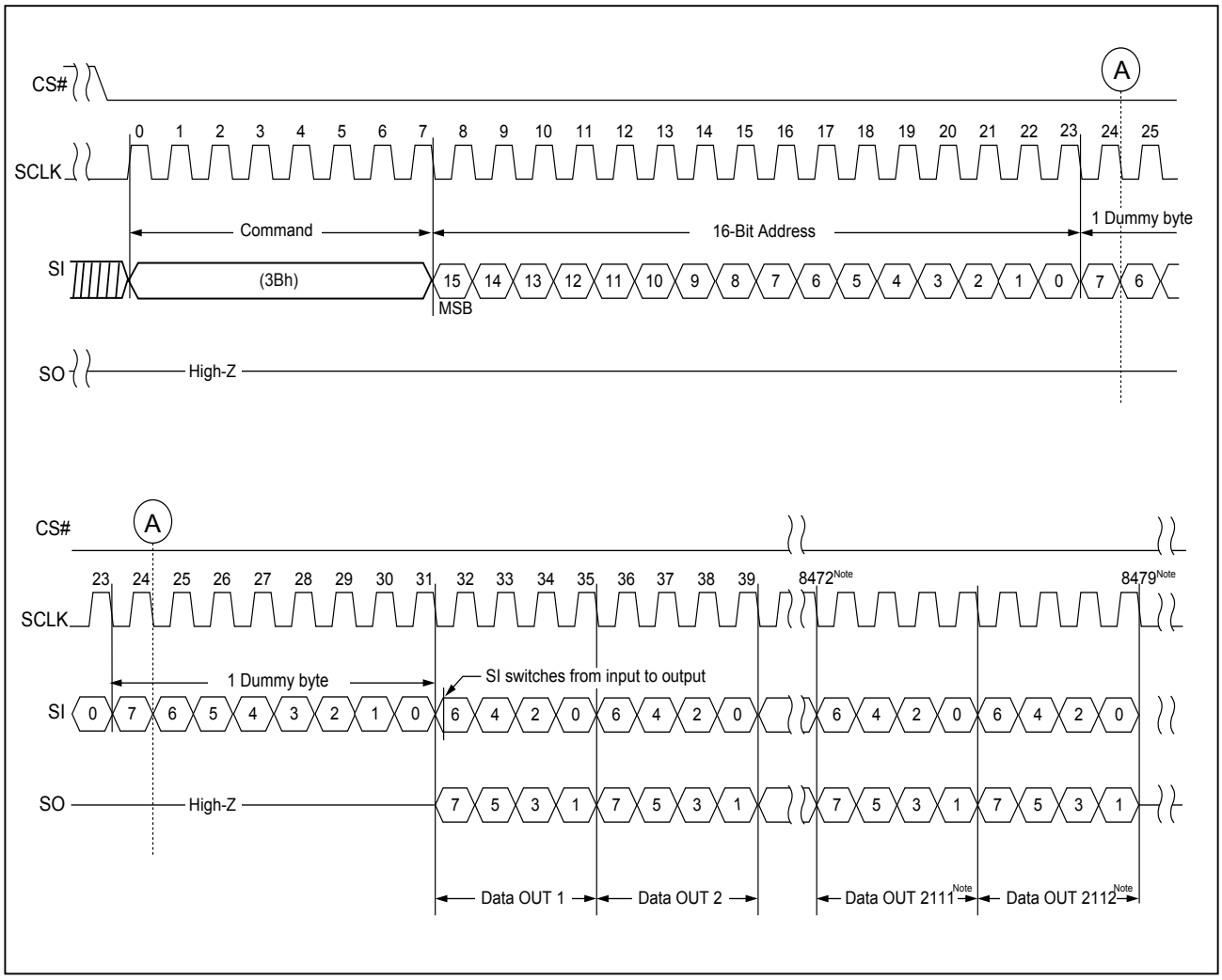


**Figure 10. READ From CACHE (03h or 0Bh) Timing**



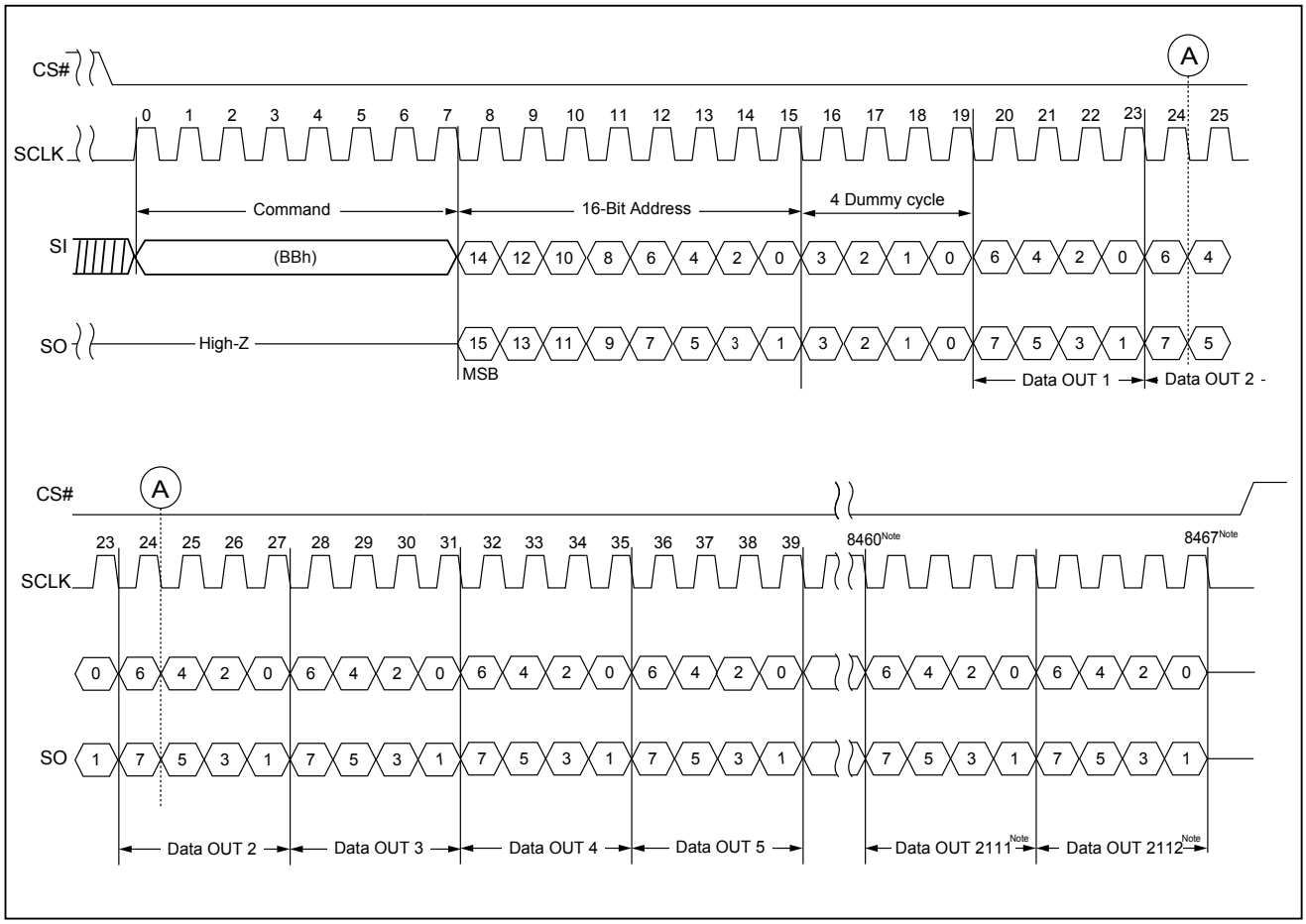

***Note:*** *2KB+64B as example.*

**Figure 11. READ FROM CACHE x 2**




***Note:*** *2KB+64B as example.*

**Figure 12. Read From Cache Dual IO 1-2-2**




***Note:*** *2KB+64B as example.*

**Figure 13. READ FROM CACHE x 4**

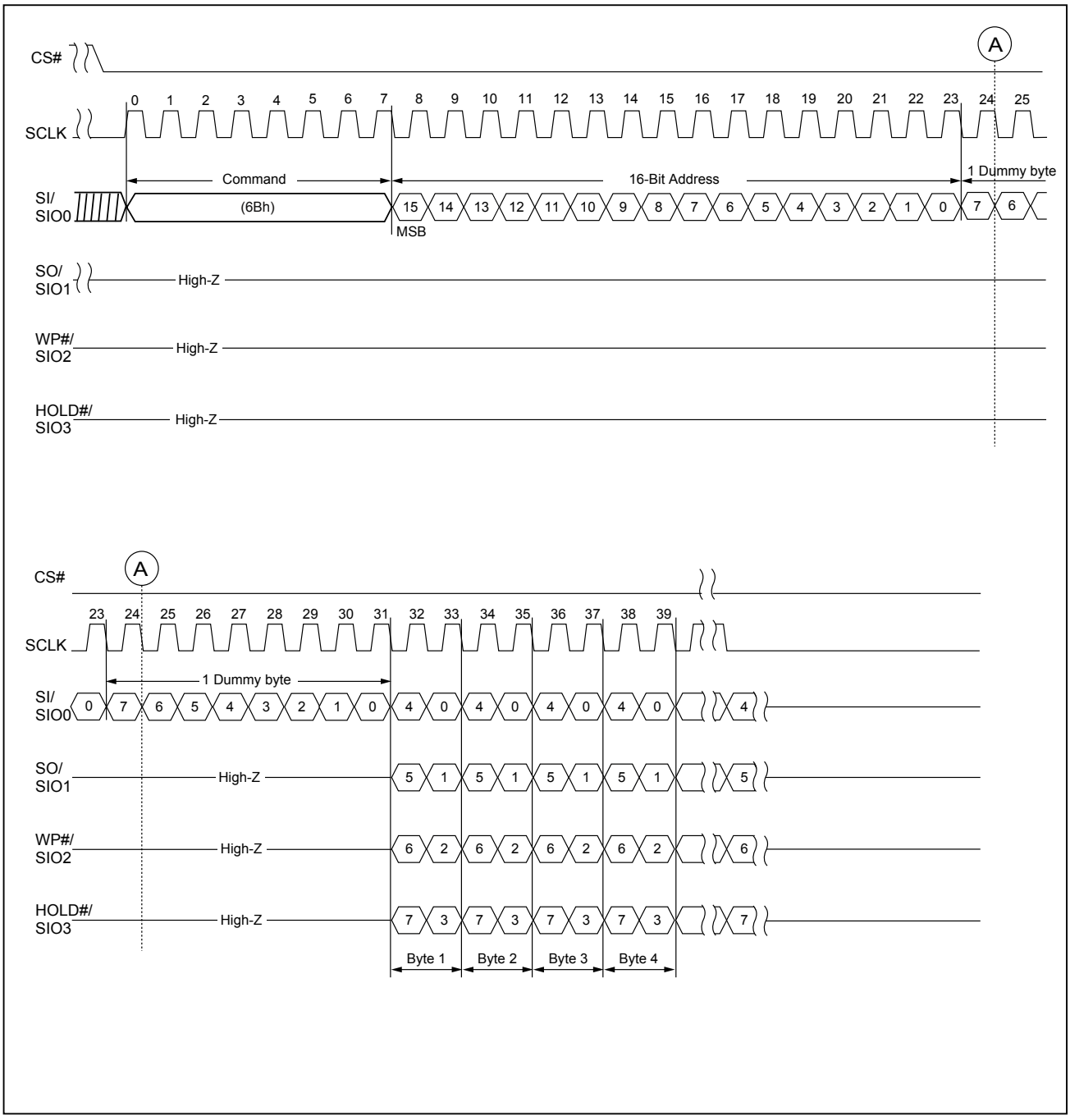
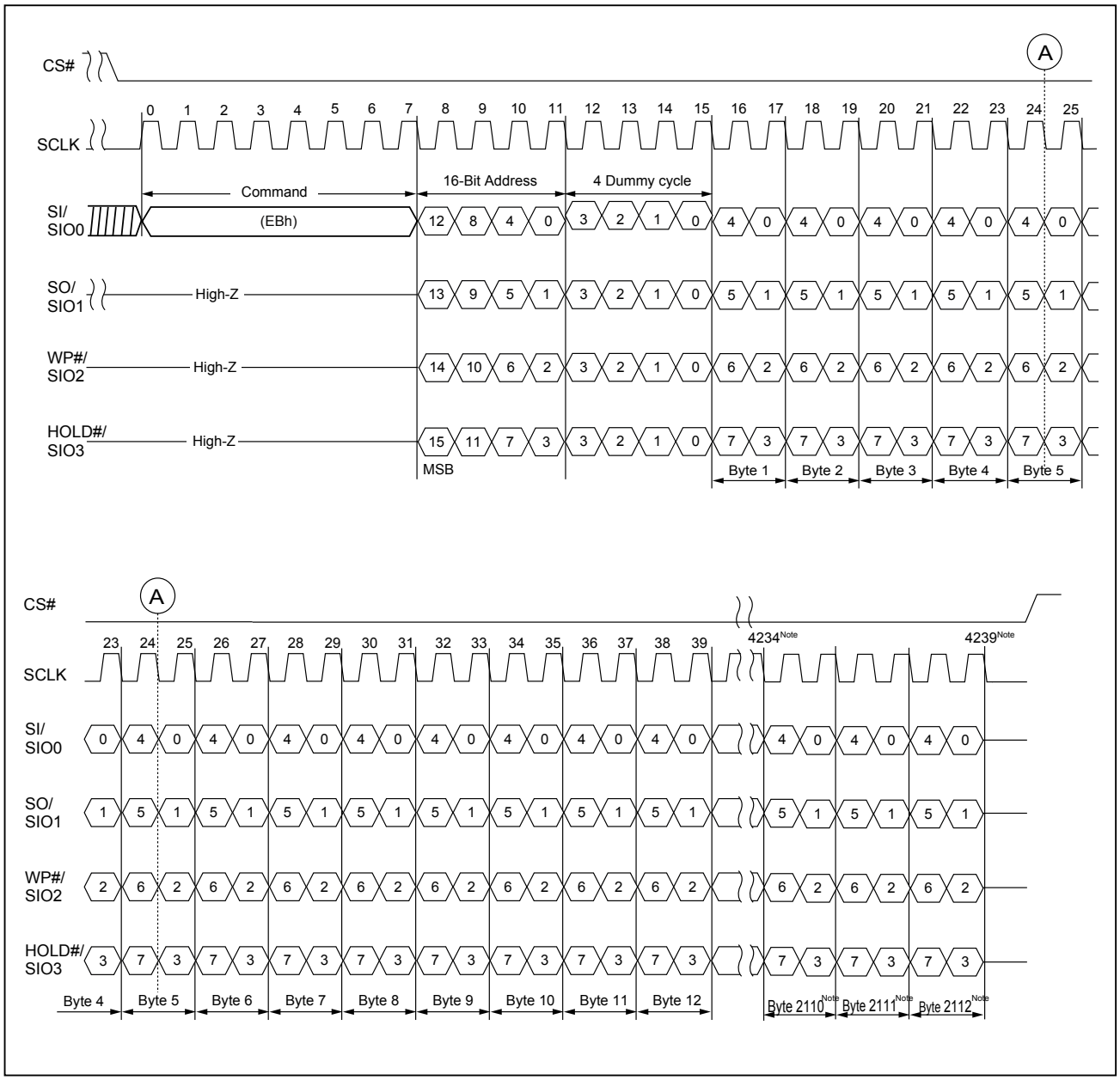


**Figure 14. Read From Cache Quad IO 1-4-4**




***Note:*** *2KB+64B as example.*

### 8-3-3. Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh)

The page read cache sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tRD to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 13h command and giving the 24-bit address, the device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) or 05h (RDSR) may be used to poll the operation status. After the status of successfully completed, following the page read cache sequential (31h) or the page read cache random (30h) command being sent to Serial Flash device; the Serial Flash device will be at a busy time of tRCBSY for the next page data transferring to cache. And then following the cache read command (03h/0Bh/3Bh/6Bh/BBh/EBh) may get the prior page data output from cache at the same time.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h or 30h command prior to the last data-out.

The PAGE READ CACHE SEQUENTIAL command is also valid for the consecutive page cross block.

**Figure 15. Page Read Cache Random (30h)**

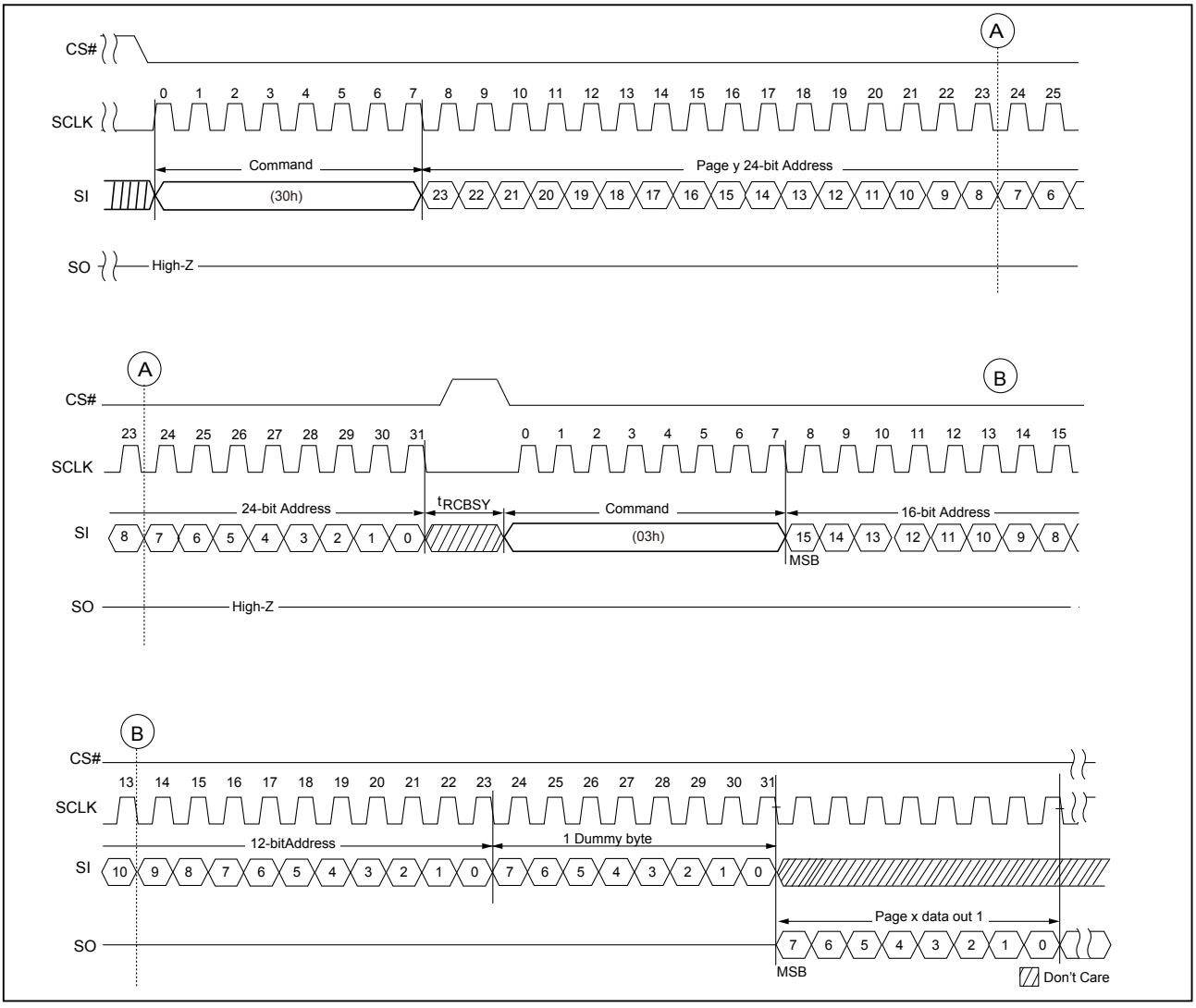


**Figure 16. Page Read Cache Sequential (31h)**

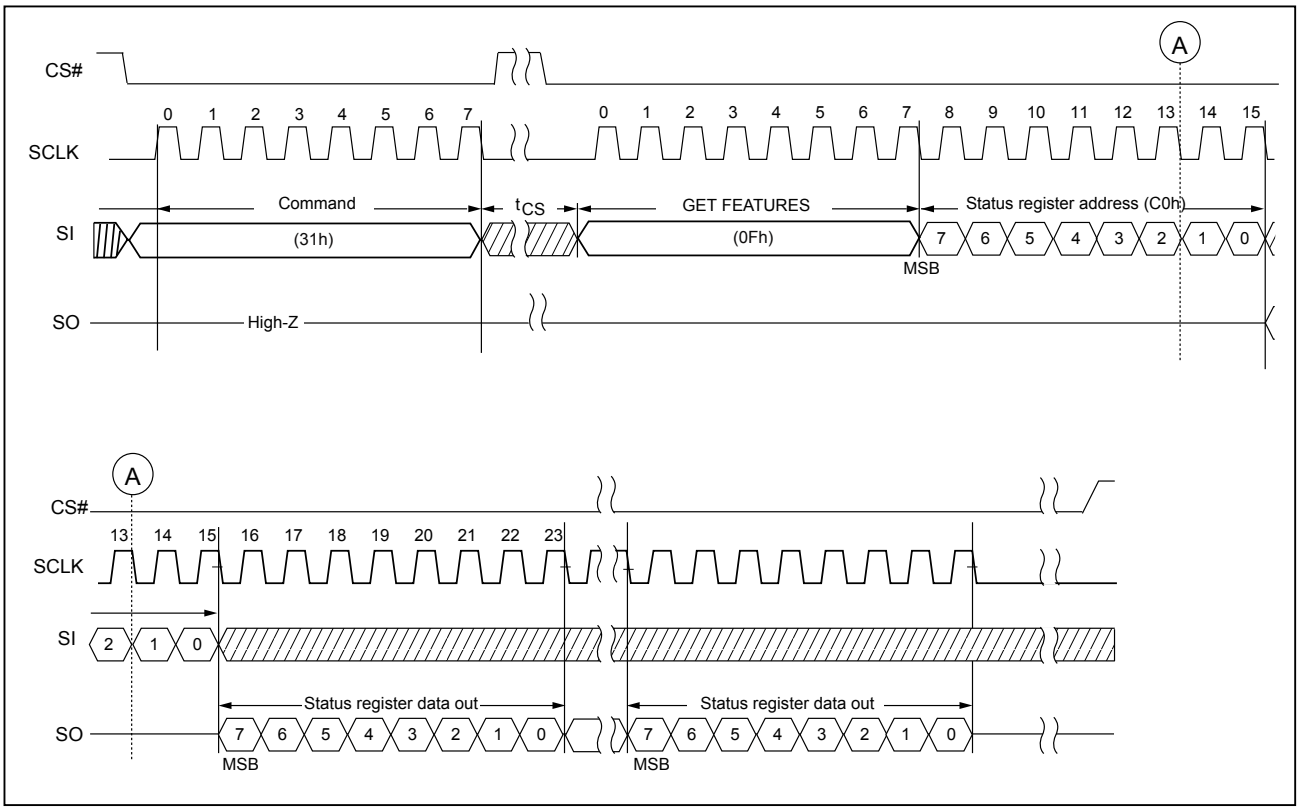


**Figure 17. Page Read Cache End (3Fh)**

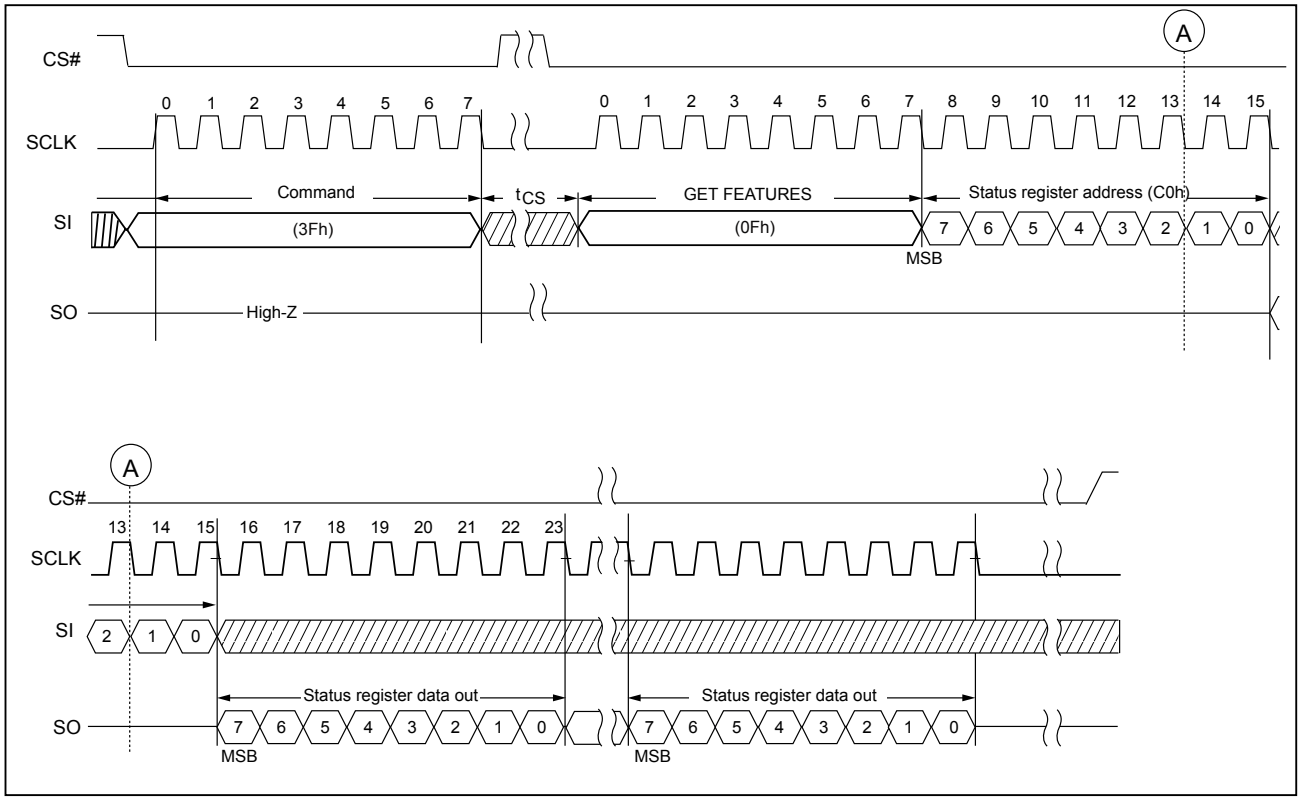
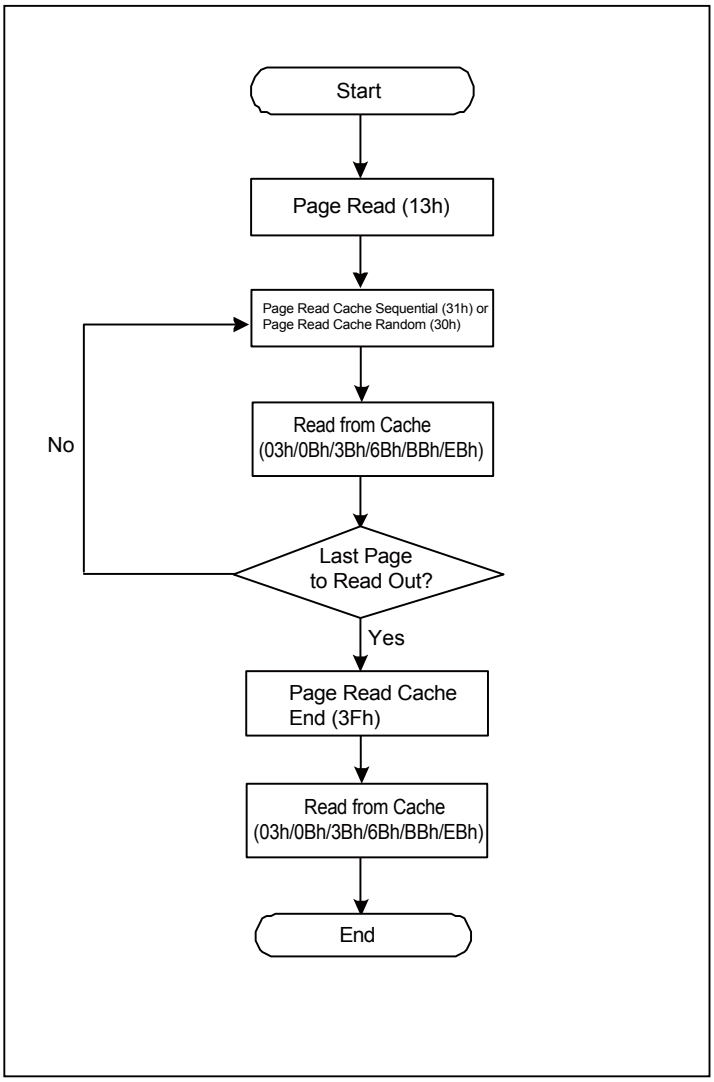


**Figure 18. Page Read Cache Flow**



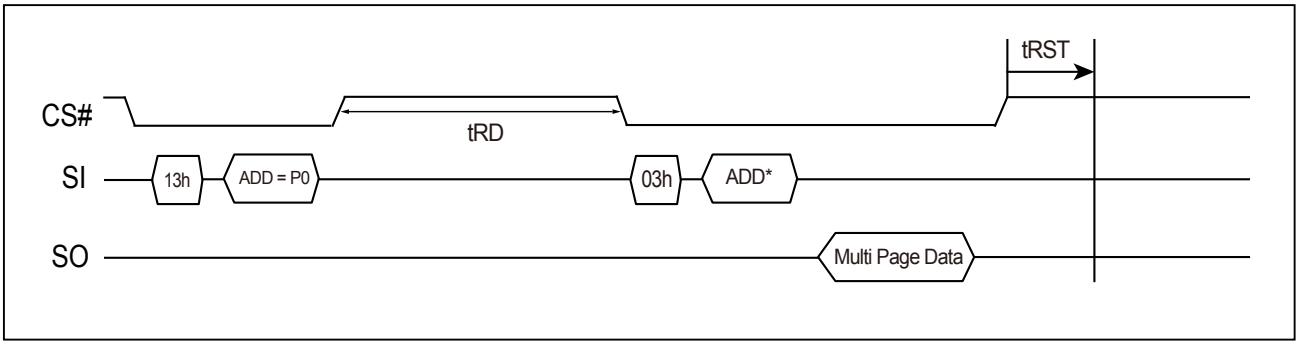
### 8-3-4. Continuous Read Operation

This device also supports the continuous read operation which allows the host to read out the data continuously from page to page with just first read latency.

The continuous read operation including: firstly, starting with the page read command and the 1st page data will be read into the cache after the read latency tRD. Secondly, Issuing the Read From Cache commands (03h/0Bh/3Bh/6Bh/BBh/EBh) to read out the data from cache continuously. After all the data is read out, the host should pullCS# high to terminate this continuous read operation and wait a 6us of tRST for the NAND device resets read operation.

The data output for each page will always start from byte 0 and a full page data (2KB) should be read out for each page.

**Figure 19. Continuous Read Waveform**




***: Address is Don't care.***

## Table 6. Command Set - Continuous Read Operation Enabled

SPI_NOR_EN = 0, **CONT = 1**

| Mode | 1st Byte | 2nd Byte | 3rd Byte | 4th Byte | 5th Byte | 6th Byte | 7th Byte | 8th Byte |
|---|---|---|---|---|---|---|---|---|
| **Get Feature** | 0Fh | ADD | Data | | | | | |
| **Read Status** | 05h | Data | | | | | | |
| **Set Feature** | 1Fh | ADD | Data | | | | | |
| **Page Read** | 13h | RADD2 | RADD1 | RADD0 | | | | |
| **Read From Cache x1** | 03h | DUMMY | DUMMY | DUMMY | DATA~ | | | |
| **Read From Cache x1 (Alternative)** | 0Bh | DUMMY | DUMMY | DUMMY | DATA~ | | | |
| **Read From Cache x2** | 3Bh | DUMMY | DUMMY | DUMMY | DATA~*2 | | | |
| **Read From Cache x4** | 6Bh | DUMMY | DUMMY | DUMMY | DATA~*4 | | | |
| **Read From Cache Dual IO 1-2-2** | BBh | DUMMY*2 | DUMMY*2 | DUMMY*2 | DATA~*2 | | | |
| **Read From Cache Quad IO 1-4-4** | EBh | DUMMY*4 | DUMMY*4 | DUMMY*4 | DUMMY*4 | DATA~*4 | | |
| **Read ID** | 9Fh | DUMMY | MID | DID1 | DID2 | | | |
| **Block Erase** | D8h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Execute** | 10h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Load x1** | 02h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load random Data x1** | 84h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load x4** | 32h | CADD1 | CADD0 | DATA~*4 | | | | |
| **Program Load Random Data x4** | 34h | CADD1 | CADD0 | DATA~*4 | | | | |
| **Write Enable** | 06h | | | | | | | |
| **Write Disable** | 04h | | | | | | | |
| **Reset** | FFh | | | | | | | |
| **Read ECCSR** | 7Ch | DUMMY | SR_ECC | | | | | |
| **Write BBM** | A1h | LBA | LBA | PBA | PBA | | | |
| **Read BBM**[*1] | A5h | DUMMY | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1~ |
| **ECC Warning Page Address** | A9h | DUMMY | RADD2_L | RADD1_L | RADD0_L | RADD2_F | RADD1_F | RADD0_F |

***Note:*** *Address is Don't Care for reach from cache command (03h/0Bh/3Bh/6Bh/BBh/EBh) in Continuous read operation.*

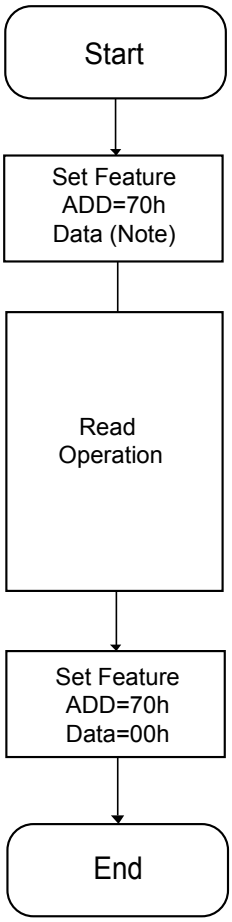
### 8-3-5. Special Read for Data Recovery

When the ECC fails to correct the data error of Serial Flash device, there's a special read for data recovery method which host executes the Special Read for Data Recovery operation and may recover the lost data again. After that, it is needed to move the data to another good block.

The Special Read for Data Recovery operation is enabled by Set Feature function (**"Table 7. Feature Settings"**).

There are 5 modes for the user to recover the lost data. The procedure of entering and exiting the operation is shown as Figure below.

**Figure 20. Procedure of Entering/Exiting the Special Read for Data Recovery operation**




***Note:*** *Please refer to the* **"Table 7. Feature Settings"**

**Table 7. Feature Settings**

| Definition | | SPEC_RD2 | SPEC_RD1 | SPEC_RD0 | Value |
|---|---|---|---|---|---|
| Special Read for Data Recovey | Disable (Default) | 0 | 0 | 0 | 00h |
| | Mode 1 | 0 | 0 | 1 | 01h |
| | Mode 2 | 0 | 1 | 0 | 02h |
| | Mode 3 | 0 | 1 | 1 | 03h |
| | Mode 4 | 1 | 0 | 0 | 04h |
| | Mode 5 | 1 | 0 | 1 | 05h |

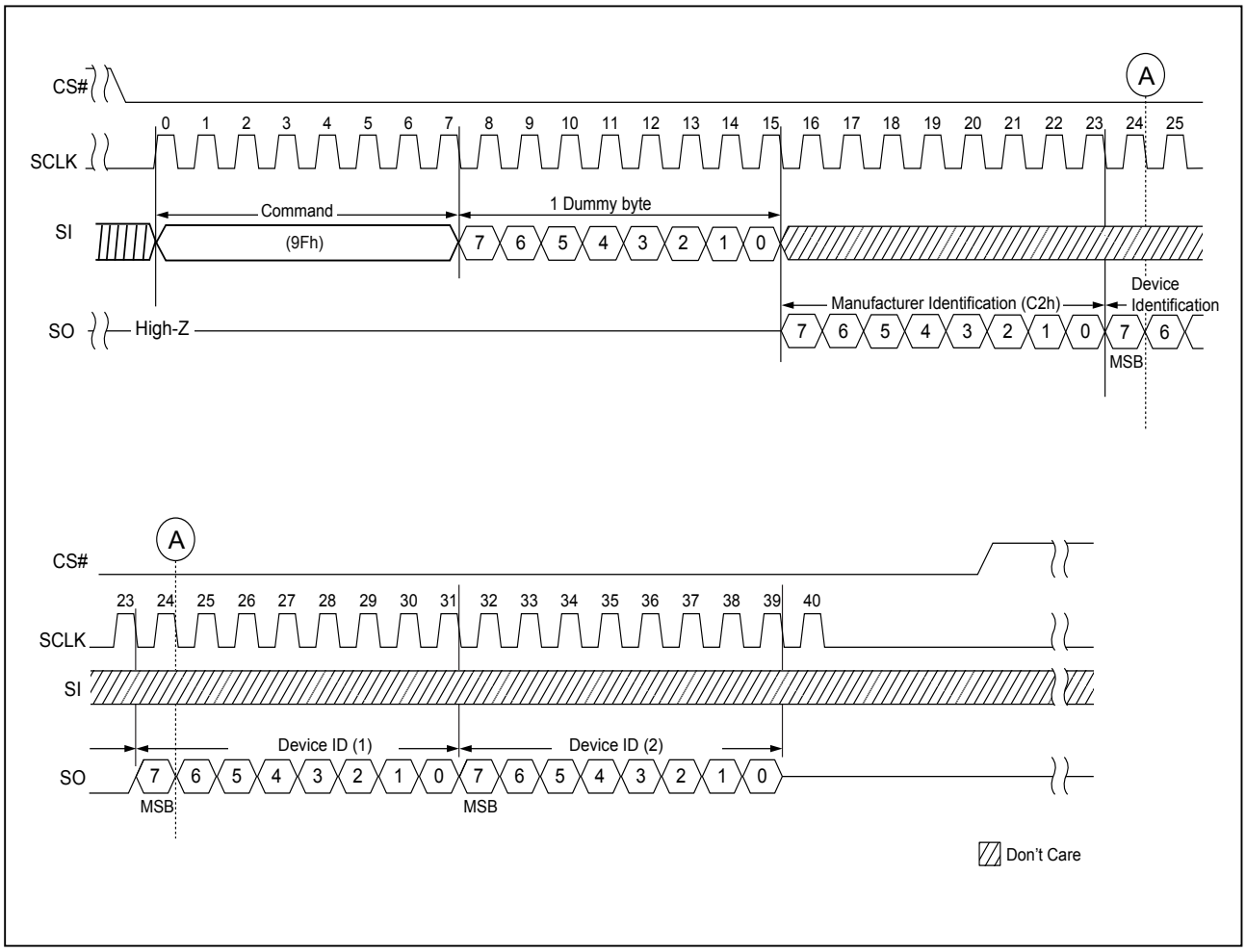
## 8-4. READ ID (9Fh)

The READ ID command is shown as the table below.

**Table 8. READ ID Table**

| Byte | Description | | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 | Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Byte 0 | Manufacturer ID (Macronix) | | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2h |
| Byte 1 | Device ID 1 | 1Gb | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 96h |
| | | 2Gb | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A6h |
| | | 4Gb | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7h |
| Byte 2 | Device ID 2 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03h |

**Figure 21. READ ID (9Fh) Timing**



## 8-5. Parameter Page

The parameter page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 01h address, issue 0Fh (GET FEATURE) with C0h feature address or 05h (RDSR) to poll the status of read completion. → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP feature (data byte = 00h) [exit parameter page read].

**Table 9. Parameter Page - MX35UF1GE4AD**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | Parameter Page Signature | | 4Fh, 4Eh, 46h, 49h |
| **4-5** | Revision Number | | 00h, 00h |
| **6-7** | Features Supported (N/A) | | 00h, 00h |
| **8-9** | Optional Commands Supported | | 06h, 00h |
| **10-31** | Reserved | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | Device Manufacturer (12 ASCII characters) | | 4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h |
| **44-63** | Device Model (20 ASCII Characters) | MX35UF1GE4AD | 4Dh, 58h, 33h, 35h, 55h, 46h, 31h, 47h, 45h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| **64** | Manufacturer ID | | C2h |
| **65-66** | Date Code | | 00h, 00h |
| **67-79** | Reserved | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 2048-byte | 00h, 08h, 00h, 00h |
| **84-85** | Number of Spare Bytes per Page | 128-byte | 80h, 00h |
| **86-89** | Number of Data Bytes per Partial Page | 512-byte | 00h, 02h, 00h, 00h |
| **90-91** | Number of Spare Bytes per Partial Page | 32-byte | 20h, 00h |
| **92-95** | Number of Pages per Block | | 40h, 00h, 00h, 00h |
| **96-99** | Number of Blocks per Unit | | 00h, 04h, 00h, 00h |
| **100** | Number of Logical Units | | 01h |
| **101** | Number of Address Cycles (N/A) | | 00h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per unit | | 14h, 00h |
| **105-106** | Block endurance | | 06h, 04h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 08h |
| **108-109** | Block endurance for guaranteed valid blocks | | 00h, 00h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partial Programming Attributes | | 00h |
| **112** | Number of ECC bits | | 00h |
| **113** | Number of Interleaved Address Bits (N/A) | | 00h |
| **114** | Interleaved Operation Attributes (N/A) | | 00h |
| **115-127** | Reserved | | 00h |

| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support (N/A) | | 00h, 00h |
| **131-132** | Program Cache Timing (N/A) | | 00h, 00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 760us | F8h, 02h |
| **135-136** | BE Maximum Block Erase time (uS) | 6000us | 70h, 17h |
| **137-138** | tRD_ECC Maximum Page Read time (uS) | 80us | 50h, 00h |
| **139-140** | tCCS Minimum (N/A) | 0ns | 00h, 00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h, 00h |
| **166** | Reserved | | 00h |
| **167** | Reliability enhancement function<br>2-7 Reserved(0)<br>1 1= Randomizer support, 0= Not support<br>0 1= Special read for data recovery support, 0= Not support | | 01h |
| **168** | NOR like features support<br>4-7: Reserved(0)<br>3 :1= XIP_RAM support, 0= Not support<br>2 :1= Automatic BBM support, 0= Not support<br>1 :1= Continuous Read support, 0= Not support<br>0 :1= BBM_table support, 0= Not support | | 03h |
| **169** | Number of special read for data recovery (N) | | 05h |
| **170-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **512-767** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **768+** | Additional Redundant Parameter Pages | | |

***Note***:
*The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*
$G(X) = X_{16} + X_{15} + X_2 + 1$

*The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.*

**Table 10. Parameter Page - MX35UF2GE4AD**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | Parameter Page Signature | | 4Fh, 4Eh, 46h, 49h |
| **4-5** | Revision Number | | 00h, 00h |
| **6-7** | Features Supported (N/A) | | 00h, 00h |
| **8-9** | Optional Commands Supported | | 06h, 00h |
| **10-31** | Reserved | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | Device Manufacturer (12 ASCII characters) | | 4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h |
| **44-63** | Device Model<br>(20 ASCII Characters) | MX35UF2GE4AD | 4Dh, 58h, 33h, 35h, 55h, 46h, 32h, 47h, 45h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| **64** | Manufacturer ID | | C2h |
| **65-66** | Date Code | | 00h, 00h |
| **67-79** | Reserved | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 2048-byte | 00h, 08h, 00h, 00h |
| **84-85** | Number of Spare Bytes per Page | 128-byte | 80h, 00h |
| **86-89** | Number of Data Bytes per Partial Page | 512-byte | 00h, 02h, 00h, 00h |
| **90-91** | Number of Spare Bytes per Partial Page | 32-byte | 20h, 00h |
| **92-95** | Number of Pages per Block | | 40h, 00h, 00h, 00h |
| **96-99** | Number of Blocks per Unit | | 00h, 08h, 00h, 00h |
| **100** | Number of Logical Units | | 01h |
| **101** | Number of Address Cycles (N/A) | | 00h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per unit | | 28h, 00h |
| **105-106** | Block endurance | | 06h, 04h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 08h |
| **108-109** | Block endurance for guaranteed valid blocks | | 00h, 00h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partial Programming Attributes | | 00h |
| **112** | Number of ECC bits | | 00h |
| **113** | Number of Interleaved Address Bits (N/A) | | 00h |
| **114** | Interleaved Operation Attributes (N/A) | | 00h |
| **115-127** | Reserved | | 00h |

| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support (N/A) | | 00h, 00h |
| **131-132** | Program Cache Timing (N/A) | | 00h, 00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 760us | F8h, 02h |
| **135-136** | BE Maximum Block Erase time (uS) | 6000us | 70h, 17h |
| **137-138** | tRD_ECC Maximum Page Read time (uS) | 80us | 50h, 00h |
| **139-140** | tCCS Minimum (N/A) | 0ns | 00h, 00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h, 00h |
| **166** | Reserved | | 00h |
| **167** | Reliability enhancement function<br>2-7 Reserved(0)<br>1 1= Randomizer support, 0= Not support<br>0 1= Special read for data recovery support, 0= Not support | | 01h |
| **168** | NOR like features support<br>4-7: Reserved(0)<br>3 :1= XIP_RAM support, 0= Not support<br>2 :1= Automatic BBM support, 0= Not support<br>1 :1= Continuous Read support, 0= Not support<br>0 :1= BBM_table support, 0= Not support | | 03h |
| **169** | Number of special read for data recovery (N) | | 05h |
| **170-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **512-767** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **768+** | Additional Redundant Parameter Pages | | |

***Note***:
*The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*
$G(X) = X_{16} + X_{15} + X_2 + 1$

*The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.*

**Table 11. Parameter Page - MX35UF4GE4AD**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | Parameter Page Signature | | 4Fh, 4Eh, 46h, 49h |
| **4-5** | Revision Number | | 00h, 00h |
| **6-7** | Features Supported (N/A) | | 00h, 00h |
| **8-9** | Optional Commands Supported | | 06h, 00h |
| **10-31** | Reserved | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | Device Manufacturer (12 ASCII characters) | | 4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h |
| **44-63** | Device Model<br>(20 ASCII Characters) | MX35UF4GE4AD | 4Dh, 58h, 33h, 35h, 55h, 46h, 34h, 47h, 45h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| **64** | Manufacturer ID | | C2h |
| **65-66** | Date Code | | 00h, 00h |
| **67-79** | Reserved | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 4096-byte | 00h, 10h, 00h, 00h |
| **84-85** | Number of Spare Bytes per Page | 256-byte | 00h, 01h |
| **86-89** | Number of Data Bytes per Partial Page | 1024-byte | 00h, 04h, 00h, 00h |
| **90-91** | Number of Spare Bytes per Partial Page | 64-byte | 40h, 00h |
| **92-95** | Number of Pages per Block | | 40h, 00h, 00h, 00h |
| **96-99** | Number of Blocks per Unit | | 00h, 08h, 00h, 00h |
| **100** | Number of Logical Units | | 01h |
| **101** | Number of Address Cycles (N/A) | | 00h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per unit | | 28h, 00h |
| **105-106** | Block endurance | | 06h, 04h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 08h |
| **108-109** | Block endurance for guaranteed valid blocks | | 00h, 00h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partial Programming Attributes | | 00h |
| **112** | Number of ECC bits | | 00h |
| **113** | Number of Interleaved Address Bits (N/A) | | 00h |
| **114** | Interleaved Operation Attributes (N/A) | | 00h |
| **115-127** | Reserved | | 00h |

| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support (N/A) | | 00h, 00h |
| **131-132** | Program Cache Timing (N/A) | | 00h, 00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 800us | 20h, 03h |
| **135-136** | BE Maximum Block Erase time (uS) | 6000us | 70h, 17h |
| **137-138** | tRD_ECC Maximum Page Read time (uS) | 110us | 6Eh, 00h |
| **139-140** | tCCS Minimum (N/A) | 0ns | 00h, 00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h, 00h |
| **166** | Reserved | | 00h |
| **167** | Reliability enhancement function<br>2-7 Reserved(0)<br>1 1= Randomizer support, 0= Not support<br>0 1= Special read for data recovery support, 0= Not support | | 01h |
| **168** | NOR like features support<br>4-7: Reserved(0)<br>3 :1= XIP_RAM support, 0= Not support<br>2 :1= Automatic BBM support, 0= Not support<br>1 :1= Continuous Read support, 0= Not support<br>0 :1= BBM_table support, 0= Not support | | 03h |
| **169** | Number of special read for data recovery (N) | | 05h |
| **170-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **512-767** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **768+** | Additional Redundant Parameter Pages | | |

***Note***:
*The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*
$G(X) = X_{16} + X_{15} + X_2 + 1$

*The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.*

## 8-6. UniqueID Page with PUF Type Code Structure

The UniqueID page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 00h address, issue 0Fh (GET FEATURE) with C0h feature address or 05h (RDSR) to poll the status of read completion → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP function (data byte = 00h) [exit unique ID read].

The MX35UFxGE4AD unique ID adopts Macronix PUF-like code structure, which is truly random and the numbers of "0" bit almost equal to numbers of "1" bit. The unique ID is 32-byte and with 16 copies for back-up purpose. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, host need to repeat the XOR with the next copy of Unique ID data.

## 8-7. Internal ECC Status

### 8-7-1. Internal ECC Enabled/Disabled

The internal ECC logic may detect 9-bit error and correct 8-bit error. The default state of the internal ECC is enabled. To enable/disable the internal ECC, it is operated by the Set Feature operation to enable internal ECC or disable the internal ECC, and then check the internal ECC state by Get Feature operation.

The internal ECC is enabled by using Set Feature command (1Fh) and followed by feature address (B0h) and then set Bit4( ECC enabled) as "1". To disable the internal ECC can be done by using the Set Feature command (1Fh) and followed by the feature address (B0h) and then set Bit4 (ECC enabled) as "0".

When the internal ECC is enabled, after the data transfer time (tRD) is completed, a Status Read operation is required to check any uncorrectable read error happened. Please refer to **"Table 20. Status Register Bit Descriptions"**.

The constraint of the internal ECC enabled operation:

- The ECC protection coverage: please refer to **"Table 12. The Distribution of ECC Segment and Spare Area - 1Gb/2Gb"**, **"Table 13. The Distribution of ECC Segment and Spare Area - 4Gb"** and **"Table 14. The Distribution of ECC Segment and Spare Area - 4Gb (Cont'd)"** below. Only the grey areas are under internal ECC protection when the internal ECC is enabled.
- The number of partial-page program is not 4 in an ECC segment, user needs to program main area and relative spare area (12B) at one program operation. For partial page program, although there are eight ECC segments (for 4Gb) and four ECC segments (for 1Gb/2Gb), user still needs to follow the NOP=4 page program condition.

**Table 12. The Distribution of ECC Segment and Spare Area - 1Gb/2Gb**

| Area | Main Area (0) | Main Area (1) | Main Area (2) | Main Area (3) | Spare(0) | | | Spare(1) | | | Spare(2) | | | Spare(3) | | | Spare2 (0) | Spare2 (1) | Spare2 (2) | Spare2 (3) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 | | | | |
| Addr. (Start) | 000h | 200h | 400h | 600h | 800h | 802h | 804h | 810h | 812h | 814h | 820h | 822h | 824h | 830h | 832h | 834h | 840h | 850h | 860h | 870h |
| Addr. (End) | 1FFh | 3FFh | 5FFh | 7FFh | 801h | 803h | 80Fh | 811h | 813h | 81Fh | 821h | 823h | 82Fh | 831h | 833h | 83Fh | 84Fh | 85Fh | 86Fh | 87Fh |
| Size | 512(B) | 512(B) | 512(B) | 512(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 16(B) | 16(B) | 16(B) | 16(B) |
| Data Type | User | User | User | User | R | User | User | R | User | User | R | User | User | R | User | User | ECC | ECC | ECC | ECC |

***Notes:*** *R1: Reserved*

*M2: Metadata 2*
*M1: Metadata 1*
*Grey area: Under ECC protection*

**Table 13. The Distribution of ECC Segment and Spare Area - 4Gb**

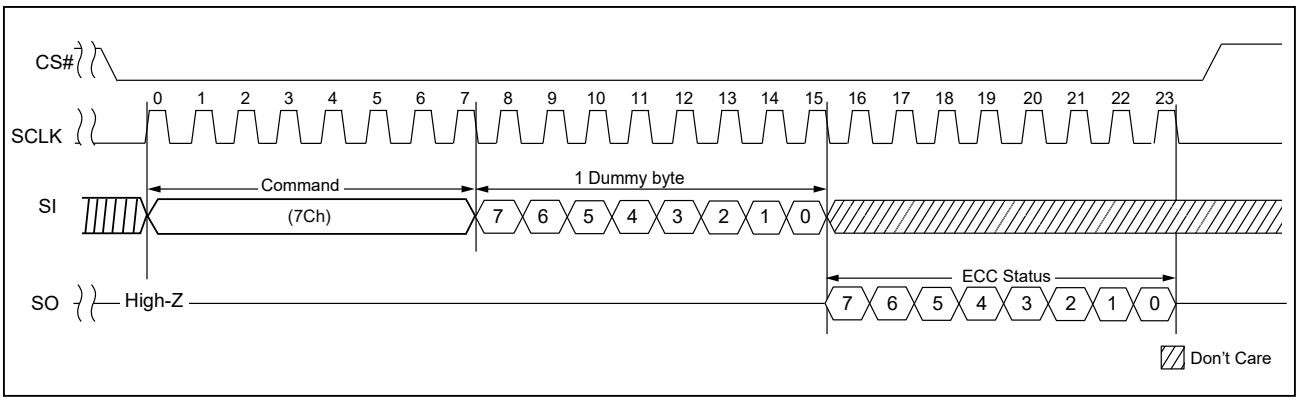
| Area | Main Area (0) | Main Area (1) | Main Area (2) | Main Area (3) | Main Area (4) | Main Area (5) | Main Area (6) | Main Area (7) | Spare(0) | | | Spare(1) | | | Spare(2) | | | Spare(3) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 |
| Addr. (Start) | 000h | 200h | 400h | 600h | 800h | A00h | C00h | E00h | 1000h | 1002h | 1004h | 1010h | 1012h | 1014h | 1020h | 1022h | 1024h | 1030h | 1032h | 1034h |
| Addr. (End) | 1FFh | 3FFh | 5FFh | 7FFh | 9FFh | BFFh | DFFh | FFFh | 1001h | 1003h | 100Fh | 1011h | 1013h | 101Fh | 1021h | 1023h | 102Fh | 1031h | 1033h | 103Fh |
| Size | 512(B) | 512(B) | 512(B) | 512(B) | 512(B) | 512(B) | 512(B) | 512(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) |
| Data Type | User | User | User | User | User | User | User | User | R | User | User | R | User | User | R | User | User | R | User | User |

**Table 14. The Distribution of ECC Segment and Spare Area - 4Gb (Cont'd)**

| Area | Spare(4) | | | Spare(5) | | | Spare(6) | | | Spare(7) | | | Spare2 (0) | Spare2 (1) | Spare2 (2) | Spare2 (3) | Spare2 (4) | Spare2 (5) | Spare2 (6) | Spare2 (7) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 | R1 | M2 | M1 | | | | | | | | |
| Addr. (Start) | 1040h | 1042h | 1044h | 1050h | 1052h | 1054h | 1060h | 1062h | 1064h | 1070h | 1072h | 1074h | 1080h | 1090h | 10A0h | 10B0h | 10C0h | 10D0h | 10E0h | 10F0h |
| Addr. (End) | 1041h | 1043h | 104Fh | 1051h | 1053h | 105Fh | 1061h | 1063h | 106Fh | 1071h | 1073h | 107Fh | 108Fh | 109Fh | 10AFh | 10BFh | 10CFh | 10DFh | 10EFh | 10FFh |
| Size | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 2(B) | 2(B) | 12(B) | 16(B) | 16(B) | 16(B) | 16(B) | 16(B) | 16(B) | 16(B) | 16(B) |
| Data Type | R | User | User | R | User | User | R | User | User | R | User | User | ECC | ECC | ECC | ECC | ECC | ECC | ECC | ECC |

### 8-7-2. Read ECCSR (7Ch) command for ECC Status Read

Besides the Get Feature( with feature address of C0h) may collect the internal ECC status; the 7Ch command may read out the error bits number for the worst segment of the page(s). This command reports two kinds of ECC status. The first kind is the ECC status for the current page, the second kind is the ECC status for the accumulated pages




| Error # | ECCSR[3:0] |
|---|---|
| 0 | 0000 |
| 1 | 0001 |
| 2 | 0010 |
| 3 | 0011 |
| 4 | 0100 |
| 5 | 0101 |
| 6 | 0110 |
| 7 | 0111 |
| 8 | 1000 |
| >8 | 1111 |

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| ECC Status for the accumulated pages | | | | ECC Status for the current page | | | |
| ECCSR[3] | ECCSR[2] | ECCSR[1] | ECCSR[0] | ECCSR[3] | ECCSR[2] | ECCSR[1] | ECCSR[0] |

## 8-8. Flexible ECC Bit Flip Threshold Setting & Read ECC Warning Page Address

Flexible ECC Bit Flip Threshold Setting: Host can set the ECC warning criterion by themselves. This Serial Flash offers “BFT[3:0]” for the user to set their own ECC warning criterion. The Chip will report the warning status when on the status feature bits ECC_S[1:0] error bit number is larger or equal to the BFT.

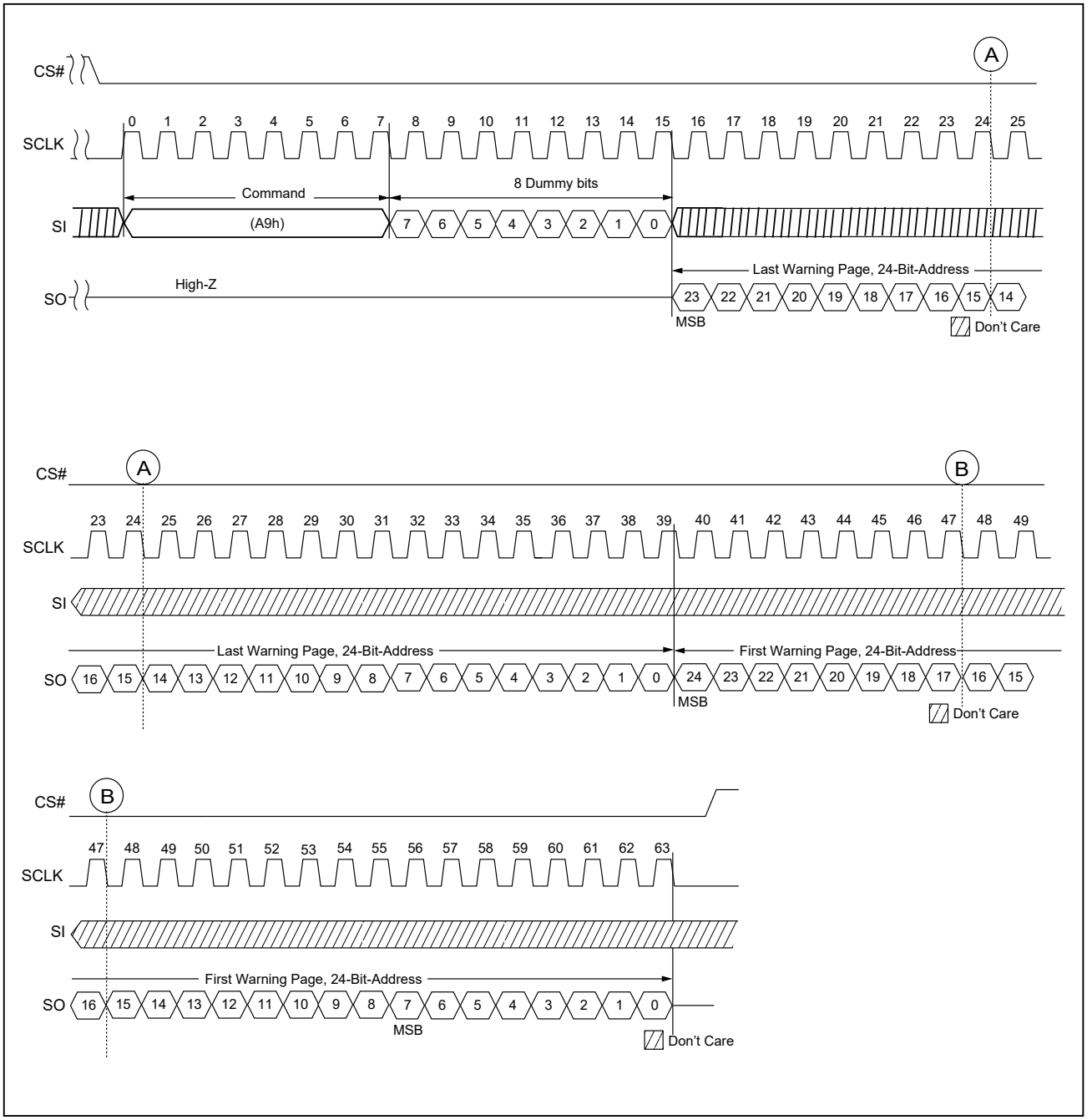
**Table 15. Flexible ECC Bit Flip Threshold Setting & Read ECC Warning Page Address**

| ADD | Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|---|---|---|---|---|---|---|---|---|---|---|
| 10h | Configuration | BFT3 | BFT2 | BFT1 | BFT0 | | | | ENPGM | F0h |

| BFT[3:0] | |
|---|---|
| 0000 | Detect uncorreted error |
| 0001 | Detect ≥1 bit error |
| 0010 | Detect ≥2 bit error |
| 0011 | Detect ≥3 bit error |
| 0100 | Detect ≥4 bit error |
| 0101 | Detect ≥5 bit error |
| 0110 | Detect ≥6 bit error (suggestion) |
| 0111 | Detect ≥7 bit error |
| 1000 | Detect ≥8 bit error |
| 1001 | Detect uncorrected error |
| 1010 | Detect uncorrected error |
| 1011 | Detect uncorrected error |
| 1100 | Detect uncorrected error |
| 1101 | Detect uncorrected error |
| 1110 | Detect uncorrected error |
| 1111 | Detect uncorrected error (default) |

Read ECC warning page address: Host can get the 1st and last page addresses which reaches the ECC warning criterion. During continuous read operation, the chip will record the 1st and last page address with error bit number is larger or equal to BFT[3:0] . Host can issue the “Read ECC warning Page address” command to read out these two page addresses

**Figure 22. ECC Warning Timing**



## 8-9. Program Operations

### 8-9-1. PAGE PROGRAM

With following operation sequences, the PAGE PROGRAM operation programs the page from byte 1 to byte 4224 (4Gb) and byte 1 to byte 2112 (1Gb/2Gb).

WRITE ENABLE (06h) → PROGRAM LOAD (02h) → PROGRAM LOAD RANDOM DATA (84h) if needed → PROGRAM EXECUTE (10h) → GET FEATUR from command to read status (0Fh) or RDSR (05h).

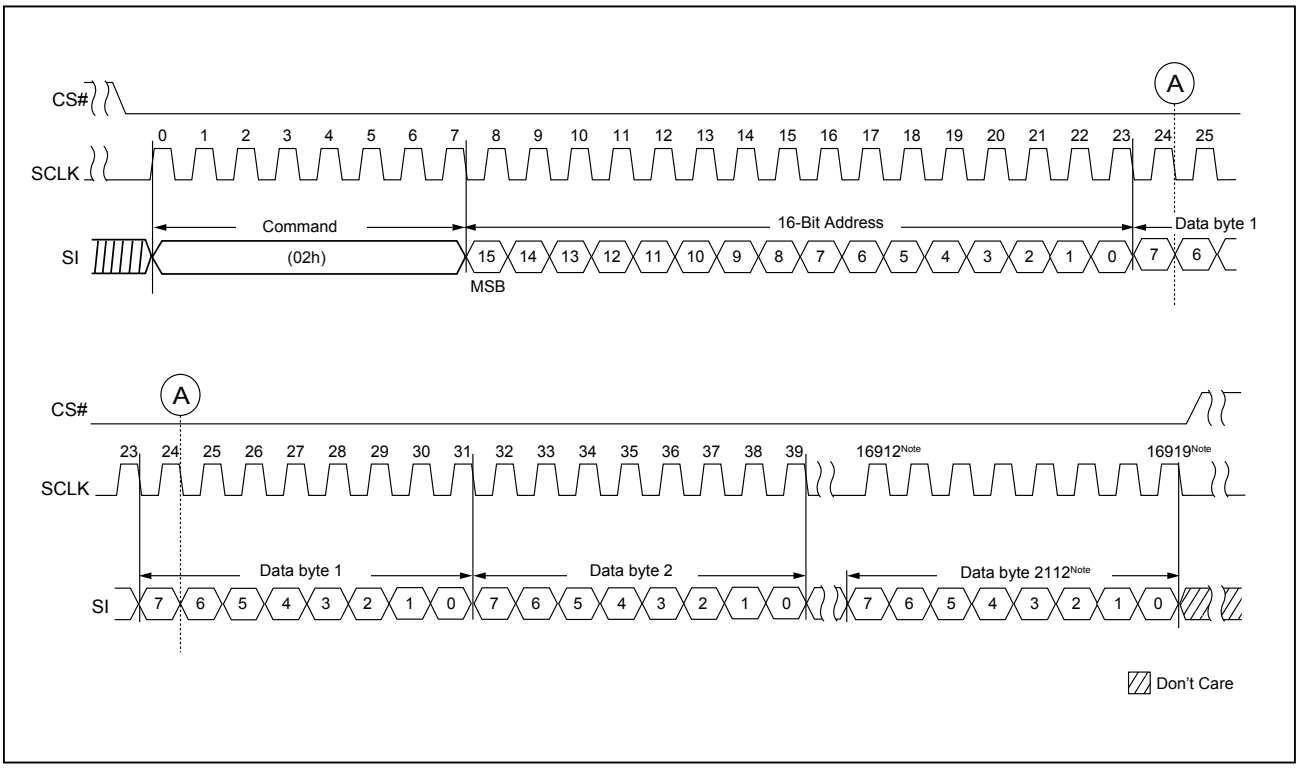
WEL bit is set with the WRITE ENABLE (06h) issued. The program operation will be ignored if 06h command not issued. In a single page, four partial page programs are allowed. Exceeded bytes (Page address is larger than 4224(4Gb) or 2112(1Gb/2Gb) for "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA", the exceeding bytes will be ignored. When CS goes high, the "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA" operation" terminates. Please note the figure below for PROGRAM LOAD.

After PROGRAM LOAD is done, the programming of data should be as following steps: issue 10h (PROGRAM EXECUTE) with 1byte command code, 24 bits address → code programming to memory and busy for tPROG → Program complete.

During programming, status to be polled by the status register.

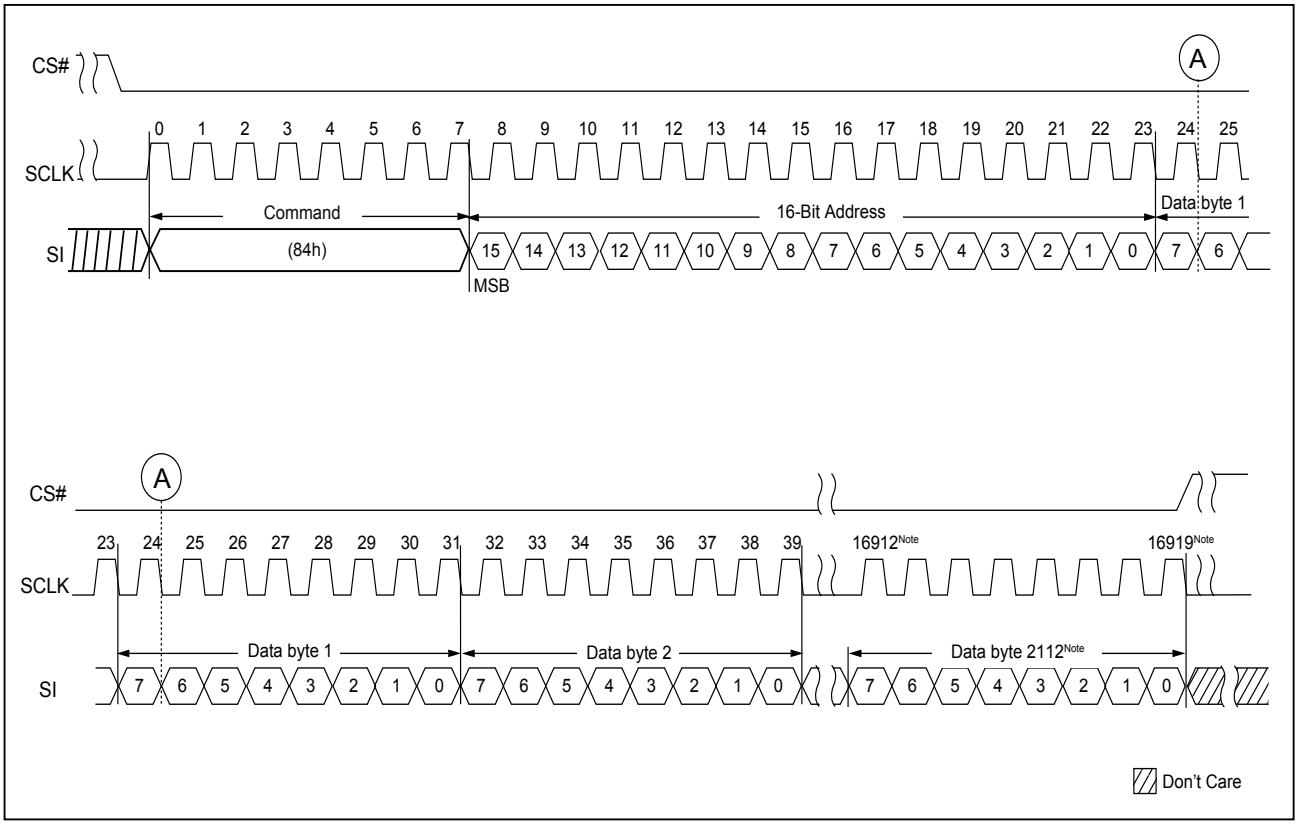
Operation shows in the Figure below.

**Figure 23. PROGRAM LOAD (02h) Timing**




***Note:*** *2KB+64B as example.*

**Figure 24. PROGRAM LOAD RANDOM DATA (84h) Timing**

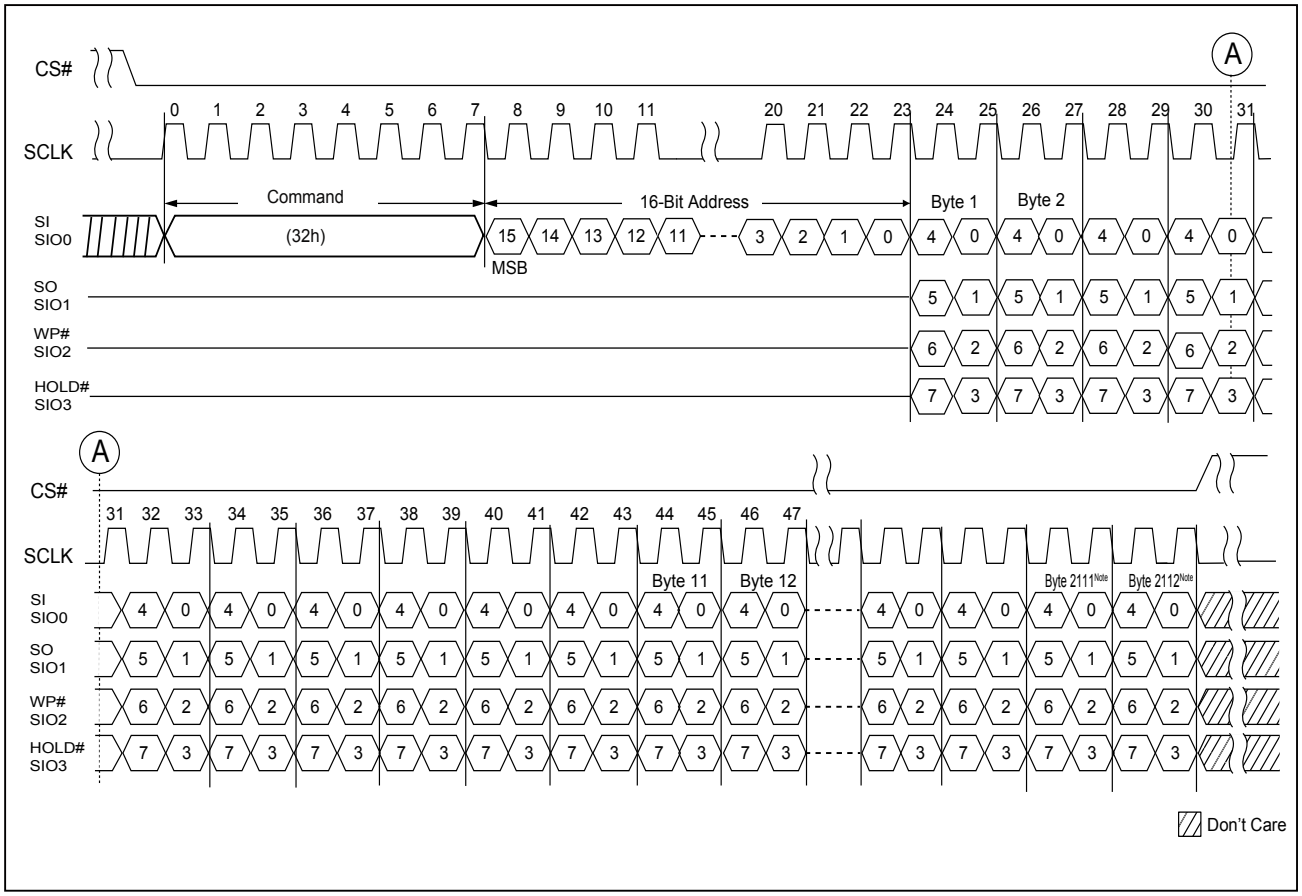



***Note:*** *2KB+64B as example.*

### 8-9-2. QUAD IO PAGE PROGRAM

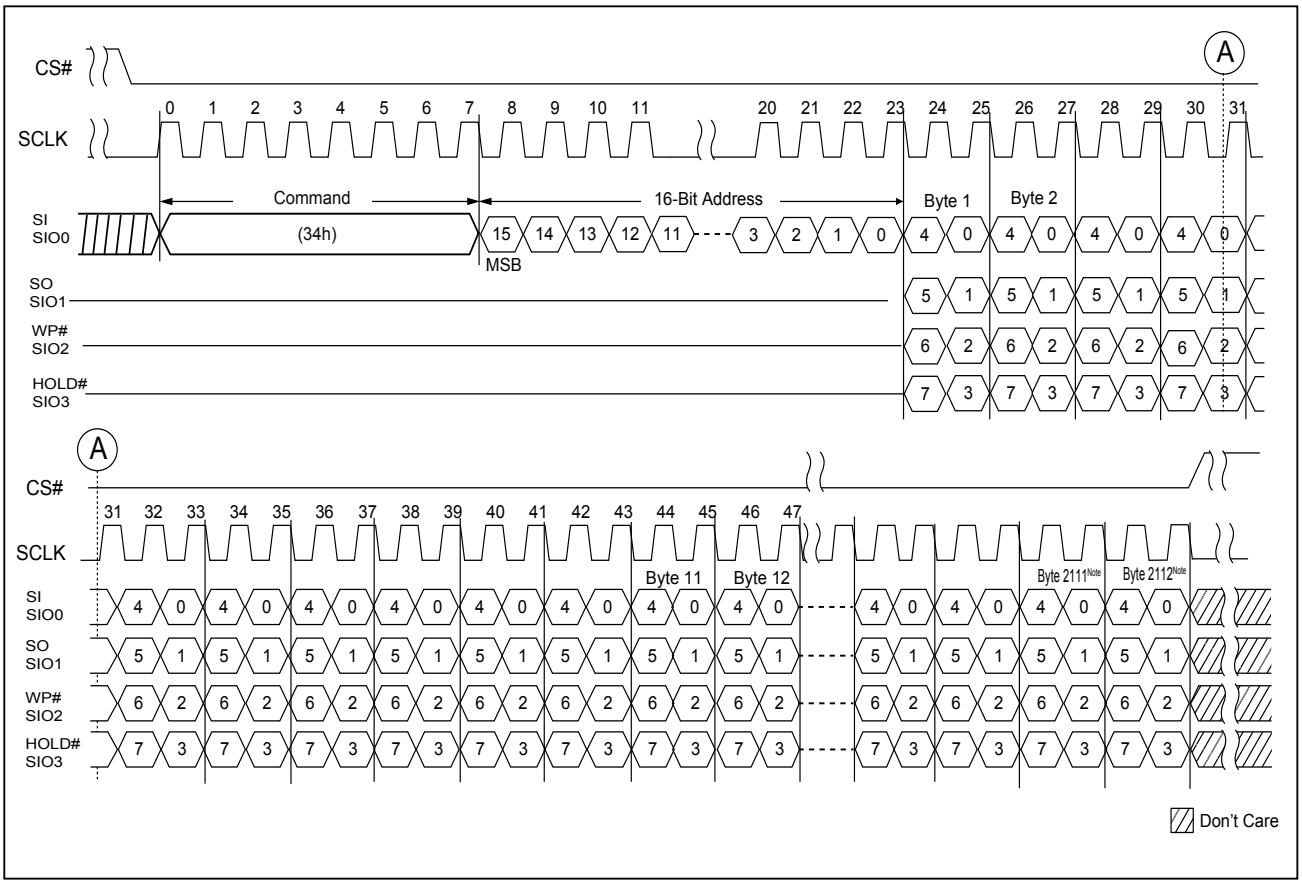
QUAD IO PAGE PROGRAM conducts the 4KB(for 4Gb) and 2KB(for 1Gb/2Gb) program with 4 I/O mode. The steps are: WRITE ENABLE (06h) → PROGRAM LOAD X4 (32h) → PROGRAM LOAD RANDOM DATA (34h) if needed → PROGRAM EXECUTE (10h) → Poll status by issuing GET FEATURE (0Fh) or RDSR (05h).

**Figure 25. PROGRAM LOAD X4 (32h) Timing**



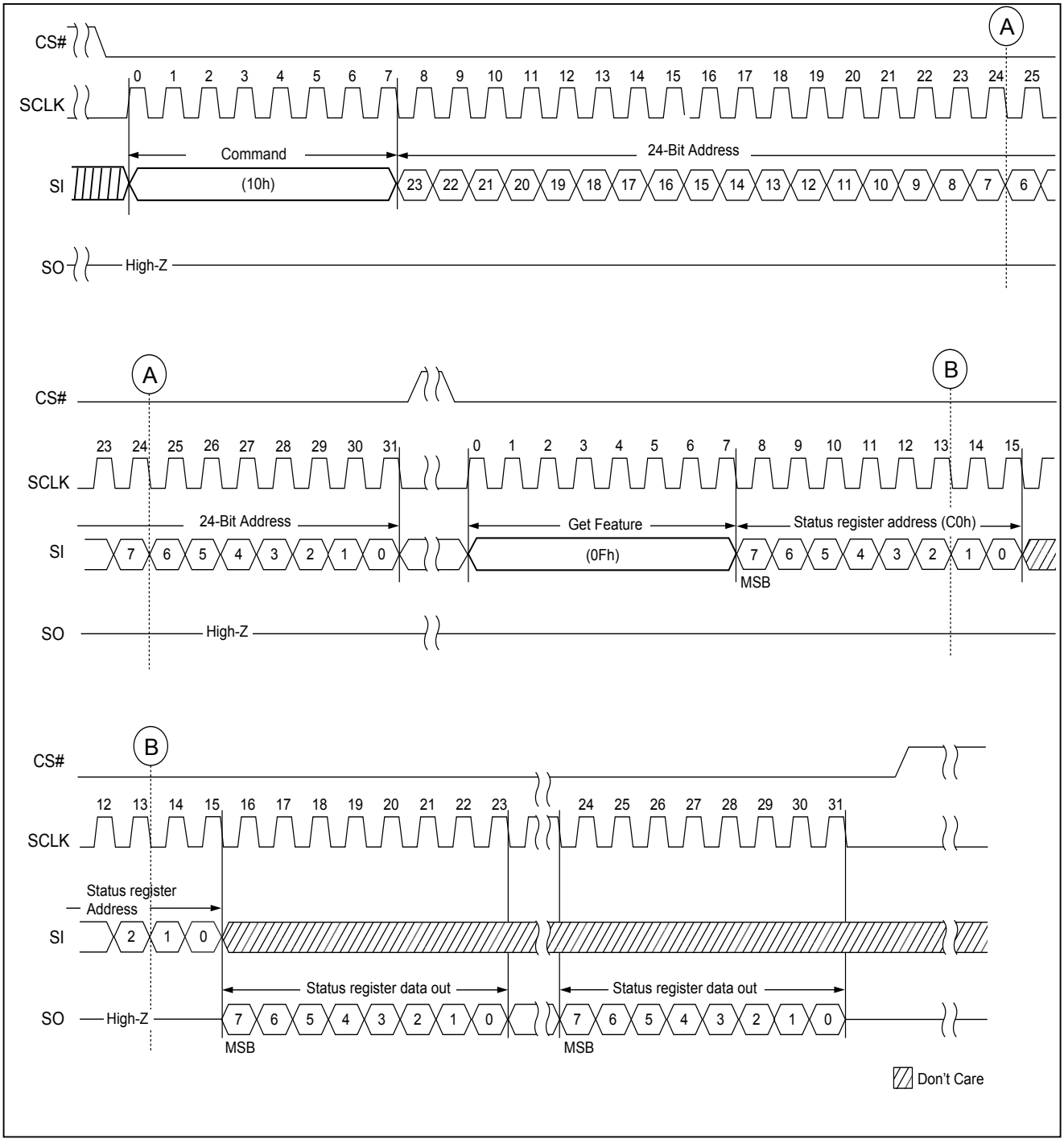

***Note:*** *2KB+64B as example.*

**Figure 26. QUAD IO PROGRAM RANDOM INPUT (34h) Timing**




***Note:*** *2KB+64B as example.*

**Figure 27. PROGRAM EXECUTE (10h) Timing**



## 8-10. BLOCK OPERATIONS

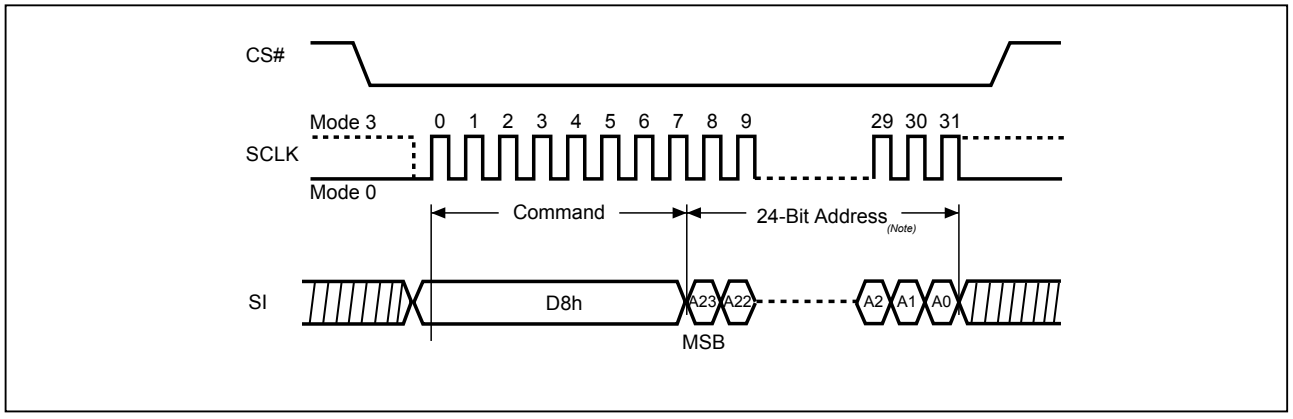
### Block Erase (D8h)

The Block Erase (D8h) instruction is for erasing the data of the chosen block to be "1". The instruction is used for a block of 256KB(for 4Gb) or 128KB(for 1Gb/2Gb) erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (D8h). Any address of the block is a valid address for Block Erase (D8h) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed. Finally, a Get Feature(0Fh) or RDSR (05h) instruction to check the status is necessary.

The sequence of issuing Block Erase instruction is: CS# goes low→ send Block Erase instruction code→ 24-bit address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Get Feature (0Fh) instruction with Address (C0h) or RDSR (05h) may check the status of the operation during the Block Erase cycle is in progress (please refer to the waveform **"Figure 7. GET FEATURE (0Fh) Timing"** and **"Table 7. Feature Settings"**). The OIP bit is "1" during the tBE timing, and is cleared to "0" when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

**Figure 28. Block Erase (BE) Sequence**




***Note:*** *The 24-bit Address includes: 17-bit row address and 7-bit dummy (for 2Gb/4Gb), or 16-bit row address and 8-bit dummy (for 1Gb).*

# 9. SPI NOR Compatible Command

Considering some SoC(or MCU) of host system must adopt the read protocol of SPI NOR like, this device provide the SPI_NOR_EN of configuration register bit to enable the read protocol of SPI NOR like for Read From Cache commands. The SPI_NOR_EN bit is OTP type once it is enable and cannot disable.

It is recommended to set the SPI_NOR_EN bit by programmer machine in advance before power on while attempts to adopt the read protocol of SPI NOR like.

Please refer to **"Figure 33. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)"**.

**Table 16. Command Set - SPI NOR Like Protocol Enabled**

(SPI_NOR_EN = 1, CONT=0)

| Mode | 1st Byte | 2nd Byte | 3rd Byte | 4th Byte | 5th Byte | 6th Byte | 7th Byte | 8th Byte |
|---|---|---|---|---|---|---|---|---|
| **Get Feature** | 0Fh | ADD | **Data** | | | | | |
| **Read Status** | 05h | Data | | | | | | |
| **Set Feature** | 1Fh | ADD | Data | | | | | |
| **Page Read** | 13h | RADD2 | RADD1 | RADD0 | | | | |
| **Page Read Cache Random** | 30h | RADD2 | RADD1 | RADD0 | | | | |
| **Page Read Cache Sequential** | 31h | | | | | | | |
| **Page Read Cache End** | 3Fh | | | | | | | |
| **Read From Cache x1** | 03h | DUMMY | CADD1 | CADD0 | DATA~ | | | |
| **Read From Cache x1 (Alternative)** | 0Bh | DUMMY | CADD1 | CADD0 | DUMMY | DATA~ | | |
| **Read From Cache x2**[Note3] | 3Bh | CADD1 | CADD0 | DUMMY | DATA~[*2] | | | |
| **Read From Cache x4**[Note3] | 6Bh | CADD1 | CADD0 | DUMMY | DATA~[*4] | | | |
| **Read From Cache Dual IO 1-2-2**[Note3] | BBh | CADD1[*2] | CADD0[*2] | DUMMY[*2] | DATA~[*2] | | | |
| **Read From Cache Quad IO 1-4-4**[Note3] | EBh | CADD1[*4] | CADD0[*4] | DUMMY[*4] | DUMMY[*4] | DATA~[*4] | | |
| **Read ID** | 9Fh | DUMMY | MID | DID1 | DID2 | | | |
| **Block Erase** | D8h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Execute** | 10h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Load x1** | 02h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load Random Data x1** | 84h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load x4**[Note3] | 32h | CADD1 | CADD0 | DATA~[*4] | | | | |
| **Program Load Random Data x4**[Note3] | 34h | CADD1 | CADD0 | DATA~[*4] | | | | |
| **Write Enable** | 06h | | | | | | | |
| **Write Disable** | 04h | | | | | | | |
| **Reset** | FFh | | | | | | | |
| **Read ECCSR** | 7Ch | DUMMY | SR_ECC | | | | | |
| **Write BBM** | A1h | LBA | LBA | PBA | PBA | | | |
| **Read BBM**[Note1] | A5h | DUMMY | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1~ |
| **ECC Warning Page Address**[Note2] | A9h | DUMMY | RADD2_L | RADD1_L | RADD0_L | RADD2_F | RADD1_F | RADD0_F |

***Notes:*** *1. A5h command may read the 40 links of BBM_table (LBAx/PBAx)*
*2. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address*
*3. *2 stands for the dual I/O phase and *4 for quad I/O mode.*

**Table 17. Command Set - SPI NOR Like Protocol Enabled & Continuous Read Operation**

(**SPI_NOR_EN = 1**, **CONT=1**)

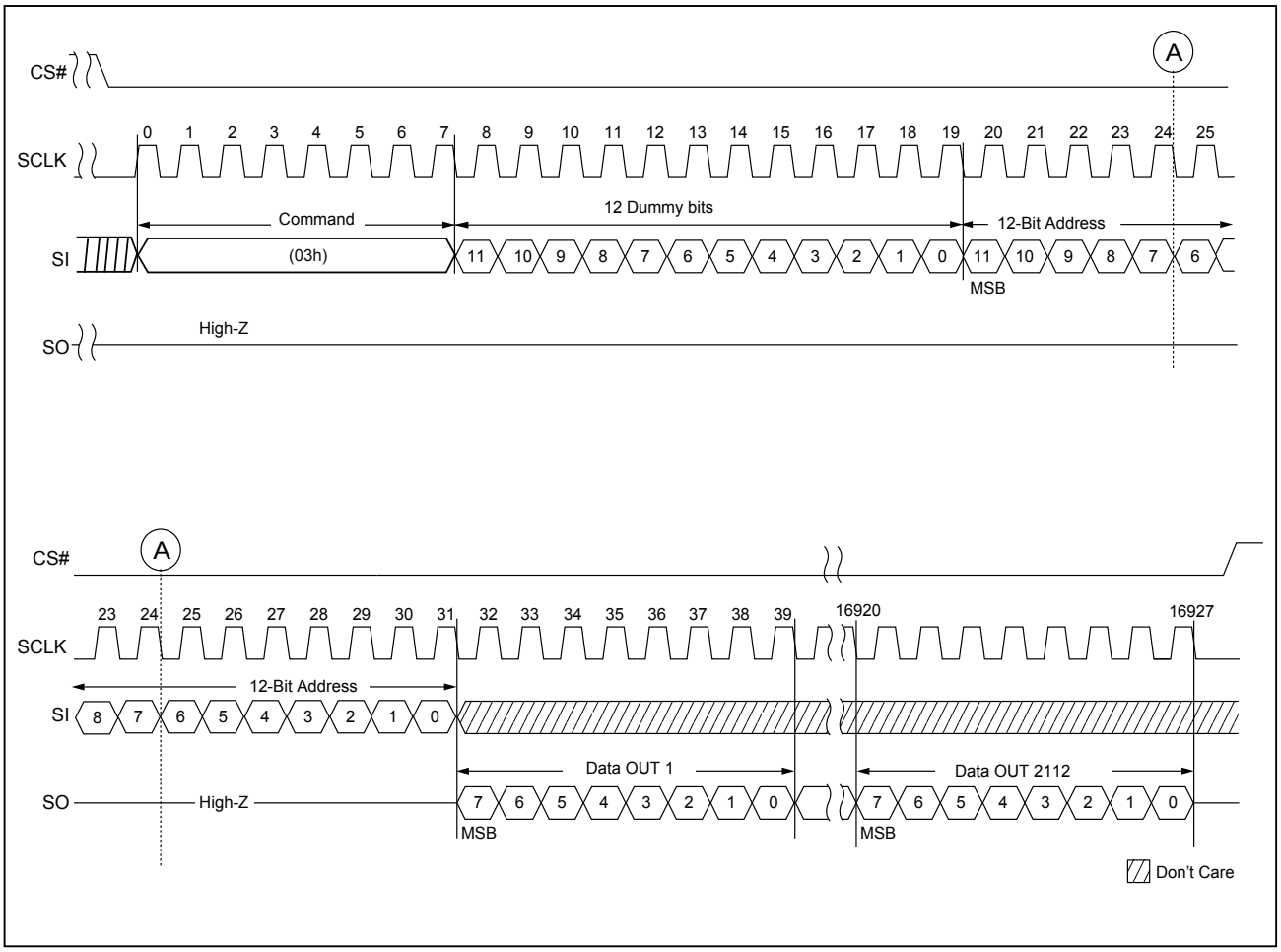
| Mode | 1st Byte | 2nd Byte | 3rd Byte | 4th Byte | 5th Byte | 6th Byte | 7th Byte | 8th Byte |
|---|---|---|---|---|---|---|---|---|
| **Get Feature** | 0Fh | ADD | Data | | | | | |
| **Read Status** | 05h | Data | | | | | | |
| **Set Feature** | 1Fh | ADD | Data | | | | | |
| **Page Read** | 13h | RADD2 | RADD1 | RADD0 | | | | |
| **Read From Cache x1** | 03h | DUMMY | DUMMY | DUMMY | DATA~ | | | |
| **Read From Cache x1 (Alternative)** | 0Bh | DUMMY | DUMMY | DUMMY | DUMMY | DATA~ | | |
| **Read From Cache x2**[Note3] | 3Bh | DUMMY | DUMMY | DUMMY | DATA~*2 | | | |
| **Read From Cache x4**[Note3] | 6Bh | DUMMY | DUMMY | DUMMY | DATA~*4 | | | |
| **Read From Cache Dual IO 1-2-2**[Note3] | BBh | DUMMY*2 | DUMMY*2 | DUMMY*2 | DATA~*2 | | | |
| **Read From Cache Quad IO 1-4-4**[Note3] | EBh | DUMMY*4 | DUMMY*4 | DUMMY*4 | DUMMY*4 | DATA~*4 | | |
| **Read ID** | 9Fh | DUMMY | MID | DID1 | DID2 | | | |
| **Block Erase** | D8h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Execute** | 10h | RADD2 | RADD1 | RADD0 | | | | |
| **Program Load x1** | 02h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load Random Data x1** | 84h | CADD1 | CADD0 | DATA~ | | | | |
| **Program Load x4**[Note3] | 32h | CADD1 | CADD0 | DATA~*4 | | | | |
| **Program Load Random Data x4**[Note3] | 34h | CADD1 | CADD0 | DATA~*4 | | | | |
| **Write Enable** | 06h | | | | | | | |
| **Write Disable** | 04h | | | | | | | |
| **Reset** | FFh | | | | | | | |
| **Read ECCSR** | 7Ch | DUMMY | SR_ECC | | | | | |
| **Write BBM** | A1h | LBA | LBA | PBA | PBA | | | |
| **Read BBM**[Note1] | A5h | DUMMY | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1~ |
| **ECC Warning Page Address**[Note2] | A9h | DUMMY | RADD2_L | RADD1_L | RADD0_L | RADD2_F | RADD1_F | RADD0_F |

***Notes:*** *1. A5h command may read the 40 links of BBM_table (LBAx/PBAx)*

*2. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address*

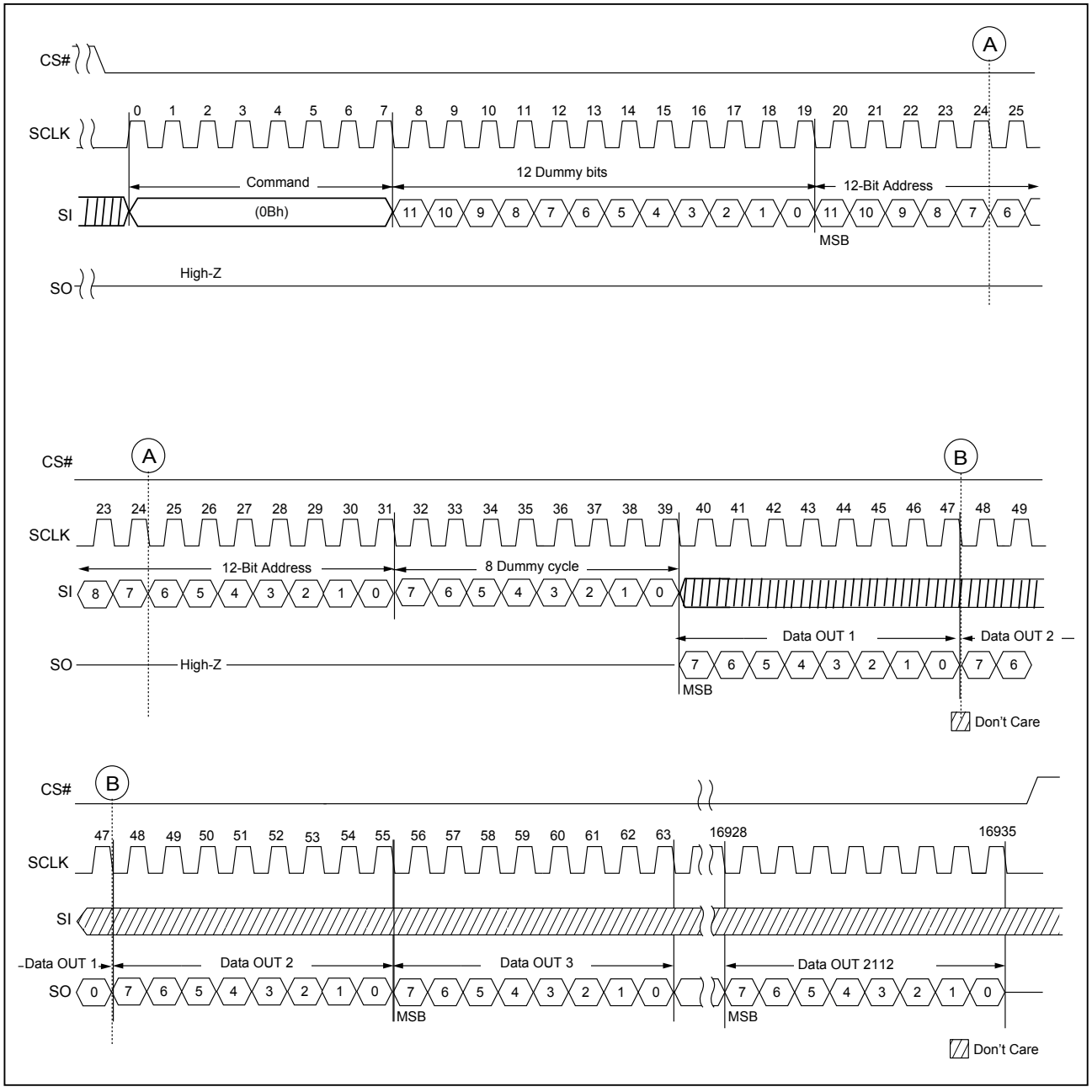
*3. *2 stands for the dual I/O phase and *4 for quad I/O mode*

**Figure 29. Read From Cache x1 (NOR like)**




***Note**: For SPI NOR Like Protocol command ('SPI_NOR_EN'=1), the Read From Cache command (03h) can run up to 20MHz only.*

**Figure 30. Read From Cache x1 (Alternative, NOR like)**



# 10. Feature Register

Feature register defines various register's definitions (Block Protection, Secure OTP, Status register). The definition of each register is defined in **"Table 18. Definition of Protection Bits"**.

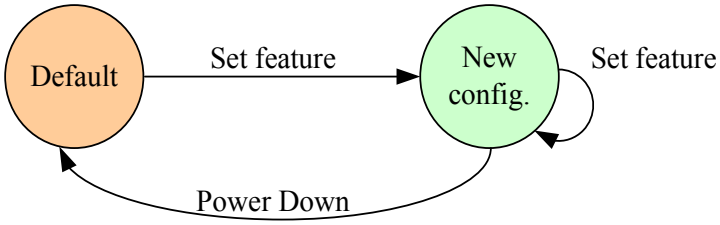
## 10-1. Configuration Feature Operation

### 10-1-1. Type: Volatile Register [Symbol: V]

Default value: can not be changed

Set feature command to change configuration register

**Figure 31. Setting of Volatile Configuration Register**

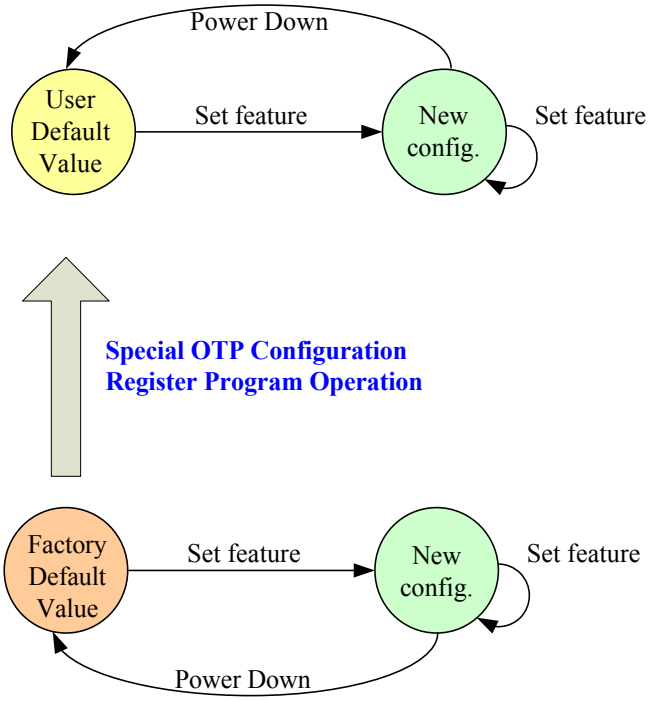



### 10-1-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2]

Default value: can be changed by special OTP Configuration Register program operation.

Set feature command to change value of configuration register. Those configuration register bits of type V2 are: CONT, BFT[3:0], DS_IO[1:0].

**Figure 32. Setting of Volatile Configuration Register (Type: V2)**




### 10-1-3. Type: One-time Setting Register [Symbol: OTP]

**- SPI_NOR_EN, OTPRWSP bit**

The OTP Configuration Register bits can be only changed from 0 to 1 through Special OTP Configuration Register Program Operation.

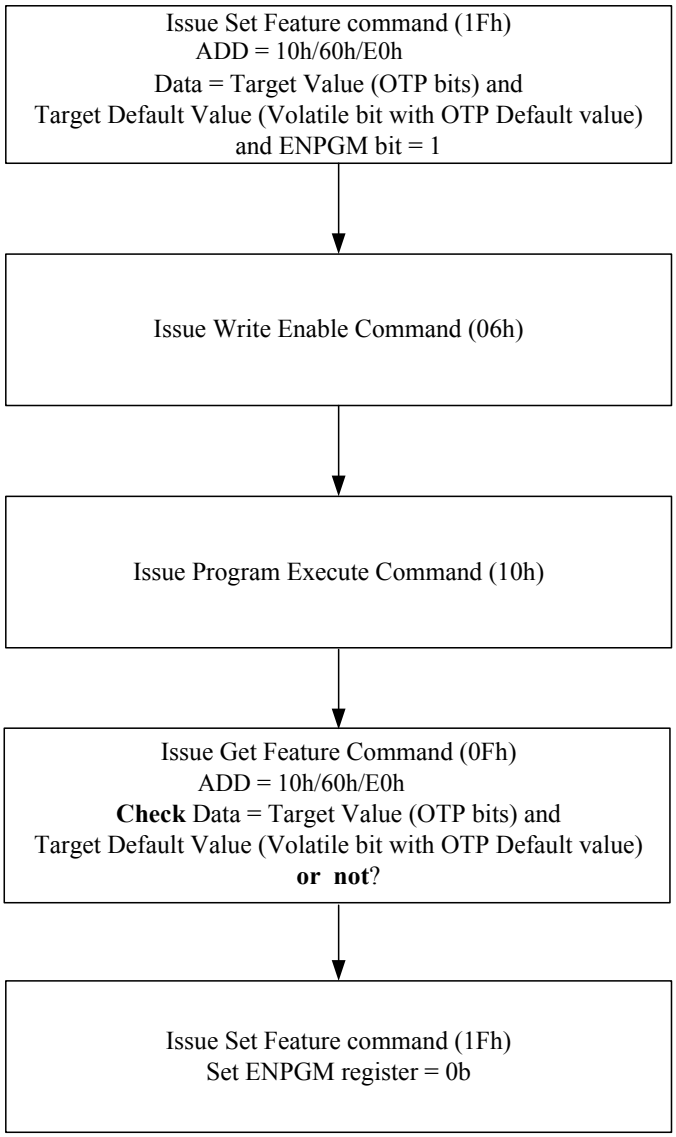
## 10-2. OTP "Configuration" Register Solid Protection

To avoid the OTP register bits and OTP Fuse value of V2 type Register bits to be programmed accidentally, this chip provide OTPRWSP (OTP register write solid protection) register to prevent it.

If OTPRWSP register bit is not programmed, the V2/OTP type registers (e.g. CONT, BFT[3:0], DS_IO[1:0], SPI_NOR_EN, OTPRWSP) can be programmed; after the OTPRWSP register is programmed, the V2/OTP type registers can not be programmed anymore.

User should program OTPRWSP register even though they do not want to change the V2/OTP register. This can avoid the accidental programming of the V2/OTP register during later usage.

**Figure 33. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)**




***Notes:***

1. *OTP Configuration Registers can be programmed together or individually by this programming flow.*
2. *It is recommended to program OTPRWSP register for V2/OTP Configuration Register solid protection. The related V2/OTP Configuration Registers can't be changed anymore, while OTPRWSP=1b.*

## 10-3. Block Protection Feature

The Block Protection feature includes three block protection bits (BPx), Block Protection Register Write Disable (BPRWD). Inverse bit (INVERT), complement bit (COMPLEMENTARY) and Solid Protection Bit (SP).

**Soft Protection Mode (SPM)**

The SPM uses the BPx bits, INVERT, and COMPLEMENTARY bits to allow part of memory to be protected as read only. The protected area definition is shown as **"Table 18. Definition of Protection Bits"**. The protected areas are more flexible which may protect various area by setting value of BP0-BP2 and Invert bit, and Complementary bit. These are volatile bits and can be modified by set feature command.

After power-up, the chip is in protection state, that is, the feature bits BPx is 1, all other bits (BPRWD, INVERT, COMPLEMENTARY and SP) are 0. The Set feature instruction (1Fh) with feature address (A0h) may change the value of the block protection bits and un-protect whole chip or a certain area for further program/erase operation. For example, after the power-on, the whole chip is protected from program/erase operation, the top 1/64 area may be un-protected by using the Set feature instruction (1Fh) with the feature address (A0h) to change the values of BP2 and BP1 from "1" to "0" as the Block protection register bits in **"Table 21. Configuration Register Bit Descriptions"**.

**Hardware Protection Mode (HPM) & Solid Protection Mode (SDPM)**

Under the Hardware Protection mode and Solid Protection Mode, the (BPx, INVERT, COMPLEMENTART) bits can not be changed.

**Hardware Protection Mode**: The device enters HPM if BPRWD bits is set to 1 and WP#/SIO2 is driven to 0.

***Note 1:*** *HPM also requires SP bit to be 0 state .*

***Note 2:*** *The Quad mode is not supported in HPM.*

**Solid Protection Mode:** If SP bit is set to 1, the device enters SDPM. After that, the selected block is solid protected and can not be un-protected until next power cycle.

**Table 18. Definition of Protection Bits**

| BP2 | BP1 | BP0 | Invert | Complementary | Protection Area |
|---|---|---|---|---|---|
| 0 | 0 | 0 | x | x | all unlocked |
| 0 | 0 | 1 | 0 | 0 | upper 1/64 locked |
| 0 | 1 | 0 | 0 | 0 | upper 1/32 locked |
| 0 | 1 | 1 | 0 | 0 | upper 1/16 locked |
| 1 | 0 | 0 | 0 | 0 | upper 1/8 locked |
| 1 | 0 | 1 | 0 | 0 | upper 1/4 locked |
| 1 | 1 | 0 | 0 | 0 | upper 1/2 locked |
| 1 | 1 | 1 | x | x | all locked (default) |
| 0 | 0 | 1 | 1 | 0 | lower 1/64 locked |
| 0 | 1 | 0 | 1 | 0 | lower 1/32 locked |
| 0 | 1 | 1 | 1 | 0 | lower 1/16 locked |
| 1 | 0 | 0 | 1 | 0 | lower 1/8 locked |
| 1 | 0 | 1 | 1 | 0 | lower 1/4 locked |
| 1 | 1 | 0 | 1 | 0 | lower 1/2 locked |
| 0 | 0 | 1 | 0 | 1 | lower 63/64 locked |
| 0 | 1 | 0 | 0 | 1 | lower 31/32 locked |
| 0 | 1 | 1 | 0 | 1 | lower 15/16 locked |
| 1 | 0 | 0 | 0 | 1 | lower 7/8 locked |
| 1 | 0 | 1 | 0 | 1 | lower 3/4 locked |
| 1 | 1 | 0 | 0 | 1 | block 0 |
| 0 | 0 | 1 | 1 | 1 | upper 63/64 locked |
| 0 | 1 | 0 | 1 | 1 | upper 31/32 locked |
| 0 | 1 | 1 | 1 | 1 | upper 15/16 locked |
| 1 | 0 | 0 | 1 | 1 | upper 7/8 locked |
| 1 | 0 | 1 | 1 | 1 | upper 3/4 locked |
| 1 | 1 | 0 | 1 | 1 | block0 |

***Note:*** *Block #0 is at lower portion.*

## 10-4. Secure OTP (One-Time-Programmable) Feature

There is an Secure OTP area which has 30 full pages (30 x 4224B for 4Gb or 30 x 2112B for 1Gb/2Gb) from page 02h to page 1Fh guarantee to be good for system device serial number storage or other fixed code storage. The Secure OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows partial page program to be “0”, once the Secure OTP protection mode is set, the Secure OTP area becomes read-only and cannot be programmed again.

The Secure OTP operation is operated by the Set Feature instruction with feature address (B0h) to access the Secure OTP operation mode and Secure OTP protection mode.

To check the Serial Flash device is ready or busy in the Secure OTP operation mode, the status register bit 0 (OIP bit) may report the status by Get Feature command operation.

To exit the Secure OTP operation or protect mode, it can be done by writing "0" to both Bit7 (Secure OTP protect bit) and bit6 (Secure OTP enable bit) for returning to the normal operation.

**Secure OTP Read**

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing normal Page Read command (13h)

**Secure OTP Program** (if the "Secure OTP Protection Bit" is "0") for

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing WRITE ENABLE command (06h)
4. Issuing Page Program command (02h)
5. Issuing program execute command (10h)

**Secure OTP Protection**

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set both the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" as "1".
3. Issuing program execute command (10h)

**Table 19. Secure OTP States**

| Secure OTP Protection Bit[Note1] | Secure OTP Enabled Bit | State |
|---|---|---|
| 0 | 0 | **Normal operation** |
| 0 | 1 | **Access the Secure OTP for reading or programming** |
| 1 | 0 | **Not applicable** |
| 1 | 1 | **Secure OTP Protection by using the Program Execution command (10h)[Note2]** |

***Note 1.*** *OTP protection bit is volatile.*

***Note 2.*** *Once the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" are set as "1", the secure OTP becomes read only.*

# 11. Configuration Registers and Status Registers

The device provides several registers which includes Block Protection registers and configuration registers to set the feature configurations as well as the status register to output the device status.

The resulting information is outlined in **"Table 20. Status Register Bit Descriptions"** & **"Table 21. Configuration Register Bit Descriptions"**.

## 11-1. Status Register

### 11-1-1. Get Feature command (0Fh)

MX35UFxGE4AD provides a status register that outputs the device status by writing a Get Feature command (0Fh) with the feature address (C0h), and then the IO pins output the status. Refer to **"Figure 7. GET FEATURE (0Fh) Timing"**.

The Get Feature (0Fh) command with the feature address(C0h) will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined as **"Table 20. Status Register Bit Descriptions"**.

### 11-1-2. Read Status command (RDSR, 05h)

In additional to read the chip status by Get Feature command, this device also supports the SPI NOR Read Status command (05h). The Read Status command can be issued any time (even during read/program/erase operation), it is recommended to check the Operation in Program (OIP) bit or Cache Read Busy (CRBSY) before sending a new instruction when a read, program or erase operation is in progress.

The sequence of issuing RDSR instruction is CS# goes low→ send RDSR instruction code →Status register data out on SO.

**Figure 34. Read Status Register (RDSR)**

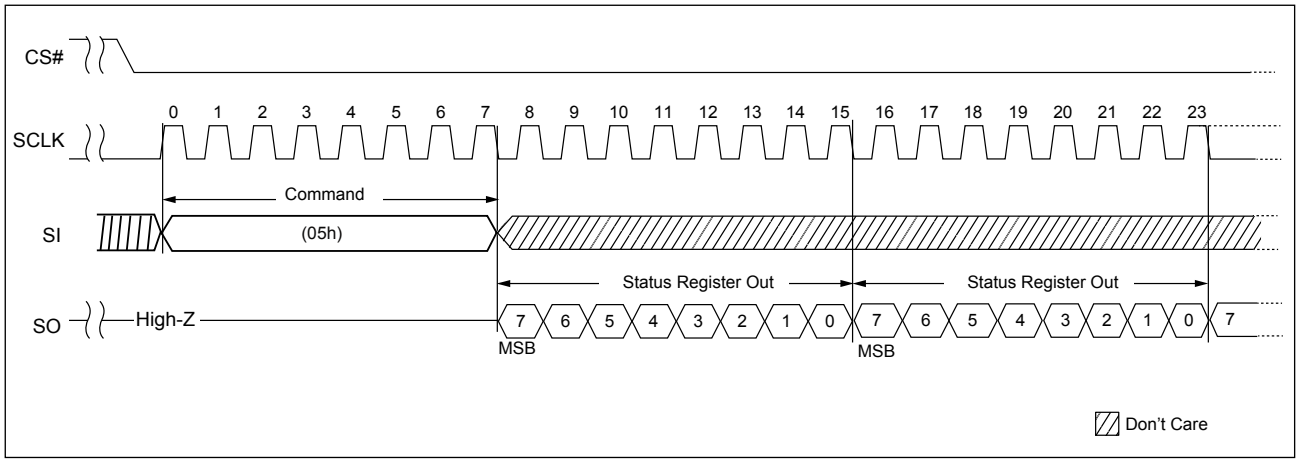


**Table 20. Status Register Bit Descriptions**

| Register | Feature bits | Type | Description |
|---|---|---|---|
| Status | CRBSY | V | Chip busy status for Cache Read operation<br>0b: Chip is ready and can accepted new command for cache operation<br>1b: Chip is busy and cannot accept new command for cache read operation |
| | BBMT_F | V | BBM table is full or not<br>0b: BBM table is not full and new L2P link can be added<br>1b: BBM table is full and new L2P link cannot be added |
| | ECC_S[1:0] | V | The bit shows the status of ECC as below:<br>00b = 0 bit error<br>01b = bit error are detected and been corrected, bit error count is less than the bit flip threshold<br>10b = bit error and can not be corrected.<br>11b = bit error are detected and been corrected, bit error count is equal or more than the bit flip threshold.<br>If CONT=0, the value of ECC_Sx(S1:S0) bits will be cleared as “00b” by reset command. After the page read or page read cache operation is completed, the bits will be updated to reflect the ECC status of the current output page. The ECC_Sx(S1:S0) value reflects the ECC status of the content of the POR page (the default POR page is the page 0 of the block 0) after a power-on reset.<br>If CONT=1, the value of ECC_Sx(S1:S0) bits will not be cleared by the reset command. After the continuous read operation is completed, the bits will be updated to reflect the ECC status of the accumulated pages in the current continuous read operation. The ECC_Sx(S1:S0) value reflects the ECC status of the content of the accumulated pages which starts from the POR page after a power-on reset.<br>If the internal ECC is disabled by the Set feature command, the ECC_ Sx(S1:S0) are invalid. |
| | P_FAIL | V | The bit value shows the status of program failure or if host program any invalid address or protected area (including protected blocks or protected Secure OTP area).<br>0: Passed<br>1: Failed<br>The bit value will be cleared (as "0") by RESET command or during the program execute command operation. |
| | E_FAIL | V | The bit value shows the status of erase failure or if host erase any invalid address or protected area (including protected blocks or protected Secure OTP area).<br>0: Passed,<br>1: Failed<br>The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation. |
| | WEL | V | Status bit for write enable successful or not. The bit value will be cleared (as "0") by issuing Write Disable command(04h) or after the program/erase operation completion.<br>0b: the chip is write protected and cannot accept any program/erase command<br>1b: the chip is not write protected and can accept the program/erase command |
| | OIP | V | Chip busy Status bit<br>0b: Chip is ready<br>1b: Chip is busy |

**Table 21. Configuration Register Bit Descriptions**

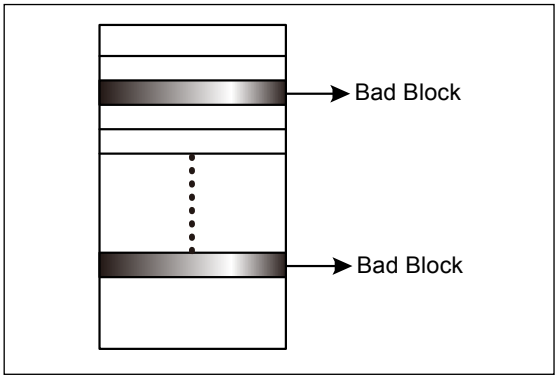
| Register | Feature bits | Type | Description |
|---|---|---|---|
| Special Read for Data Recovery | SPEC_RD[2:0] | V | Special Read for data recovery option |
| Configuration | ENPGM | V | Enable the special OTP configuration register program operation<br>0b: Disabled<br>1b: Enabled |
| | BFT[3:0] | V2 | ECC bit flip threshold |
| | OTPRWSP | OTP | V2/OTP type feature register write solid protection<br>0b: V2/OTP feature register are not solid protected<br>1b: V2/OTP feature register are solid protected (after OTPRWSP bit is programmed) |
| | SPI_NOR_EN | OTP | Enable SPI NOR Interface<br>0b: SPI NOR Interface is NOT selected<br>1b: SPI NOR Interface is selected |
| | CONT | V2 | Enable Continuous read operation mode<br>0b: Not enabled<br>1b: Enabled |
| | QE | V | Quad enable<br>0b: Not enabled<br>1b: Enabled |
| | OTP_PROT | V | Secure OTP protection<br>0b: Not enabled<br>1b: Enabled |
| | OTPEN | V | Secure OTP enable<br>0b: Not enabled<br>1b: Enabled |
| | ECC_EN | V | Internal ECC enabled<br>0b: Not enabled<br>1b: Enabled (default) |
| | DS_IO[1:0] | V2 | I/O Strength Feature, refer to **"Table 3. I/O Strength Feature Table"** |
| Block Protection | BPRWD | V | Block protection on register write protect<br>0b: Block protection register is not protected<br>1b & WP# = HI: Block protection register is not protected<br>1b & WP# = Low: Block protection register is protected |
| | BP[2:0], Invert, Complementary | V | Block protection registers |
| | SP | V | Enabled the block protection register write solid protection function<br>0b: Block protection register is not solid protected<br>1b: Block protection register is solid protected |

# 12. SOFTWARE ALGORITHM

## 12-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is necessary to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since the bad block marks may be cleared by any erase operation.

**Figure 35. Bad Blocks**




While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **"Figure 36. Bad Block Test Flow"** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

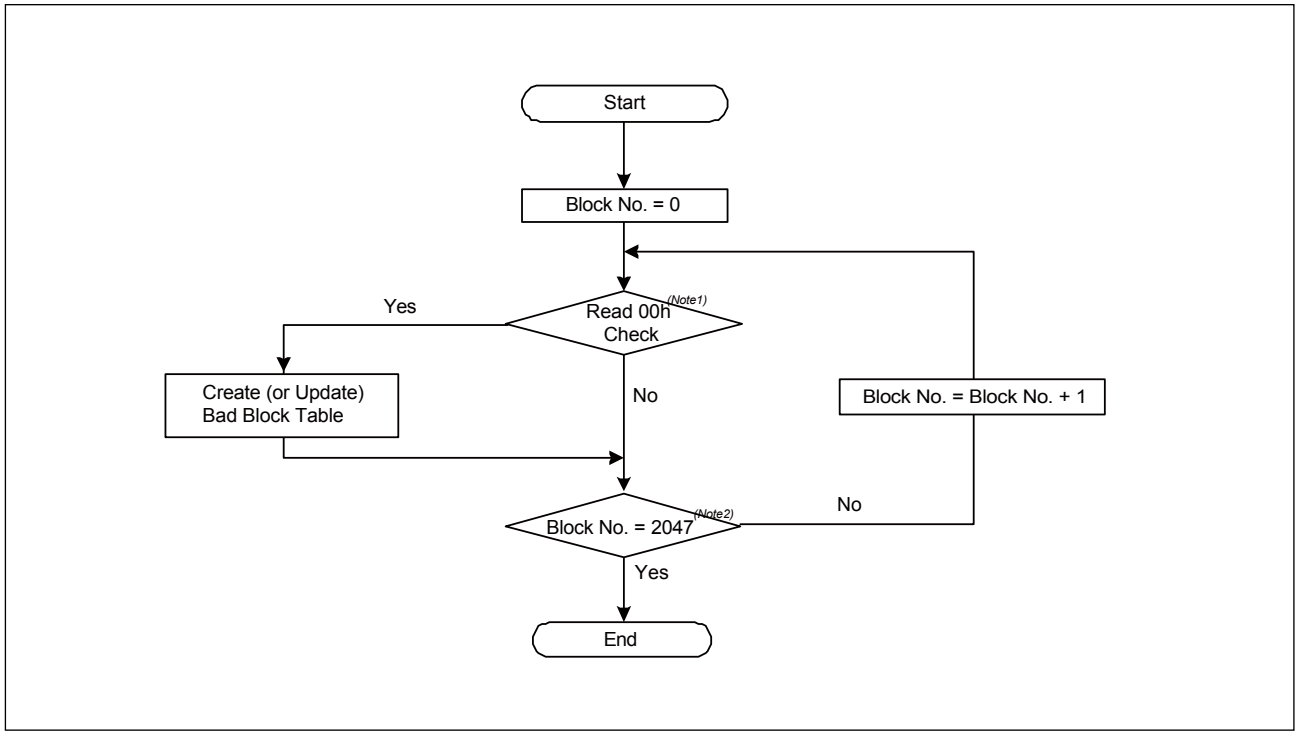
**Table 22. Valid Blocks**

| | Density | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Valid (Good) Block Number | 4Gb | 2008 | | 2048 | Block | Block 0-7 is guaranteed to be good |
| | 2Gb | 2008 | | 2048 | Block | Block 0-7 is guaranteed to be good |
| | 1Gb | 1004 | | 1024 | Block | Block 0-7 is guaranteed to be good |

## 12-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal Serial flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **"Figure 36. Bad Block Test Flow"** shows the recommended flow for creating a bad block table. There is a simple way to build the bad block table, by utilizing the internal "Bad Block management" table in the device and maintain the link of logical to physical block address.

**Figure 36. Bad Block Test Flow**




***Note 1:*** *Read 00h check is at the 1st byte of the 1st and 2nd pages of the block spare area.*

***Note 2:*** *Block No.=1023 for 1Gb.*

## Bad Block Management Function

The BBM table supports 40 links.

The BBM table is an OTP Non-volatile memory

1. The BBM table is written by “Write BBM” command (A1h) and input the address of LBA & PBA, and then wait a tPROG time.
2. The user can read the BBM by “read BBM” command (A5h)

**Figure 37. BBM Table**

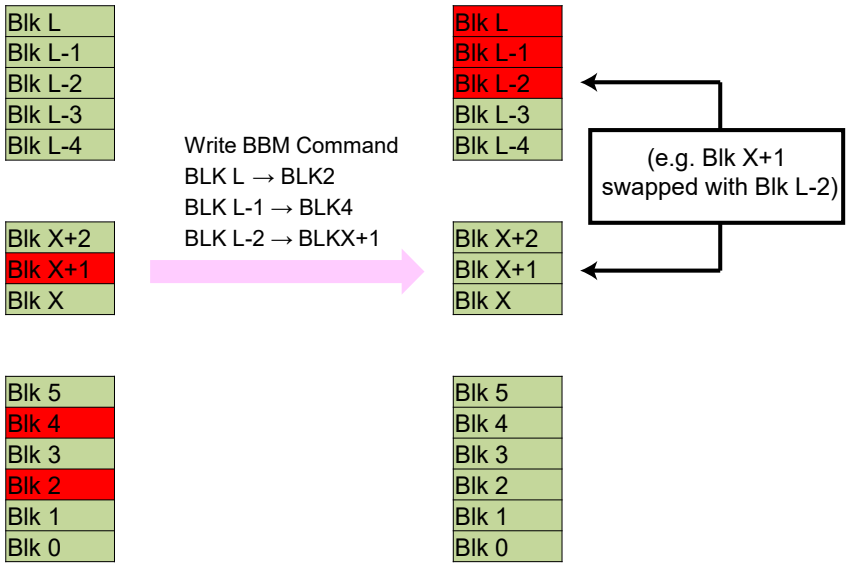



**Figure 38. Write BBM Command (A1h)**

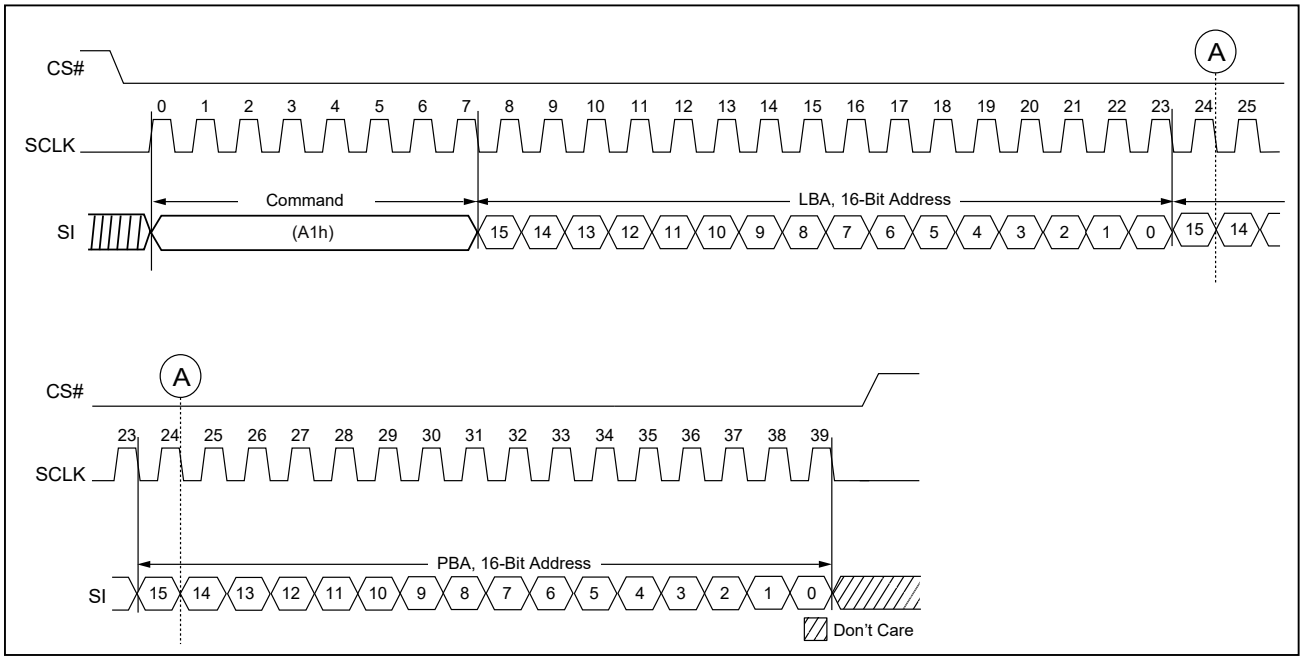


**Figure 39. Read BBM Command (A5h)**

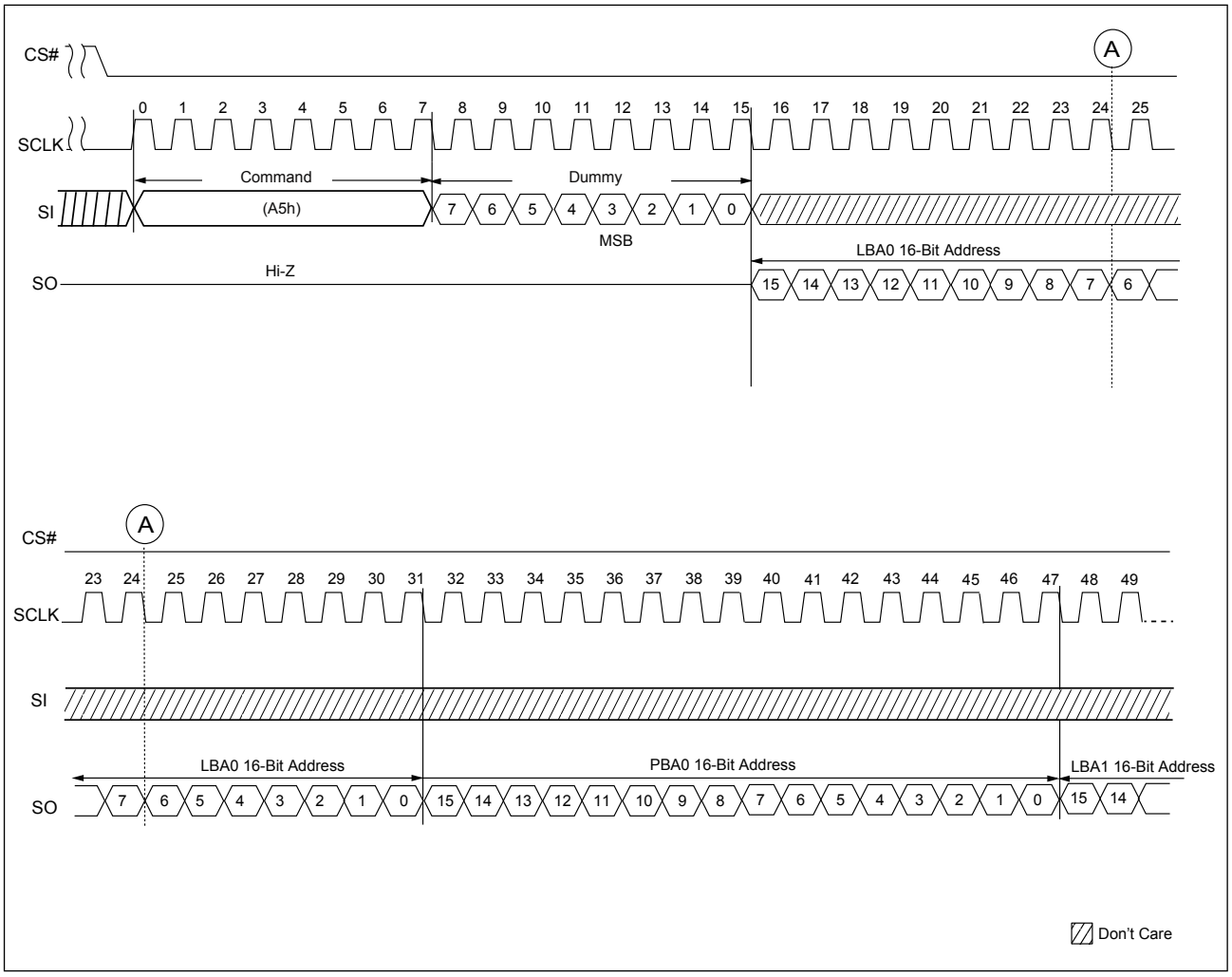


**Figure 40. Bad Block Management**

The user can read the BBM table full or not by “get feature” command for BBMT_F status bit.

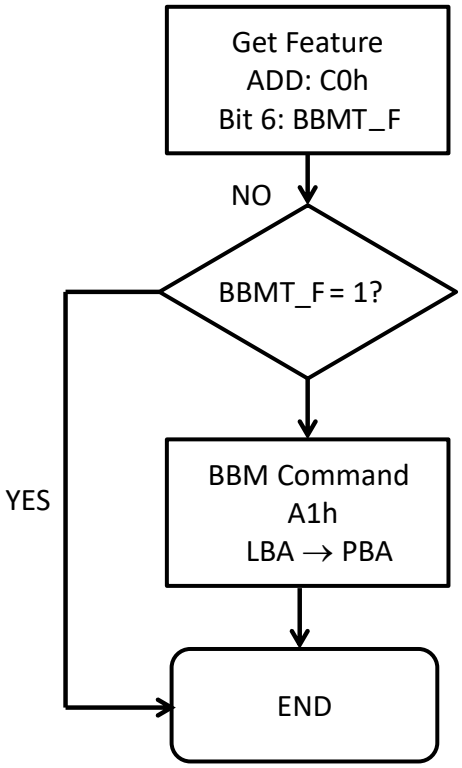



**Table 23. BBM Address Definition**

When user read out the BBM table, the LBA[15:14] has special meaning which indicates this link is enable and valid status.

| ADD | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|
| LBA[15:8] | ENABLE | INVALID | 0 | 0 | 0 | LRA[16]*Note* | LRA[15] | LRA[14] |
| LBA[7:0] | LRA[13] | LRA[12] | LRA[11] | LRA[10] | LRA[9] | LRA[8] | LRA[7] | LRA[6] |
| PBA[15:8] | 0 | 0 | 0 | 0 | 0 | PRA[16]*Note* | PRA[15] | PRA[14] |
| PBA[7:0] | PRA[13] | PRA[12] | PRA[11] | PRA[10] | PRA[9] | PRA[8] | PRA[7] | PRA[6] |

***Note:*** *LRA[16]/PRA[16] is not applicable for 1Gb.*

| ENABLE | INVALID | Description |
|---|---|---|
| 0 | 0 | This link is not used |
| 1 | 0 | This link is enabled and valid |
| 1 | 1 | This link is enabled but invalid |
| 0 | 1 | This case does not exist |

## 12-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

**Table 24. Failure Modes**

| Failure Mode | Detection and Countermeasure | Sequence |
|---|---|---|
| **Erase Failure** | **Status Read after Erase** | Block Replacement |
| **Programming Failure** | **Status Read after Program** | Block Replacement |
| **Read Failure** | **Read Failure** | Special Read |

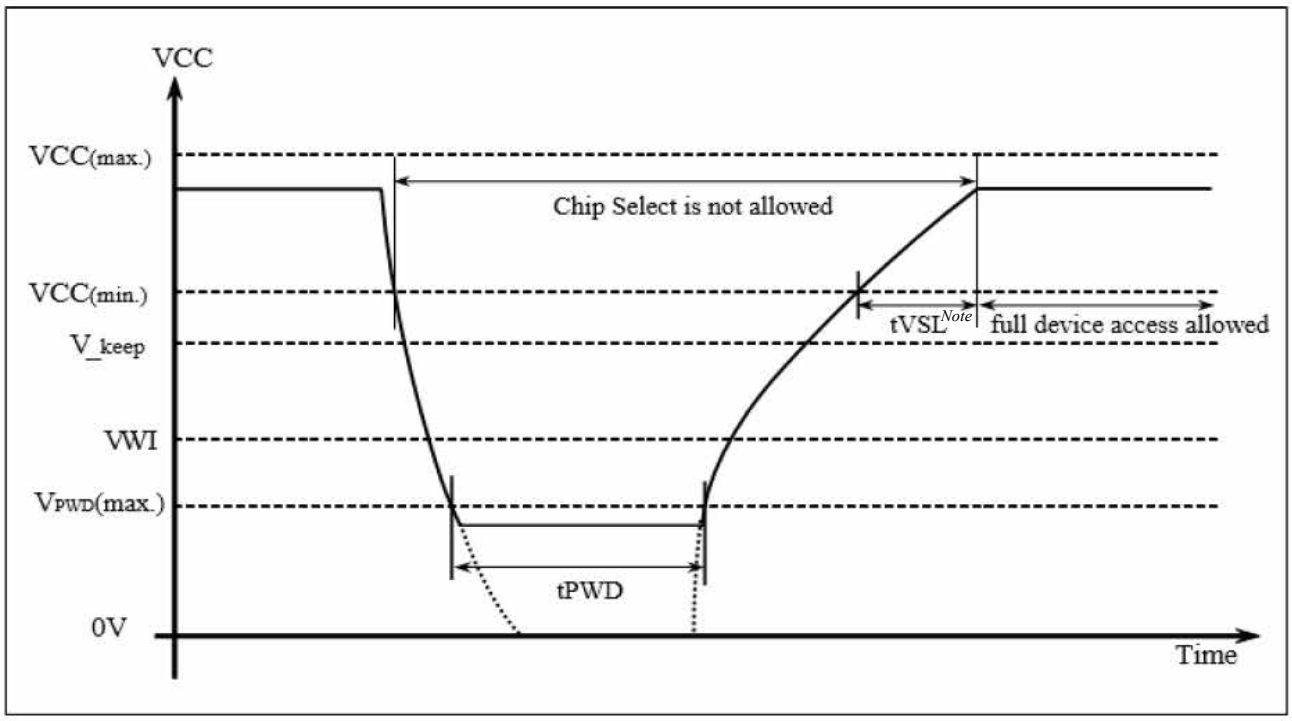
# 13. DEVICE POWER-UP

## 13-1. Power-up

After the Chip reaches the power on level, the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. The device can be fully accessible when VCC reaches the power-on level and wait 5ms.

During the power on and power off sequence, it is necessary to keep the WP# = Low for internal data protection.

**Figure 41. Power Up/Down and Voltage Drop**




***Note:*** *After VCC ramp up to VCC(min) during power on, the user can issue the read status command to check 'OIP' bit for the chip busy status.*

**Table 25. Power-Up/Down Voltage and Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{PWD}$ | VCC voltage needs to be below $V_{PWD}$ for proper initialization to occur | | 0.9 | V |
| $V_{_keep}$ | Voltage threshold where re-initialization is necessary if VDD drop below to $V_{_KEEP}$ | 1.5 | | V |
| tPWD | The minimum duration to ensure initialization occurs | 300 | | us |
| tVSL | VCC(min.) to device operation | 5000 | | us |
| VCC | VCC Power Supply | 1.7 | 1.95 | V |
| VWI | Write Inhibit Voltage | 1.0 | 1.5 | V |

***Note:*** *These parameters are characterized only.*

# 14. PARAMETERS

## 14-1. ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Temperature under Bias** | -50°C to +125°C |
| **Storage temperature** | -65°C to +150°C |
| **All input voltages with respect to ground (Note 2)** | -0.6V to 2.4V |
| **VCC supply voltage with respect to ground (Note 2)** | -0.6V to 2.4V |
| **ESD protection** | >2000V |

***Notes:***

1. *The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.*
2. *Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.*
3. *During voltage transitions, all pins may overshoot Vss to -1.0V and Vcc to +1.0V for periods up to 20ns, please refer to* **"Figure 42. Maximum Negative Overshoot Waveform"** *and* **"Figure 43. Maximum Positive Overshoot Waveform"**.

**Figure 42. Maximum Negative Overshoot Waveform**

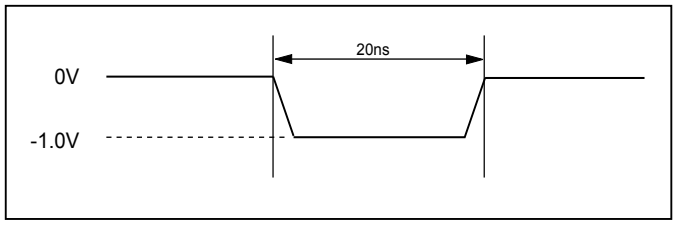



**Figure 43. Maximum Positive Overshoot Waveform**

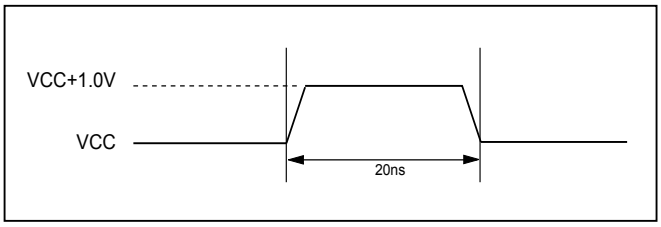



**Table 26. AC Testing Conditions**

| Testing Conditions | Value | Unit |
|---|---|---|
| **Input pulse level** | 0 to VCC | V |
| **Output load capacitance** | 1TTL+CL(30) | pF |
| **Input rising & falling time** | 5 | ns |
| **Input timing measurement reference levels** | VCC/2 | V |
| **Output timing measurement reference levels** | VCC/2 | V |

**Table 27. Capacitance**

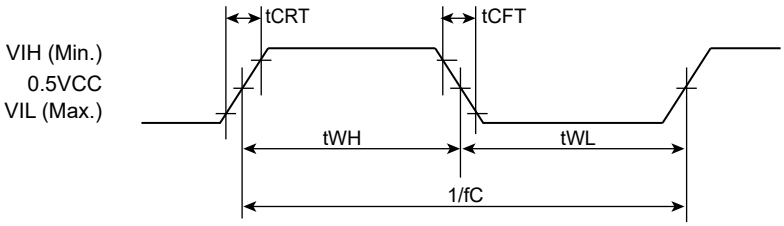
TA = +25°C, F = 1 MHz

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input capacitance | | | 10 | pF | VIN = 0V |
| COUT | Output capacitance | | | 10 | pF | VOUT = 0V |

**Table 28. Operating Range**

| Temperature | VCC | Tolerance |
|---|---|---|
| -40°C to + 85°C | +1.8V | 1.7-1.95V |

**Figure 44. SCLK TIMING DEFINITION**



### Table 29. DC Characteristics

| Symbol | Parameter | Min. | Typical | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ILI | Input leakage current | | | ± 10 | uA | VIN= 0 to VCC MAX |
| ILO | Output leakage current | | | ± 10 | uA | VOUT= 0 to VCC MAX |
| ISB1 | VCC standby current (CMOS) | | | 110 | uA | VIN=VCC or GND, CS#=VCC |
| ICC1 | VCC active current (Read for non-continuous read operation) | | | 40 | mA | f=133MHz, Iout = 0mA |
| | | | | 30 | mA | f=80MHz, Iout = 0mA |
| ICC2 | VCC active current (Read for continuous read operation) | | | 50 | mA | f=104MHz, Iout = 0mA |
| | | | | 40 | mA | f=80MHz, Iout = 0mA |
| ICC3 | VCC active current (Program) | | | 40 | mA | |
| ICC4 | VCC active current (Erase) | | | 30 | mA | |
| VIL | Input low level | -0.3 | | 0.2VCC | V | |
| VIH | Input high level | 0.8VCC | | VCC + 0.3 | V | |
| VOL | Output low voltage | | | 0.2 | V | IOL= 1mA |
| VOH | Output high voltage | VCC-0.2 | | | V | IOH= -20uA |

### Table 30. General Timing Characteristics

| Symbol | Parameter | | Note | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| fC | Serial Clock Frequency for all command | | 1 | D.C. | 133 | MHz |
| tCHHH | HOLD# Hold Time (relative to SCLK) | | | 3.375 | - | ns |
| tCHHL | HOLD Hold Time (relative to SCLK) | | | 3.375 | - | ns |
| tCS | CS# Diselect Time | | | 30 | - | ns |
| tCHSH | CS# Active Hold Time (relative to SCLK) | | | 3.375 | - | ns |
| tSLCH | CS# Active Setup Time (relative to SCLK) | | | 3.375 | - | ns |
| tSHCH | CS# Not Active Setup Time (relative to SCLK) | | | 3.375 | - | ns |
| tCHSL | CS# Not Active Hold Time (relative to SCLK) | | | 3.375 | - | ns |
| tDIS | Output Disable Time | | | - | 6 | ns |
| tHC | HOLD Setup Time (relative to SCLK) | | | 3.375 | - | ns |
| tHD | HOLD# Setup Time (relative to SCLK) | | | 3.375 | - | ns |
| tHDDAT | Data Input Hold Time | | | 2 | - | ns |
| tHO | Data Output Hold time | | | 1 | | ns |
| tHZ | HOLD# to Output High-Z | | | - | 12 | ns |
| tLZ | HOLD# to Output Low-Z | | | - | 7 | ns |
| tSUDAT | Data In Setup Time | | | 2 | - | ns |
| tV | Serial Clock Low to Output Valid | 30pF | | - | 6 | ns |
| | | 10pF | | - | 5 | ns |
| tWH | Serial Clock High Time | | | 0.45 x 1/fC | - | ns |
| tWL | Serial Clock Low Time | | | 0.45 x 1/fC | - | ns |
| tCRT | Clock Rise Time (peak to peak) | | | 0.5 | - | V/ns |
| tCFT | Clock Fall Time (peak to peak) | | | 0.5 | - | V/ns |
| tWPH | Write protect Hold Time | | | 100 | - | ns |
| tWPS | Write protect Setup Time | | | 20 | - | ns |
| tVSL | VCC(min.) to device operation | | | 5 | - | ms |
| tRST | Device reset time (Idle/ Read/ Program/ Erase) | | 2 | | 5/5/10/500 | us |

***Notes:***

***1****: fC(max) is 20MHz for read from cache x1 (03h) if SPI NOR interface is enabled ('SPI_NOR_EN'=1) and the fC(max) is 104MHz (for 4Gb) and 80MHz (for 1Gb/2Gb) is for sequential page of continuous read operation.*

***2:*** *the tRST is 5ms for the first RESET command after Power-on.*

**Table 31. Program/ Read/ Erase Characteristics (1Gb/2Gb)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tRD | Data transfer time from Serial Flash array to data register | - | - | 80 | us |
| tRD_OTP | Data transfer time from Serial Flash array to data register for OTP Page | - | - | 85 | us |
| tRCBSY | Dummy busy time for cache read | - | 50 | 80 | us |
| tPROG | Page Programming time | - | 360 | 760 | us |
| tERS | Block Erase Time | - | 4 | 6 | ms |
| NOP | Number of partial-page programming operation supported | | | 4 | Cycle |

**Table 32. Program/ Read/ Erase Characteristics (4Gb)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tRD | Data transfer time from Serial Flash array to data register | - | - | 110 | us |
| tRD_OTP | Data transfer time from Serial Flash array to data register for OTP Page | - | - | 115 | us |
| tRCBSY | Dummy busy time for cache read | - | 90 | 110 | us |
| tPROG | Page Programming time | - | 400 | 800 | us |
| tERS | Block Erase Time | - | 4 | 6 | ms |
| NOP | Number of partial-page programming operation supported | | | 4 | Cycle |

**Figure 45. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1**

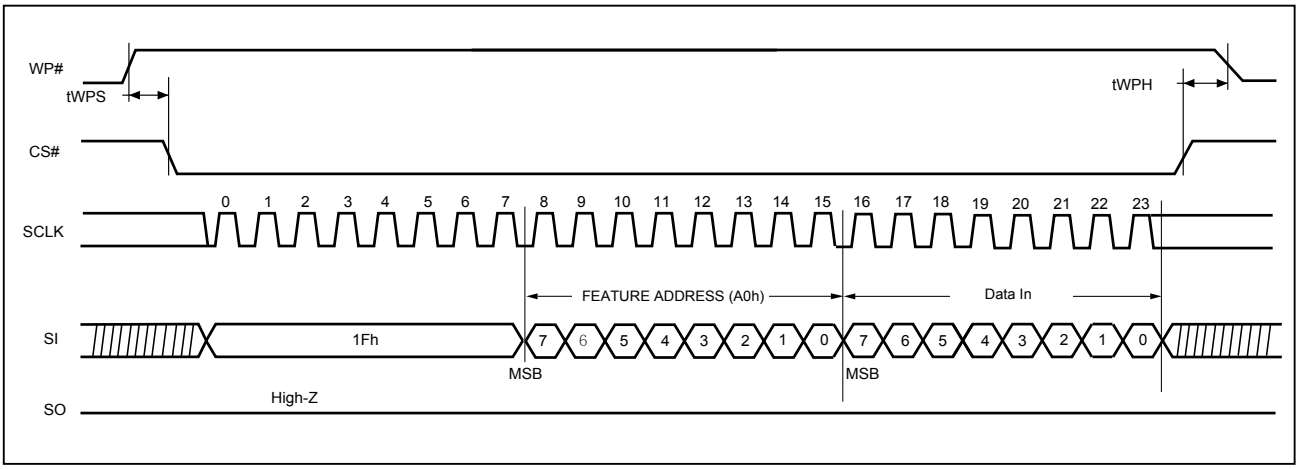



**Figure 46. Serial Input Timing**

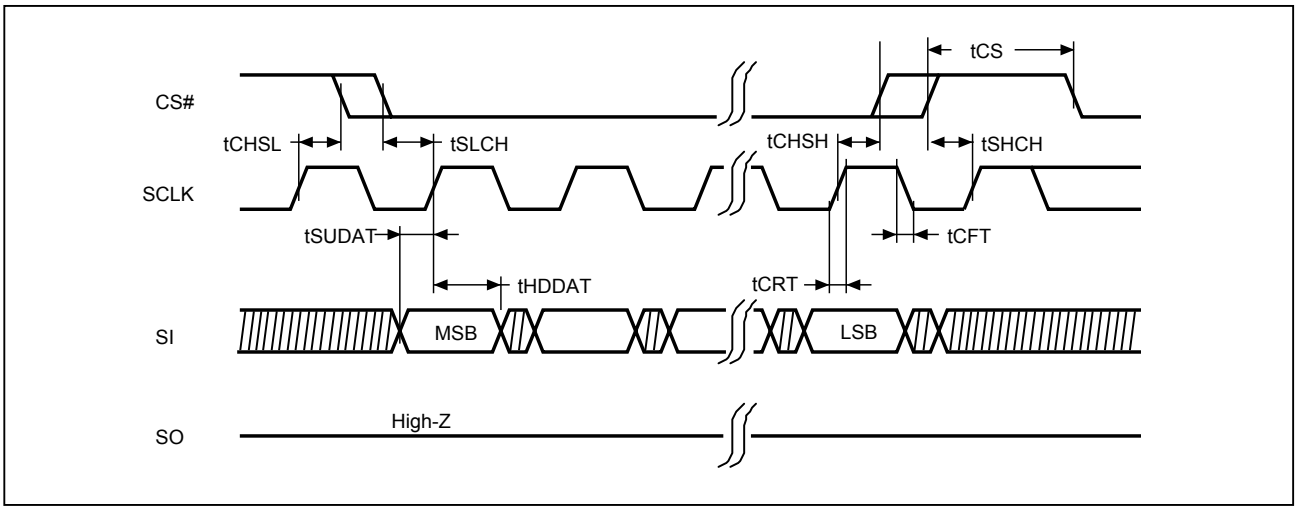



**Figure 47. Serial Output Timing**

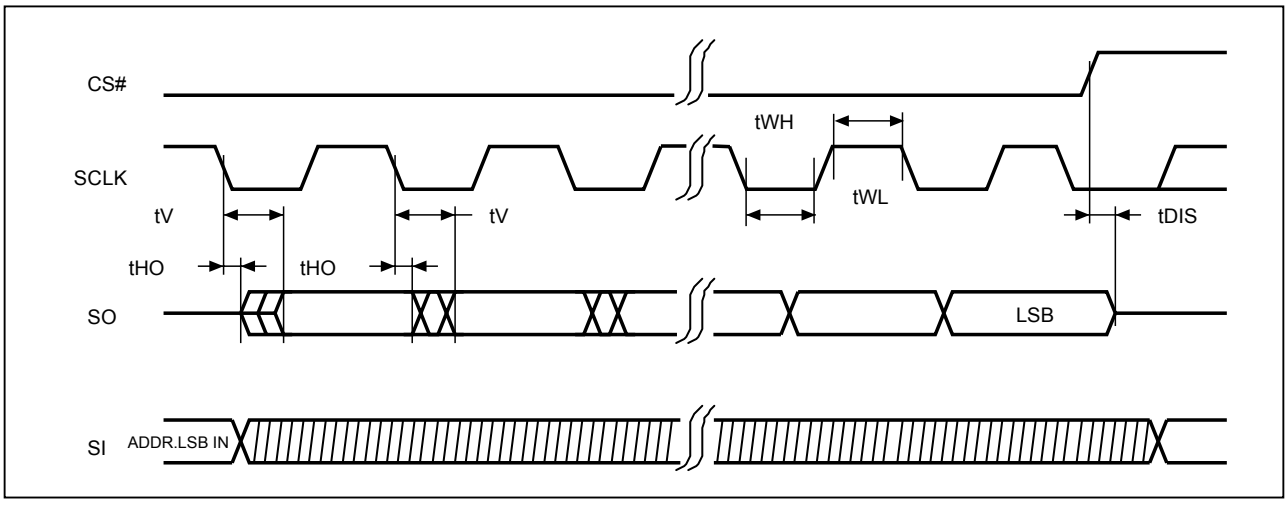
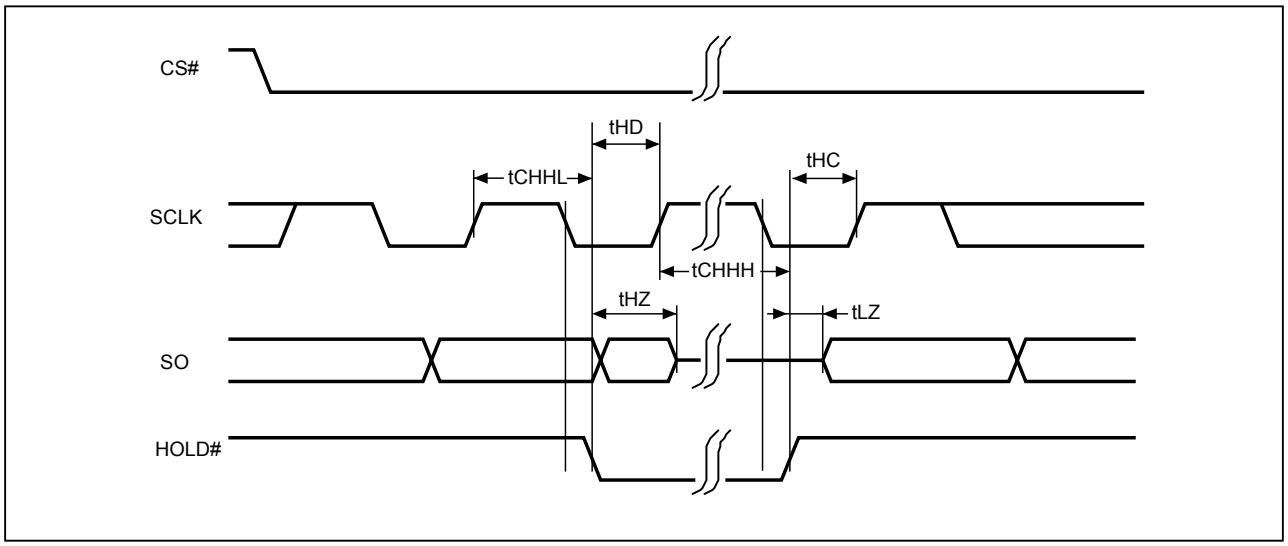


**Figure 48. Hold Timing**

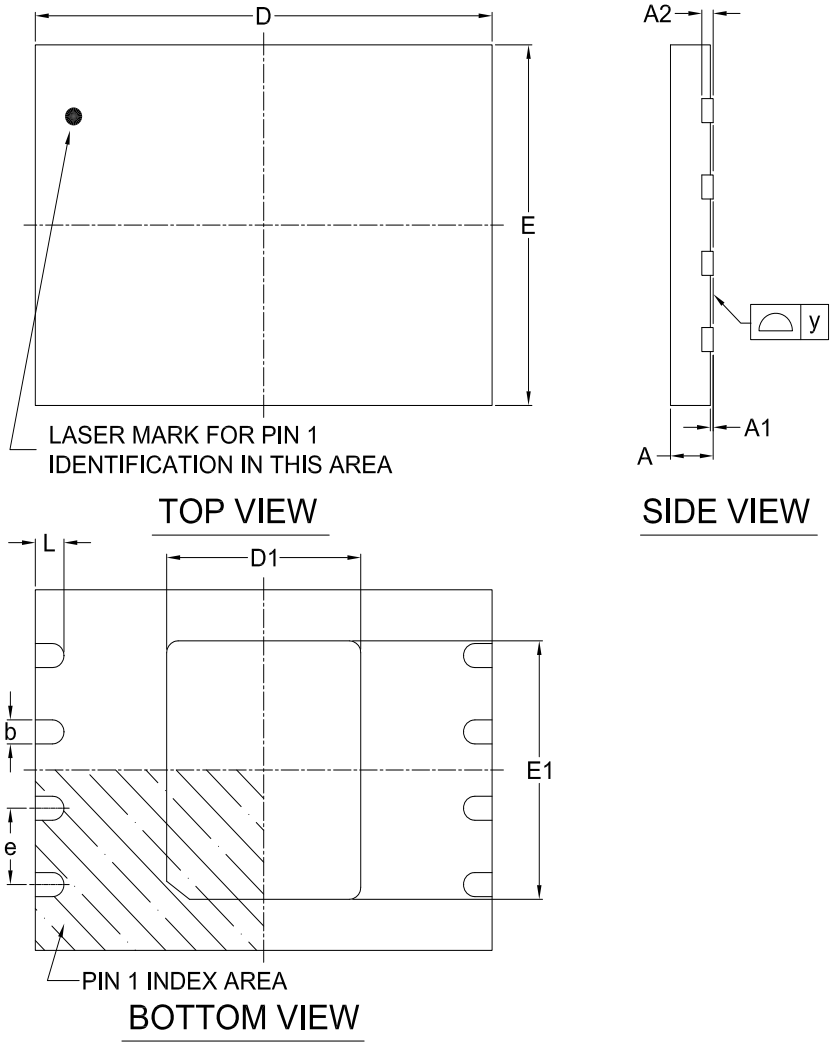



***Note:*** *SI is "don't care" during HOLD operation.*

# 15. PACKAGE INFORMATION

## 15-1. 8-WSON (8x6x0.8mm)

**Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)**




Note:

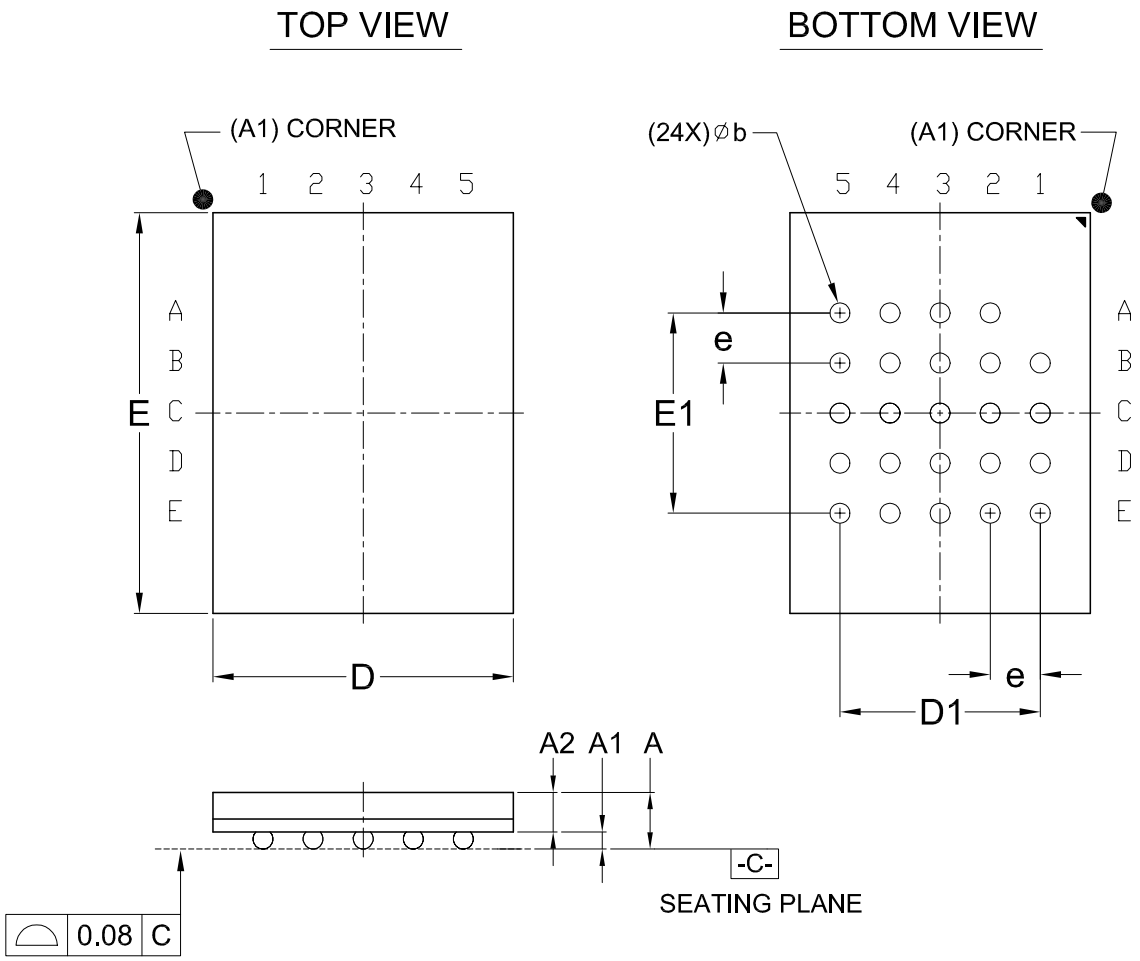
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.70 | --- | --- | 0.35 | 7.90 | 3.35 | 5.90 | 4.25 | 0.45 | --- | 0.00 |
| | Nom. | --- | --- | 0.20 | 0.40 | 8.00 | 3.40 | 6.00 | 4.30 | 0.50 | 1.27 | --- |
| | Max. | 0.80 | 0.05 | --- | 0.48 | 8.10 | 3.45 | 6.10 | 4.35 | 0.55 | --- | 0.05 |
| Inch | Min. | 0.028 | --- | --- | 0.014 | 0.311 | 0.132 | 0.232 | 0.167 | 0.018 | --- | 0.00 |
| | Nom. | --- | --- | 0.008 | 0.016 | 0.315 | 0.134 | 0.236 | 0.169 | 0.020 | 0.05 | --- |
| | Max. | 0.032 | 0.002 | --- | 0.019 | 0.319 | 0.136 | 0.240 | 0.171 | 0.022 | --- | 0.002 |

### 15-2. 24-BGA (6x8x1.2mm)

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.25 | 0.65 | 0.35 | 5.90 | --- | 7.90 | --- | --- |
| | Nom. | --- | 0.30 | --- | 0.40 | 6.00 | 4.00 | 8.00 | 4.00 | 1.00 |
| | Max. | 1.20 | 0.35 | --- | 0.45 | 6.10 | --- | 8.10 | --- | --- |
| Inch | Min. | --- | 0.010 | 0.026 | 0.014 | 0.232 | --- | 0.311 | --- | --- |
| | Nom. | --- | 0.012 | --- | 0.016 | 0.236 | 0.157 | 0.315 | 0.157 | 0.039 |
| | Max. | 0.047 | 0.014 | --- | 0.018 | 0.240 | --- | 0.319 | --- | --- |

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