1.8V, 1G-bit/2G-bit/4G-bit Serial NAND Flash Memory

MX35UFxG24AD

Contents

1. FEATURES 5

2. GENERAL DESCRIPTIONS 6

Figure 1. Logic Diagram 6

3. ORDERING INFORMATION 7

4. BALL ASSIGNMENT AND DESCRIPTIONS 8

Figure 2. 8-WSON (8x6mm) 8

5. PIN DESCRIPTIONS 8

6. DEVICE OPERATION 9

Figure 3. Serial Mode Supported 9

7. ADDRESS MAPPING 10

8. COMMAND DESCRIPTION 11

Table 1. Command Set 11

8-1. WRITE Operations 12

8-1-1. Write Enable 12

Figure 4. Write Enable (WREN) Sequence 12

8-1-2. Write Disable (04h) 12

Figure 5. Write Disable (WRDI) Sequence 12

8-2. Feature Operations 13

8-2-1. GET Feature (0Fh) and SET Feature (1Fh) 13

Table 2. Configuration Registers 13

Table 3. I/O Strength Feature Table 13

Figure 6. GET FEATURE (0Fh) Timing 14

Figure 7. SET FEATURE (1Fh) Timing 14

8-3. READ Operations 15

8-3-1. PAGE READ (13h) 15

8-3-2. QE Bit 15

8-3-3. DC Bit (Dummy Cycle Option Bit) 15

Figure 8. PAGE READ (13h) Timing x1 16

Figure 9. READ FROM CACHE (03h or 0Bh) Timing 17

Figure 10. READ FROM CACHE x 2 18

Figure 11. Read From Cache Dual IO 1-2-2 (DC bit = 0) 19

Figure 12. READ FROM CACHE x 4 20

Figure 13. Read From Cache Quad IO 1-4-4 (DC bit = 0) 21

8-3-4. Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh) 22

Figure 14. Page Read Cache Random (30h) 22

Figure 15. Page Read Cache Sequential (31h) 23

Figure 16. Page Read Cache End (3Fh) 24
Figure 17. Page Read Cache Flow 25
8-3-5. Special Read for Data Recovery 26
Figure 18. Procedure of Entering/Exiting the Special Read for Data Recovery operation 26
Table 4. Feature Settings 27
8-3-6. Randomizer Operation 27
Table 5. The definition of RANDOPT bit for the randomized area per page 27

9. SPI NOR Compatible Command 28
Table 6. Command Set - SPI NOR Like Protocol Enabled 28
Figure 19. Read From Cache x1 (NOR like) 29
Figure 20. Read From Cache x1 (Alternative, NOR like) 30
9-3-1. READ ID (9Fh) 31
Table 7. READ ID Table 31
Figure 21. READ ID (9Fh) Timing 31

9-1. Parameter Page 32
Table 8. Parameter Page Data Structure (MX35UF1G24AD) 32
Table 9. Parameter Page Data Structure (MX35UF2G24AD) 34
Table 10. Parameter Page Data Structure (MX35UF4G24AD) 36

9-2. UniqueID Page with PUF Type Code Structure 38

9-3. Program Operations 39
9-3-1. PAGE PROGRAM 39
Figure 22. PROGRAM LOAD (02h) Timing 39
Figure 23. PROGRAM LOAD RANDOM DATA (84h) Timing 40
9-3-2. QUAD IO PAGE PROGRAM 41
Figure 24. PROGRAM LOAD X4 (32h) Timing 41
Figure 25. PROGRAM EXECUTE (10h) Timing 42
Figure 26. QUAD IO PROGRAM RANDOM INPUT (34h) Timing 43

10. BLOCK OPERATIONS 44

10-1. Block Erase (D8h) 44
Figure 27. Block Erase (BE) Sequence 44

11. Feature Register 45

11-1. Configuration Feature Operation 45
11-1-1. Type: Volatile Register [Symbol: V] 45
11-1-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2] 45
11-1-3. Type: One-time Setting Register [Symbol: OTP] 45
Figure 28. Setting of Volatile Configuration Register 45
Figure 29. Setting of Volatile Configuration Register (Type: V2) 45
Figure 30. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits) 46

11-2. OTP "Configuration" Register Solid Protection 46
11-3. Block Protection Feature 47
Table 11. Definition of Protection Bits 48
11-4. Secure OTP (One-Time-Programmable) Feature 49
Table 12. Secure OTP States 49
11-5. Status Register 50
11-5-1. Get Feature command (0Fh) 50
11-5-2. Read Status command (RDSR) 50
Figure 31. Read Status Register (RDSR) 50
Table 13. Status Register Bit Descriptions 51
12. Deep Power-down Mode 52
Figure 32. Deep Power-down (DP) Sequence and Release from Deep Power-down Sequence 52
13. SOFTWARE ALGORITHM 53
13-1. Invalid Blocks (Bad Blocks) 53
Figure 33. Bad Blocks 53
Table 14. Valid Blocks 53
13-2. Bad Block Test Flow 54
Figure 34. Bad Block Test Flow 54
13-3. Failure Phenomena for Read/Program/Erase Operations 54
Table 15. Failure Modes 54
14. DEVICE POWER-UP 55
14-1. Power-up 55
Figure 35. Power Up/Down and Voltage Drop 55
Table 16. Power-Up/Down Voltage and Timing 55
15. PARAMETERS 56
15-1. ABSOLUTE MAXIMUM RATINGS 56
Figure 36. Maximum Negative Overshoot Waveform 56
Figure 37. Maximum Positive Overshoot Waveform 56
15-2. LATCH-UP CHARACTERISTICS 56
Table 17. AC Testing Conditions 57
Table 18. Capacitance 57
Table 19. Operating Range 57
Figure 38. SCLK TIMING DEFINITION 57
Table 20. DC Characteristics 58
Table 21. General Timing Characteristics 58
Table 22. Program/ Read/ Erase Characteristics 59
Figure 39. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1 60
Figure 40. Serial Input Timing 60
Figure 41. Serial Output Timing 60
Figure 42. Hold Timing 61
16. PACKAGE INFORMATION 62
16-1. 8-WSON (8x6x0.8mm) 62

1. FEATURES

- **1Gb/2Gb/4Gb SLC NAND Flash**
  - Bus: x4
  - 1Gb/2Gb:
    Page size: (2048+128) byte,
    Block size: (128K+8K) byte
  - 4Gb: Page size: (4096+256) byte,
    Block size: (256K+16K) byte
- **8-bit ECC/ 544B is required**
- **Fast Read Access**
  - Supports data read by x1 x2 & x4 modes, (1-1-1,1-1-2, 1-1-4, 1-2-2, 1-4-4)[Note 1]
  - Latency of array to register: 25us
  - Frequency: 166 MHz (DC bit = 1 for 1-2-2 & 1-4-4 read modes above 108MHz)
- **Page Program Operation**
  - Page program time: 320us(typ.)
- **Block Erase Operation**
  - Block erase time: 4ms(typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 to 1.95V
- **BP bits for Block group protection**
- **Unique ID Read with PUF type code structure**
- **Low Power Dissipation**
  - Max. 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max.) standby current
- **Deep power-down mode**
  - 15uA (Max.)
- **High Reliability**
  - Randomizer (default disable): enabled by Set Feature
  - Special Read for data recovery : enabled by Set Feature
  - Program / Erase Endurance: Typical 60K cycles (with 8-bit ECC per 512+32) Byte
  - Data Retention: 10 years[Note2]
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  8-WSON (8x6mm)
  All packaged devices are RoHS Compliant and Halogen-free.

Notes:

1. Which indicates the number of I/O for command, address and data.

2. Please contact Macronix for Reliability report on the detailed condition of retention test.

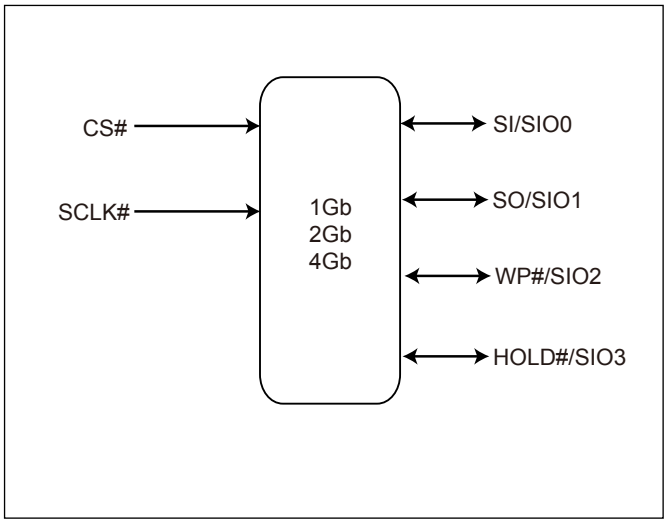
2. GENERAL DESCRIPTIONS

The MX35UFxG24AD is a 1Gb/2Gb/4Gb SLC NAND Flash memory device with Serial interface.

The memory array of this device adopted the same cell architecture as the parallel NAND, however implementing the industry standard serial interface.

The device needs the micro controller of host side to support 8-bit ECC/544-byte operation.

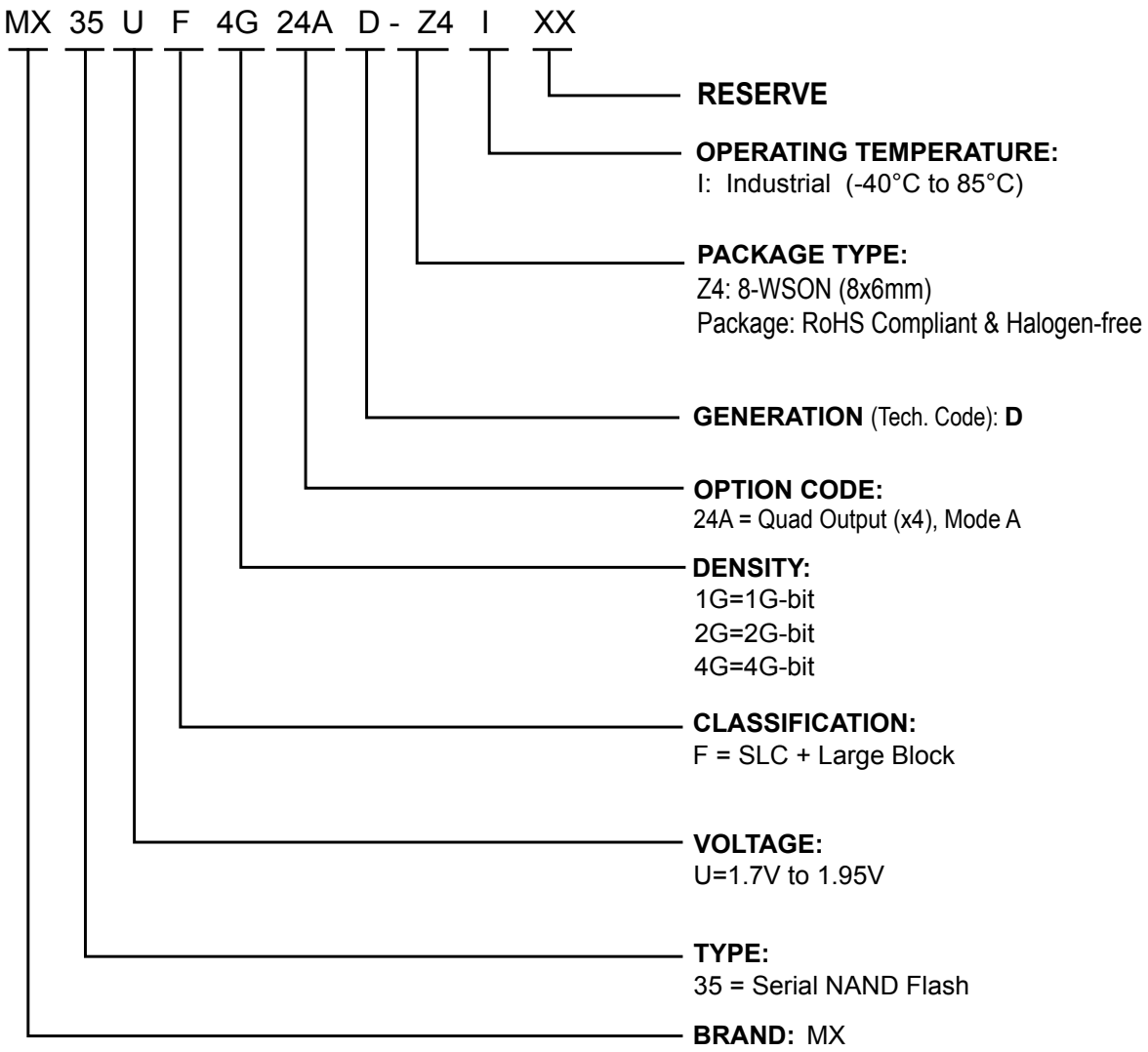
Figure 1. Logic Diagram



3. ORDERING INFORMATION

Part Name Description

Macronix NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Macronix's product search at http://www.Macronix.com. Contact Macronix sales for devices not found.

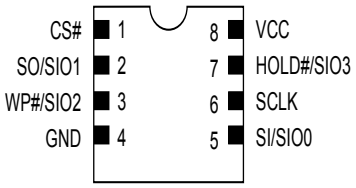


Please contact Macronix regional sales for the latest product selection and available form factors.

Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX35UF4G24AD-Z4I	4Gb	x4	1.8V	8-WSON	Industrial
MX35UF2G24AD-Z4I	2Gb	x4	1.8V	8-WSON	Industrial
MX35UF1G24AD-Z4I	1Gb	x4	1.8V	8-WSON	Industrial

4. BALL ASSIGNMENT AND DESCRIPTIONS

Figure 2. 8-WSON (8x6mm)



5. PIN DESCRIPTIONS

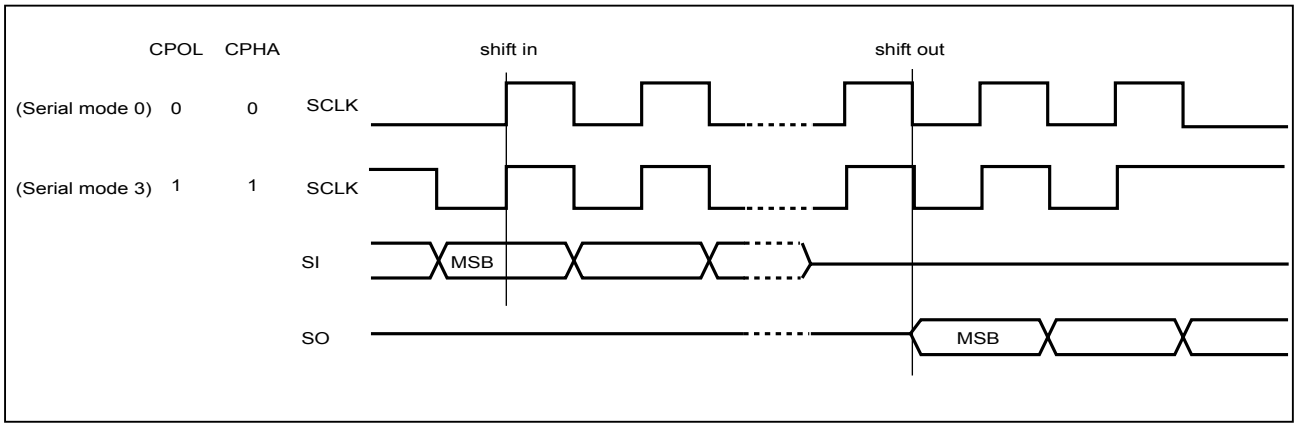
SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
HOLD#/SIO3	Hold or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
VCC	+ 1.8V Power Supply
GND	Ground

***Note 1**. Which indicates the number of I/O for command, address, and data.*

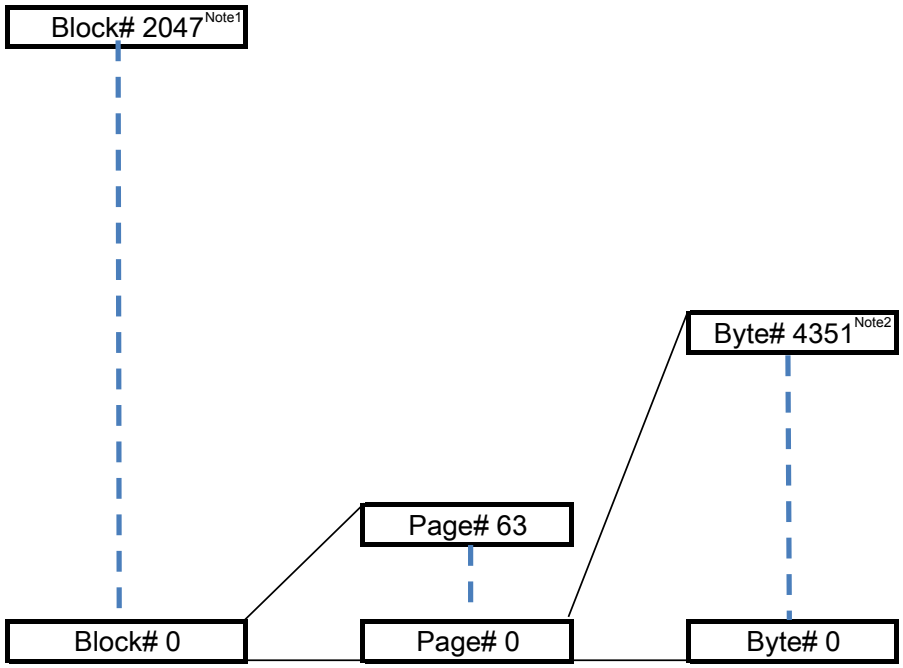
6. DEVICE OPERATION

1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When an incorrect command is written to this device, it enters standby mode and stays in standby mode until the next CS# falling edge. In standby mode, This device's SO pin should be High-Z.
3. When a correct command is written to this device, it enters active mode and stays in active mode until the next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as **"Figure 3. Serial Mode Supported"**.
5. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

Figure 3. Serial Mode Supported



7. ADDRESS MAPPING



Block address	Page address	Byte address
RA [16:6]	RA [5:0]	CA [12:0]Note3

Note1: **1023 for 1Gb**

Note2: **Byte#=2175 for 1Gb/2Gb**

Note3: **CA[11:0] for 1Gb/2Gb**

8. COMMAND DESCRIPTION

Table 1. Command Set

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte
Get Feature	0Fh	ADD	Data			
Read Status	05h	Data				
Set Feature	1Fh	ADD	Data			
Page Read	13h	RADD2	RADD1	RADD0		
Page Read cache random	30h	RADD2	RADD1	RADD0		
Page Read cache sequential	31h					
Page Read cache last	3Fh					
Read From Cache x1	03h	CADD1	CADD0	DUMMY	DATA~	
Read From Cache x1 (alternative)	0Bh	CADD1	CADD0	DUMMY	DATA~	
Read From Cache x2Note	3Bh	CADD1	CADD0	DUMMY	DATA~(2)	
Read From Cache x4Note	6Bh	CADD1	CADD0	DUMMY	DATA~(4)	
Read From Cache Dual IO 1-2-2Note	BBh	CADD1(2)	CADD0(2)	DUMMY(2)	DATA~(2)	
Read From Cache Quad IO 1-4-4Note	EBh	CADD1(4)	CADD0(4)	DUMMY(4)	DUMMY(4)	DATA~(4)
Read ID	9Fh	DUMMY	MID	DID1	DID2	
Block Erase	D8h	RADD2	RADD1	RADD0		
Program execute	10h	RADD2	RADD1	RADD0		
Program Load x1	02h	CADD1	CADD0	DATA~		
Program Load random data x1	84h	CADD1	CADD0	DATA~		
Program Load x4Note	32h	CADD1	CADD0	DATA~(4)		
Program Load random data x4Note	34h	CADD1	CADD0	DATA~(4)		
Write enable	06h					
Write disable	04h					
Reset	FFh					
Enter Deep Power-down mode	B9h					

Note: *(2) stands for the dual I/O mode and (4) for quad I/O mode*

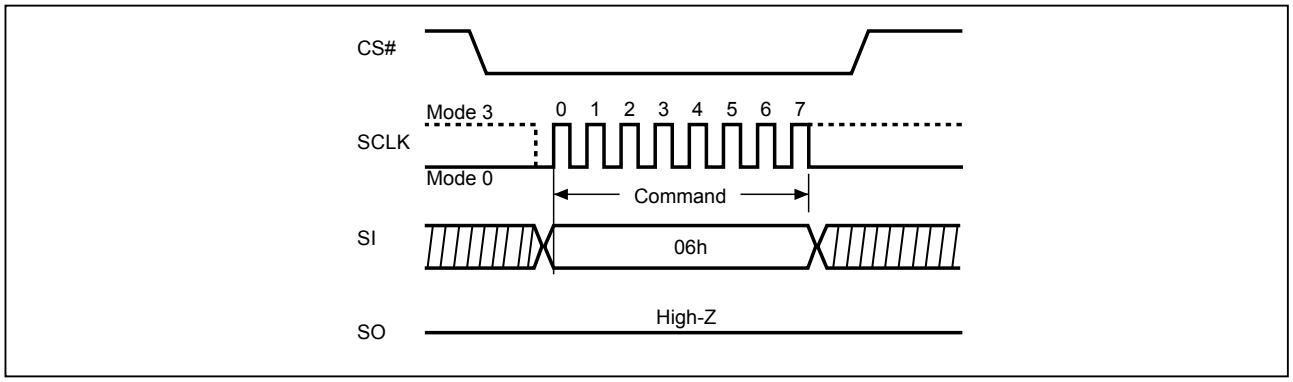
8-1. WRITE Operations

8-1-1.Write Enable

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit. Instructions like Page Program, Secure OTP program, and Block Erase that are intended to change the device content, should be preceded by the WREN instruction

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

Figure 4. Write Enable (WREN) Sequence



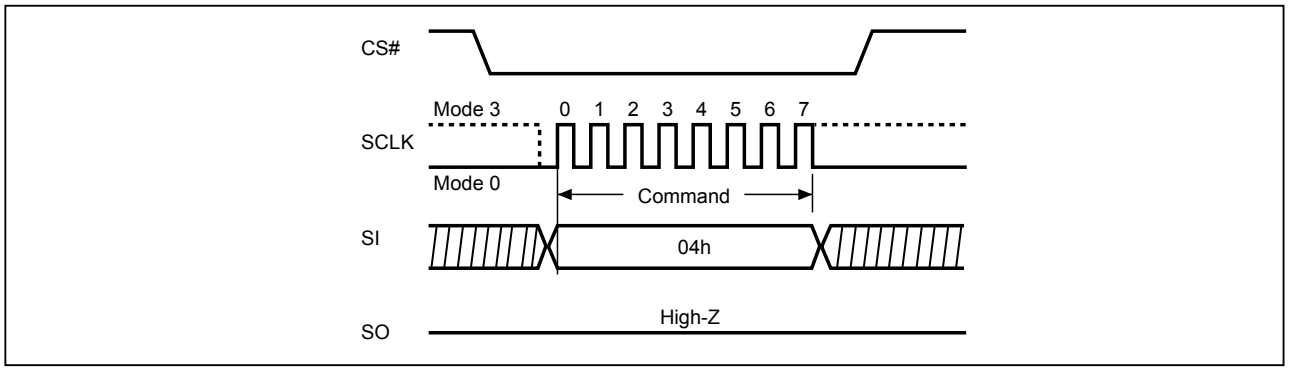
8-1-2.Write Disable (04h)

The Write Disable (WRDI, 04h) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high. It disables the following operations:

- Block Erase
- Secure OTP program
- Page program

Figure 5. Write Disable (WRDI) Sequence



8-2. Feature Operations

8-2-1.GET Feature (0Fh) and SET Feature (1Fh)

By issuing a one byte address into the feature address, the device may then decide if it's a feature read or feature modification. (0Fh) is for the "GET FEATURE"; (1Fh) is for the "SET FEATURE".

The RESET command (FFh) will clear the status and special read for data recovery registers, the other feature registers remain until the power is being cycled or modified by the settings in the table below. After a RESET command (FFh) is issued, the Status register OIP bit0 or CRBSY will go high. These bits can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the RESET command (FFh) has no effect on the Block Protection and Configuration registers.

The Block Protection and Configuration registers will return to their default state after a power cycle, and can also be changed using the Set Feature command. Issuing the Get Feature command to read the selected register value will not affect register content.

Table 2. Configuration Registers

ADD	Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
10h	Configuration	bit name						RANDOPT	RANDEN	ENPGM	00h
		Type						V2	V2	V	
60h	Configuration	bit name							SPI_NOR_EN	OTPRWSP	00h
		Type							OTP	OTP	
70h	Special Read for Data Recovery	bit name						SPEC_RD2	SPEC_RD1	SPEC_RD0	00h
		Type						V	V	V	
A0h	Block Protection	bit name	BPRWD[1]		BP2	BP1	BP0	Invert	Comp.	SP[2]	38h
		Type	V2		V2	V2	V2	V2	V2	V2	
B0h	Configuration	bit name	OTP_PROT	OTPEN						QE	00h
		Type	V	V						V2	
C0h	Status	bit name	CRBSY				PGM-FAIL	ERS_FAIL	WEL	OIP	00h
		Type	V				V	V	V	V	
D0h	Configuration	bit name		DS[3]							00h
		Type		V							
E0h	Configuration	bit name	DS_IO[1]	DS_IO[0]				DC			00h
		Type	V2	V2				V2			

V: Volatile.

V2: Volatile, the default value of these volatile feature bits can be changed once by Special OTP Configuration Register Program Operation.

OTP: One time setting.

Note 1: *If BPRWD is enabled and WP# is LOW, then the block protection register cannot be changed.*

Note 2: *SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of the protection bits (BPx bits, Invert bits, complementary bits) cannot be changed during the current power cycle.*

Note 3: *DS bit is reserved for the purpose of stacked die as 8Gb.*

Table 3. I/O Strength Feature Table

DS_IO[1]	DS_IO[0]	Drive Strength
0	0	normal (default, 20 ohm typical)
0	1	underdrive 1 (25 ohm typical)
1	0	underdrive 2 (35 ohm typical)
1	1	underdrive 3 (85 ohm typical)

Figure 6. GET FEATURE (0Fh) Timing

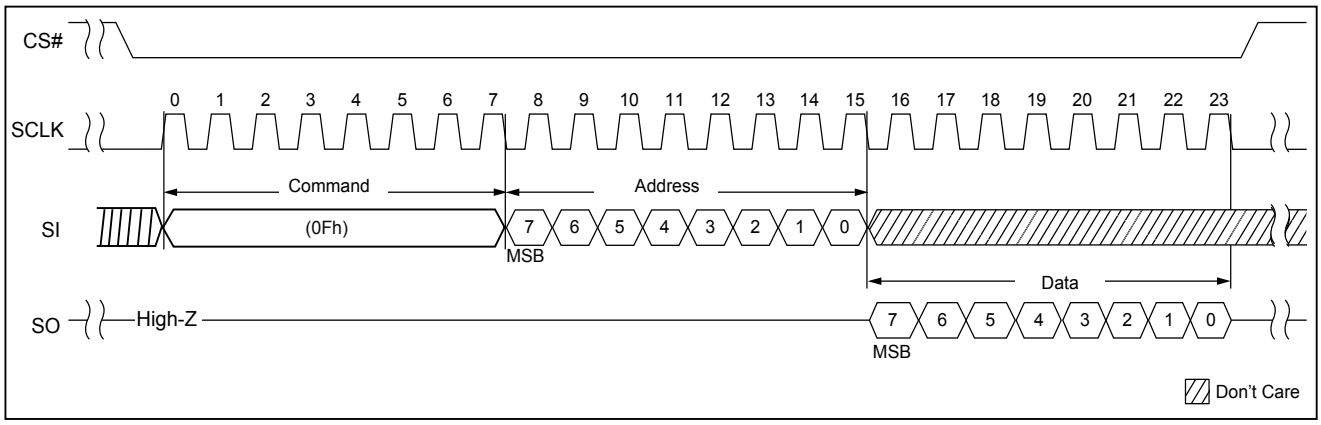
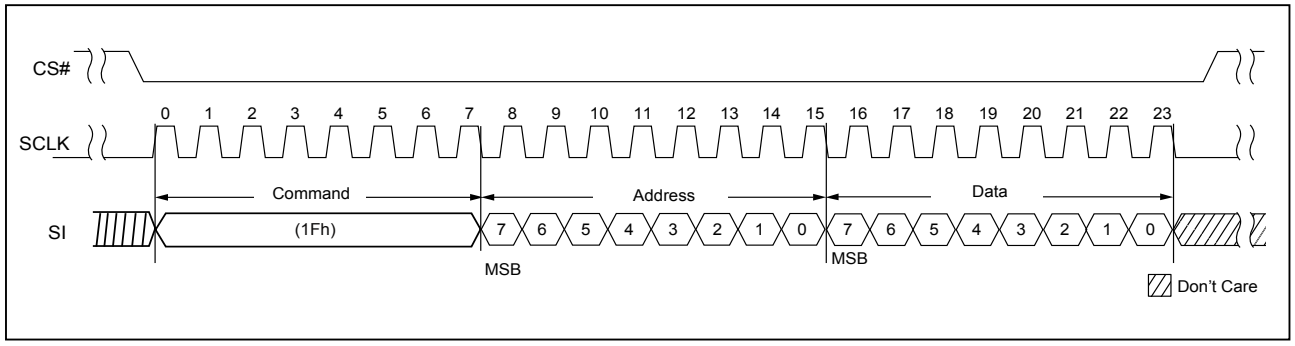


Figure 7. SET FEATURE (1Fh) Timing



8-3. READ Operations

The device supports "Power-on Read" function, after power up, host may issue the Read From Cache command, and the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer.

The device supports the page read operation and page read cache Random/sequential operation.

8-3-1.PAGE READ (13h)

The page read operation transfers data from array to cache by issuing the page read (13h) command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) or 05h (RDSR) may be used to poll the operation status.

After read operation is completed, the Read from cache (03H or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh), read from cache dual IO (1-2-2) (BBh) and Read from cache Qual IO (1-4-4) (EBh) may be issued to fetch the data.

8-3-2.QE Bit

The Quad Enable (QE) bit, volatile bit and the default value can be changed once, while it is "0", it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the feature of Hardware Protection Mode(HPM) and HOLD will be disabled. Upon power cycle, the QE bit will go into the default setting "0". The default value can be changed by the Special OTP Configuration Register Program Operation, the factory default value is "0" while shipping.

8-3-3.DC Bit (Dummy Cycle Option Bit)

The Dummy cycle option bit allows user to define the dummy cycle numbers for the read from cache command operation (1-2-2, 1-4-4 mode). There will be two options: 4 dummy cycles for SPI clock rate of max. 108MHz, or 8 dummy cycle numbers for high SPI clock rate up to 166MHz. The DC bit is a volatile bit with its default value can be changed once by the Special OTP Configuration Register Program. The factory default value is “0” while shipping.

Figure 8. PAGE READ (13h) Timing x1

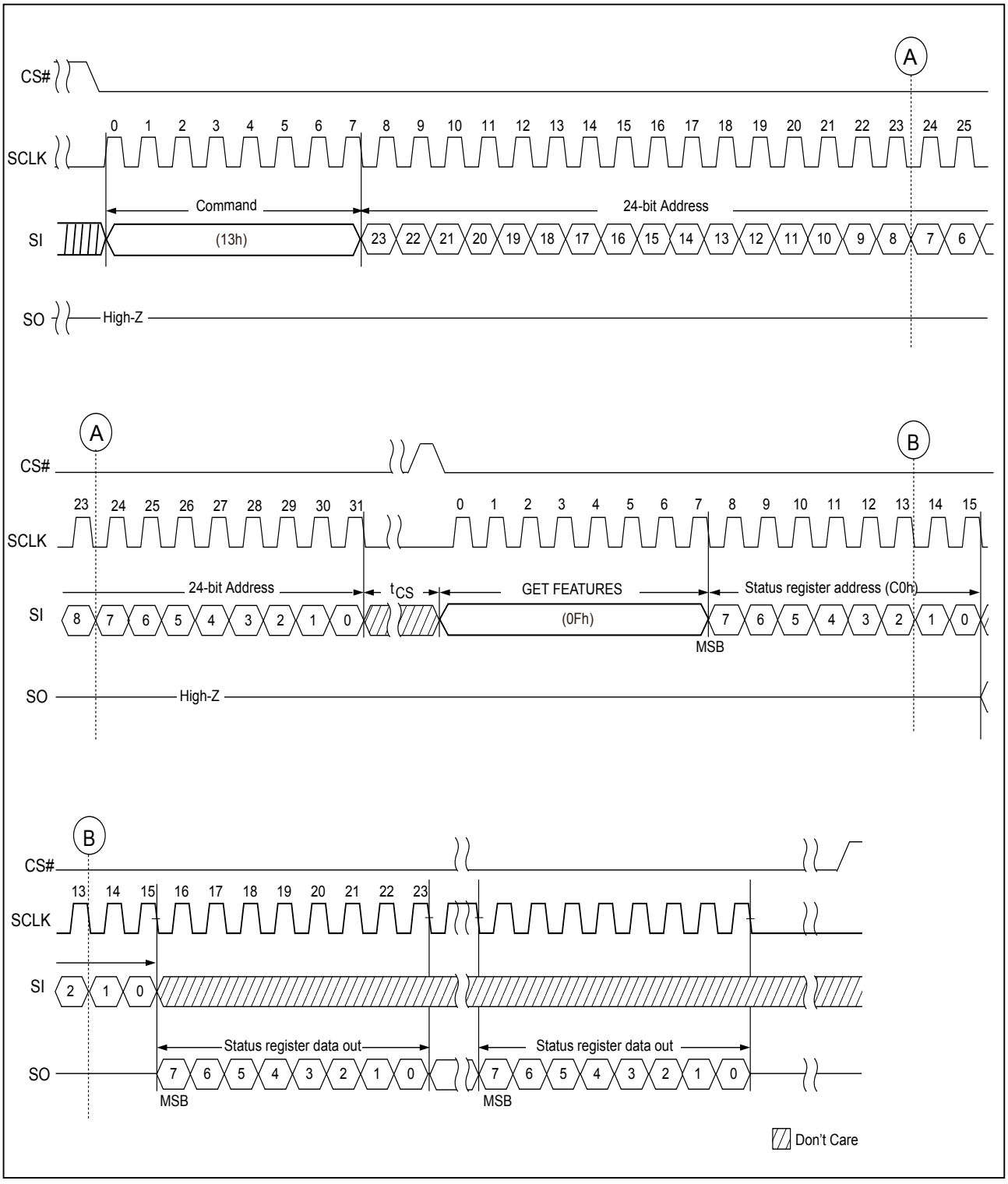
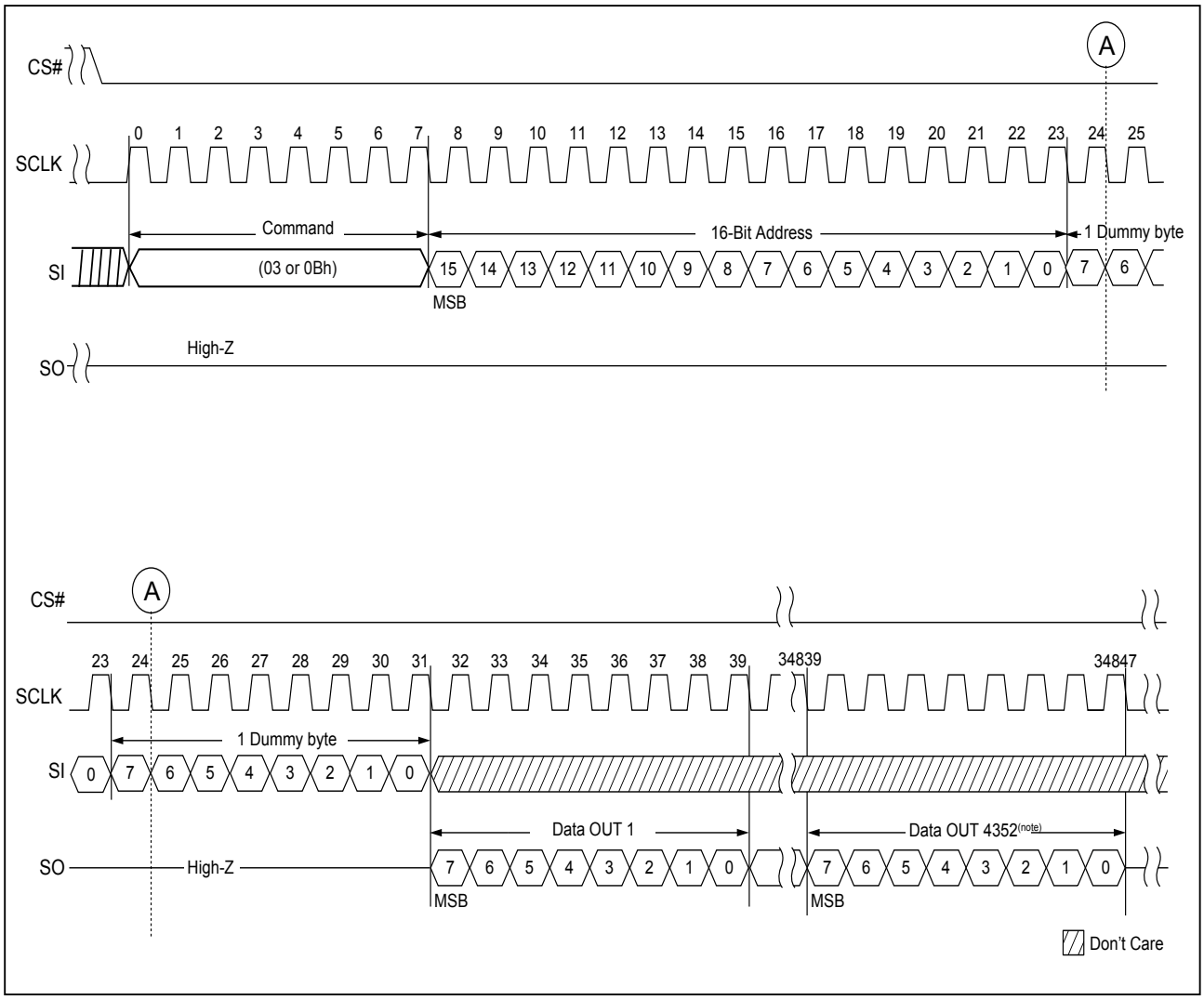
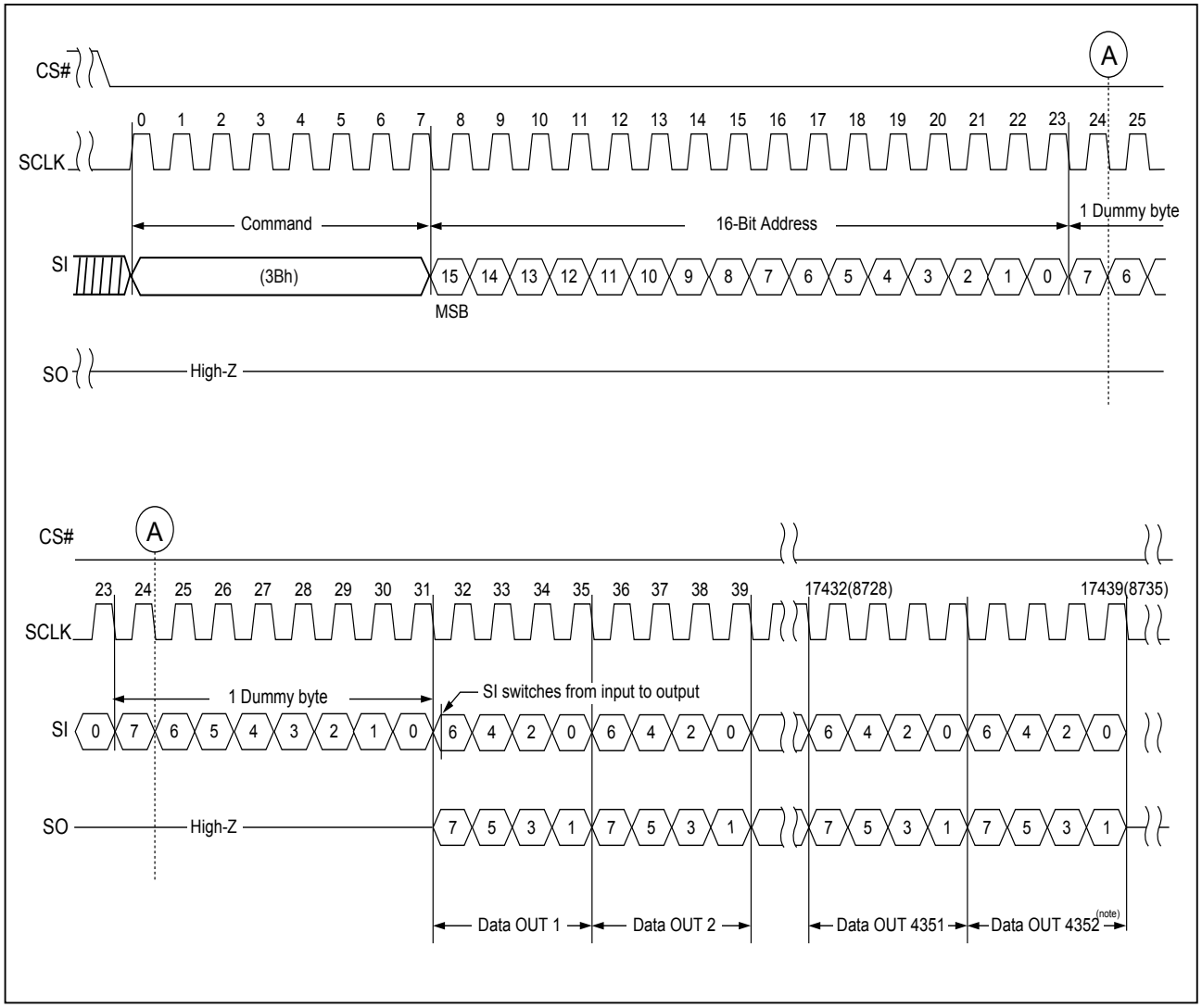


Figure 9. READ FROM CACHE (03h or 0Bh) Timing



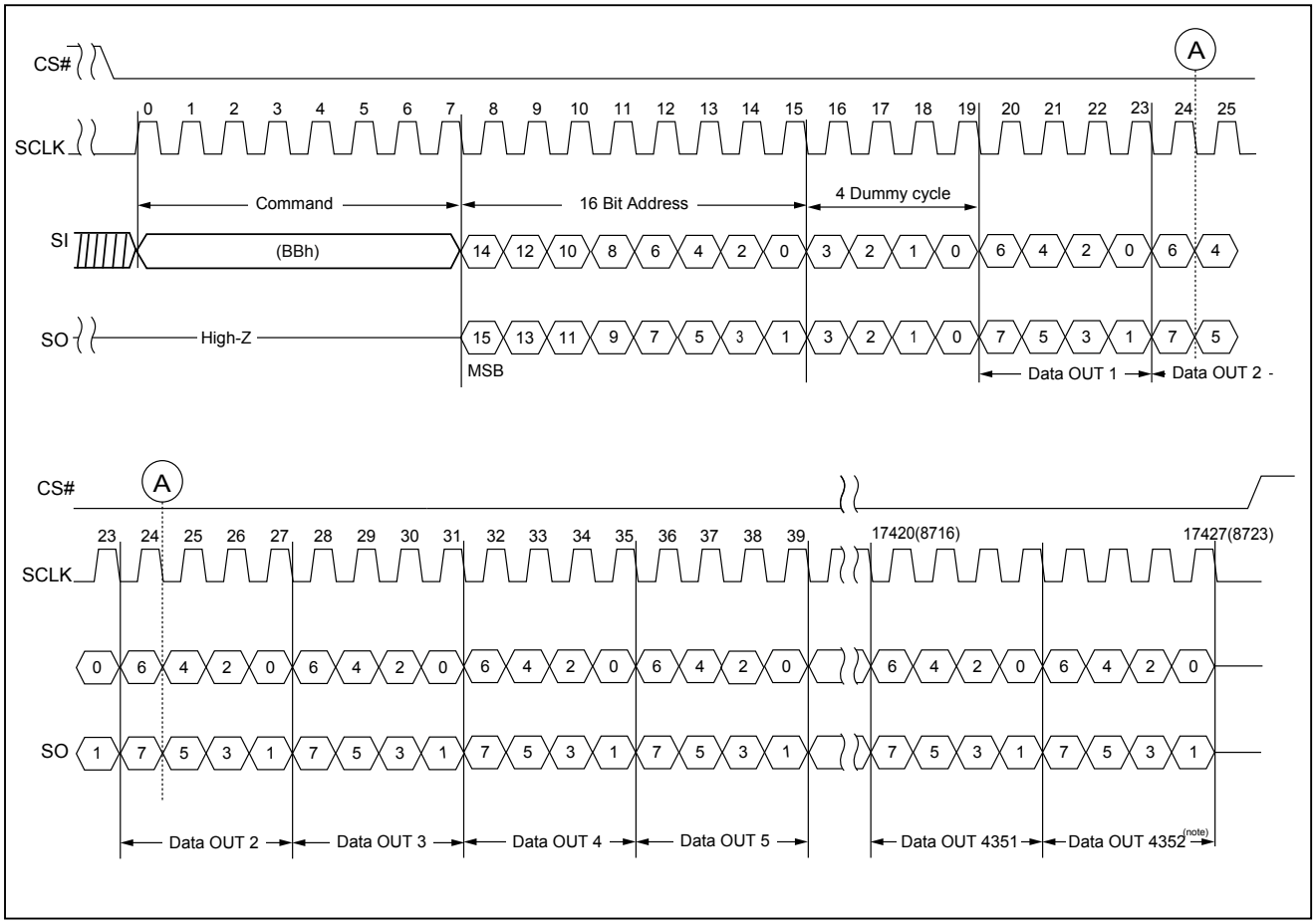
***Note**: Data byte is 2176 for 1Gb/2Gb.*

Figure 10. READ FROM CACHE x 2



Note*: *Data byte is 2176 for 1Gb/2Gb.

Figure 11. Read From Cache Dual IO 1-2-2 (DC bit = 0)



Note*: *Data byte is 2176 for 1Gb/2Gb.

Figure 12. READ FROM CACHE x 4

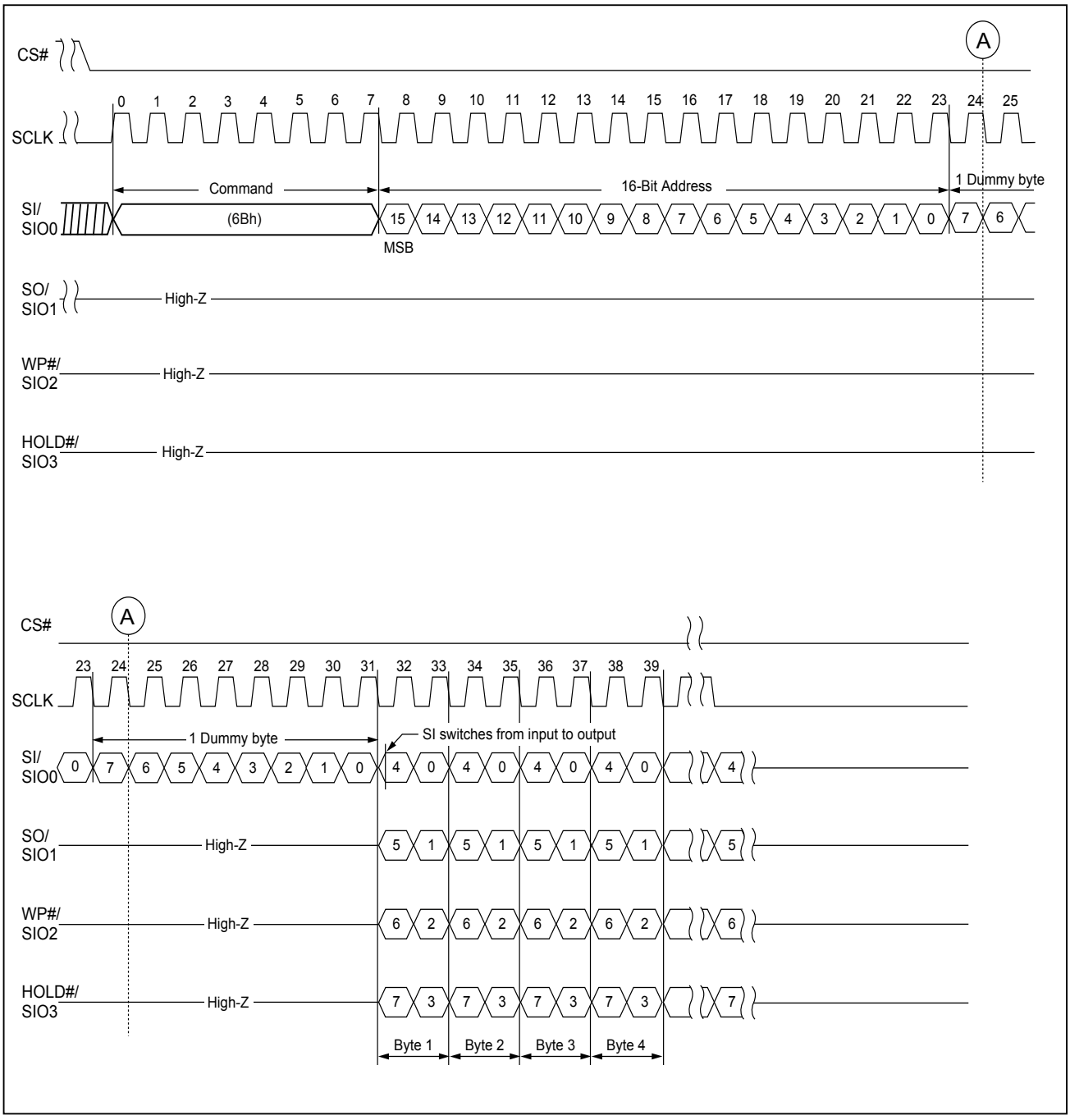
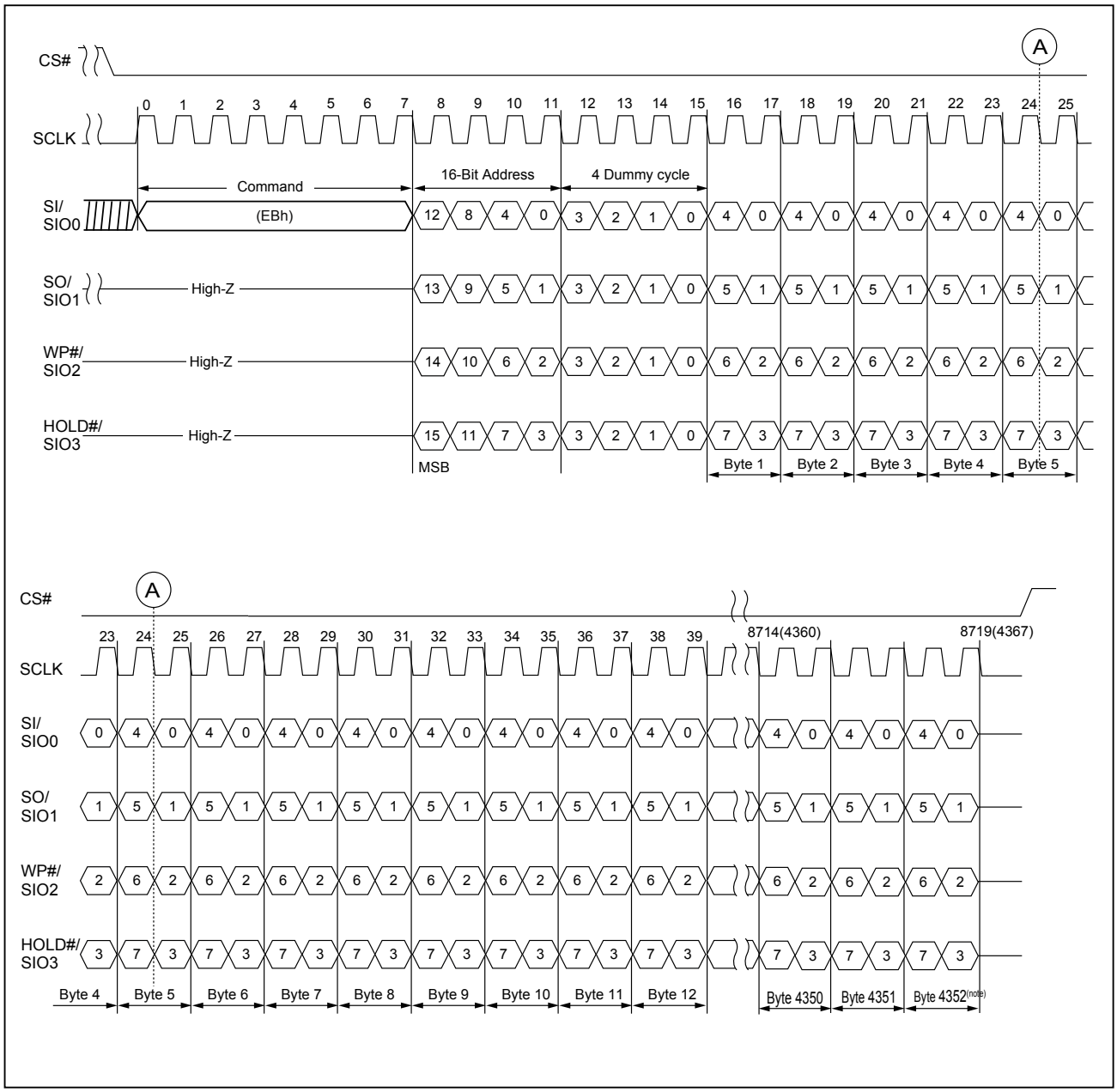


Figure 13. Read From Cache Quad IO 1-4-4 (DC bit = 0)



Note*: *Data byte is 2176 for 1Gb/2Gb.

8-3-4.Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh)

The page read cache sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tRD to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 13h command and giving the 24-bit address, the device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) or 05h (RDSR) may be used to poll the operation status. After the status of successfully completed, following the page read cache sequential (31h) or the page read cache random (30h) command being sent to NAND device; the NAND device will be at a busy time of tRCBSY for the next page data transferring to cache. And then following the cache read command (03h/0Bh/3Bh/6Bh/BBh/EBh) may get the prior page data output from cache at the same time.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h or 30h command prior to the last data-out.

The PAGE READ CACHE SEQUENTIAL command is also valid for the consecutive page cross block.

Figure 14. Page Read Cache Random (30h)

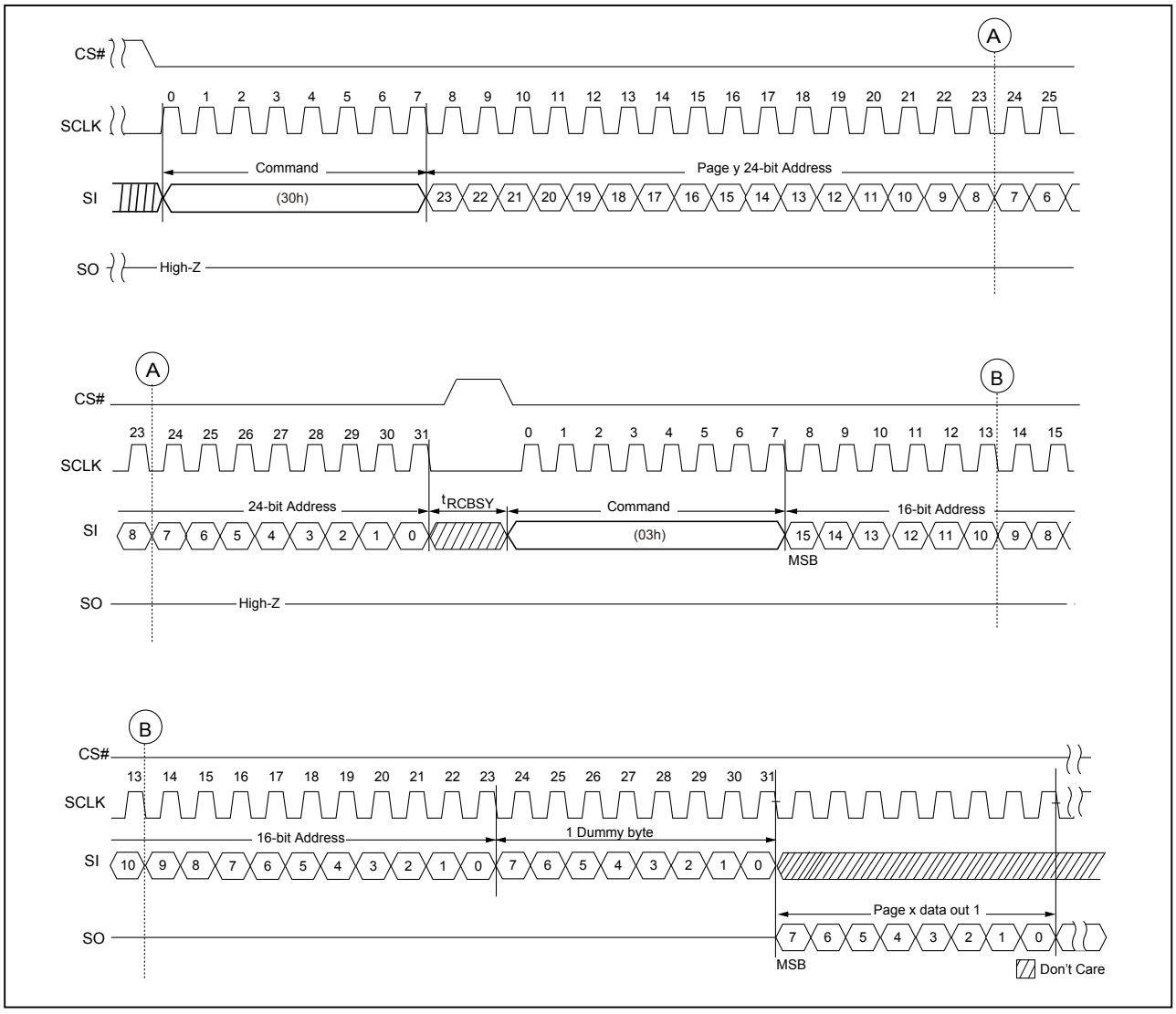


Figure 15. Page Read Cache Sequential (31h)

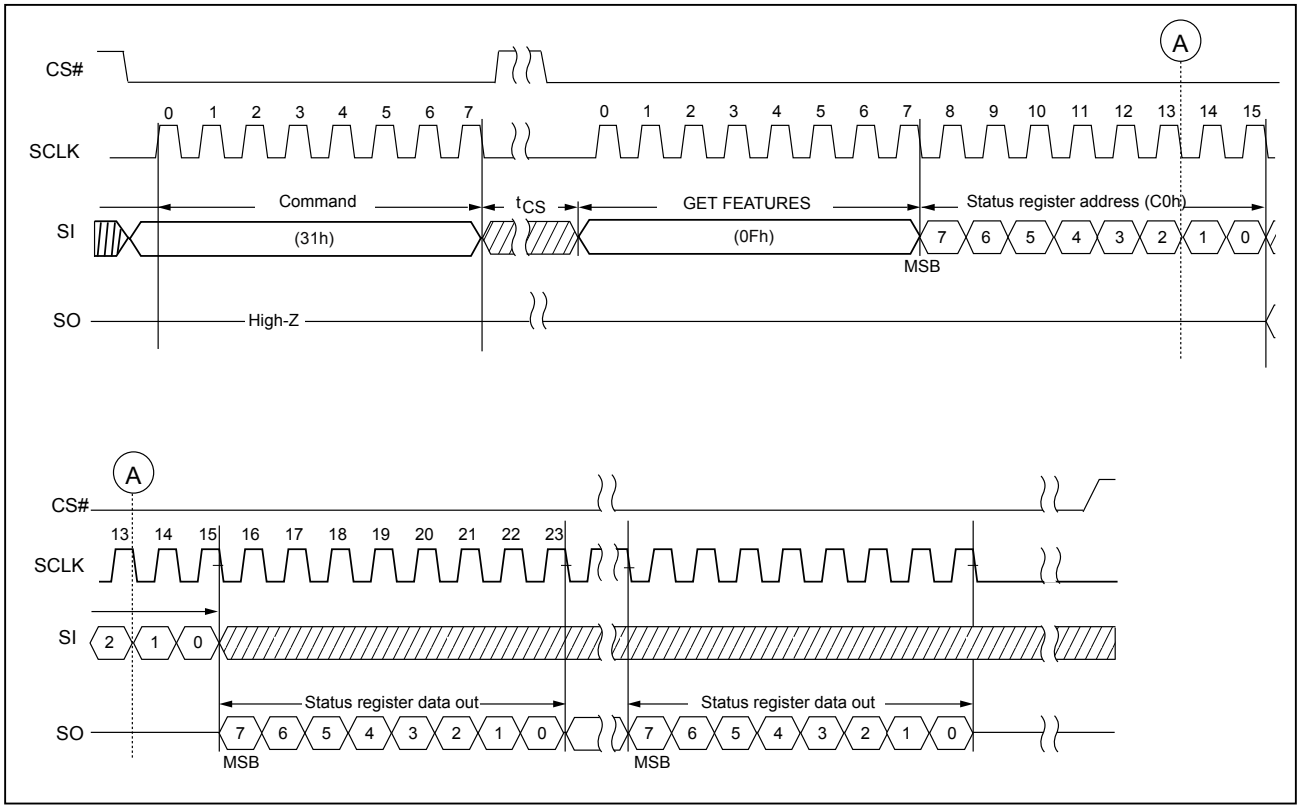


Figure 16. Page Read Cache End (3Fh)

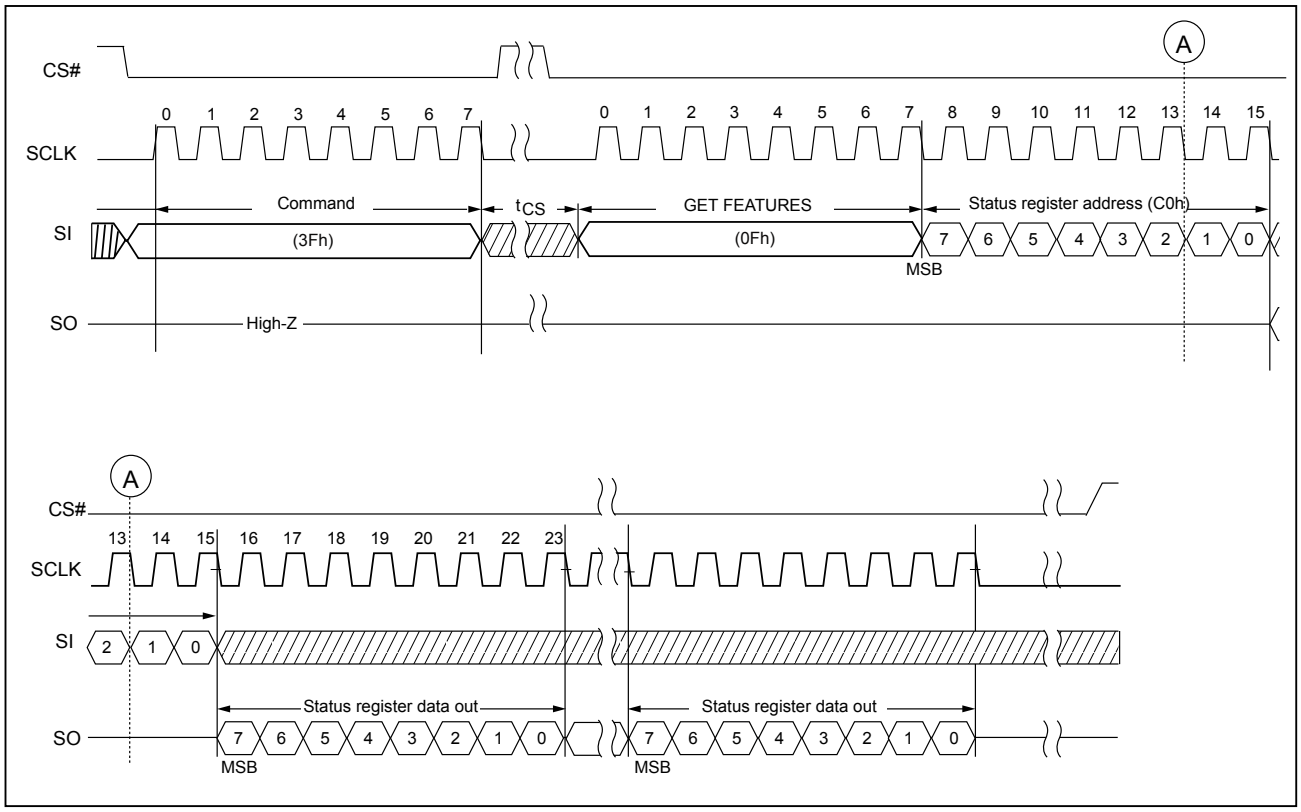
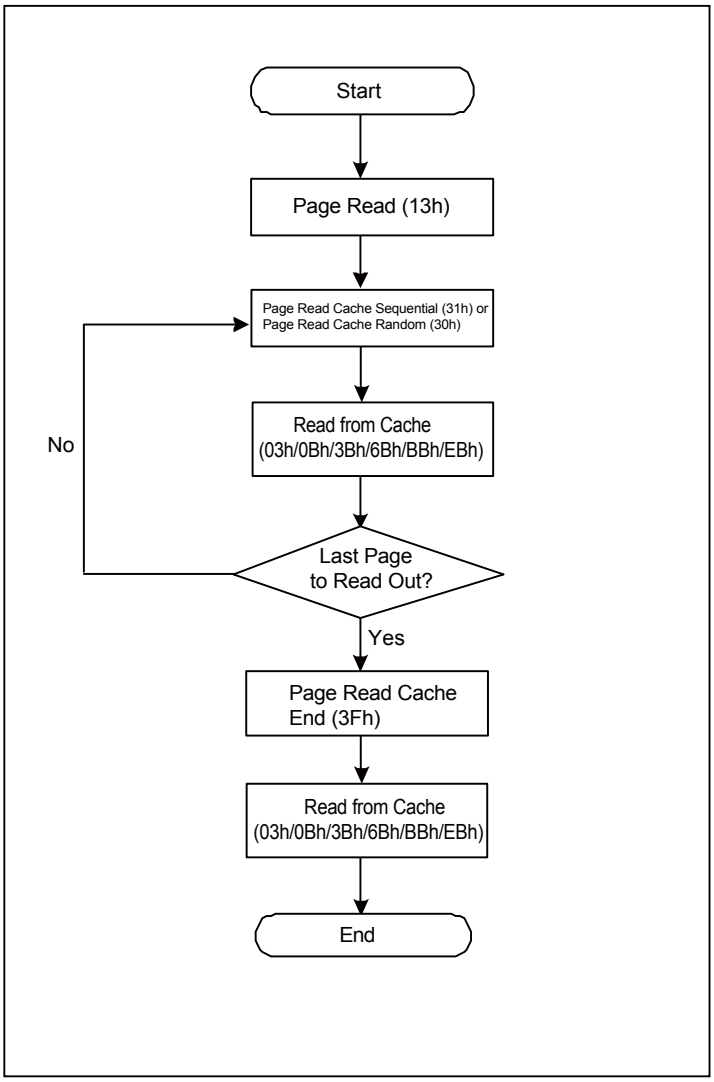


Figure 17. Page Read Cache Flow



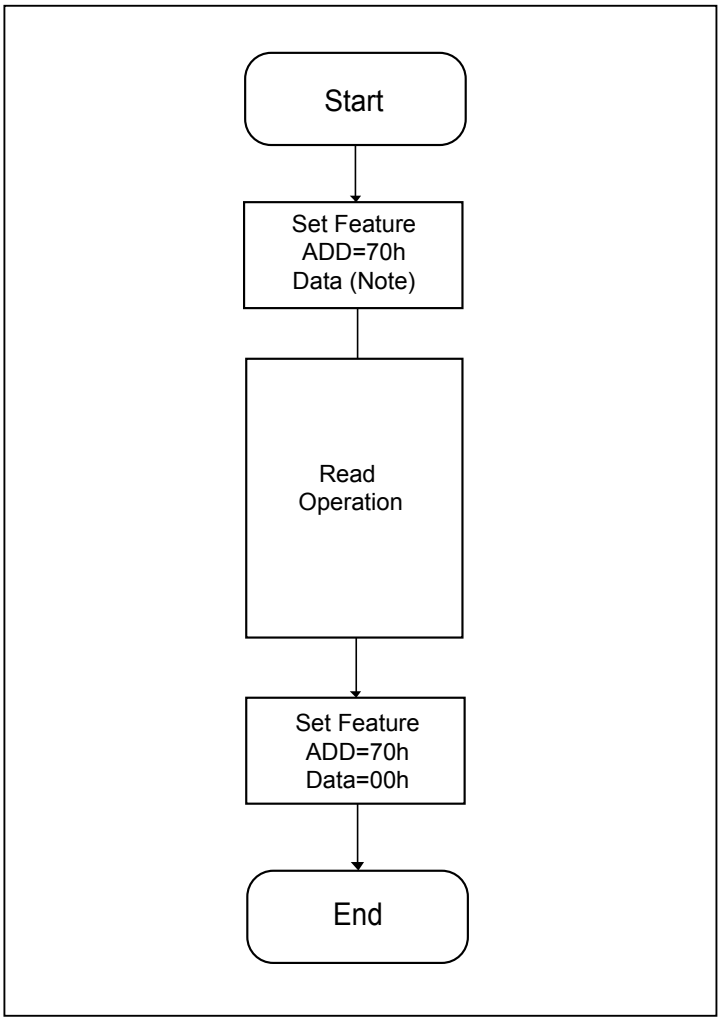
8-3-5.Special Read for Data Recovery

When the host ECC fails to correct the data error of NAND device, there's a special read for data recovery method which host executes the Special Read for Data Recovery operation and may recover the lost data by host ECC again. After that, it is needed to move the data to another good block.

The Special Read for Data Recovery operation is enabled by Set Feature function (**"Table 4. Feature Settings"**).

There are 5 modes for the user to recover the lost data. The procedure of entering and exiting the operation is shown as Figure below.

Figure 18. Procedure of Entering/Exiting the Special Read for Data Recovery operation



Note: Please refer to **"Table 4. Feature Settings"**.

Table 4. Feature Settings

Definition		SPEC_RD2	SPEC_RD1	SPEC_RD0	Value
Special Read for Data Recovey	Disable (Default)	0	0	0	00h
	Mode 1	0	0	1	01h
	Mode 2	0	1	0	02h
	Mode 3	0	1	1	03h
	Mode 4	1	0	0	04h
	Mode 5	1	0	1	05h

8-3-6.Randomizer Operation

The randomizer function is enabled on the NAND device, the user data and OTP area are scrambled in random pattern before written to the NAND device. When attempting to use the randomizer function, it is necessary to enable the randomizer function prior to program data in main array and OTP area. The randomizer function is enabled through “set feature” operation (as **"Table 2. Configuration Registers"**). The following feature bits RANDEN and RANDOPT is related with randomizer function (as **"Table 2. Configuration Registers"**)

To enable the randomizer function, RANDEN bit must be set to “1”, RANDOPT can be set to “0” or “1” depending on the user choice (as **"Table 5. The definition of RANDOPT bit for the randomized area per page"** (as grey color).

Both RANDEN and RANDOPT feature bits are volatile bits with their default value can be changed once with the Special OTP Configuration Register Program Operation. The RANDEN and RANDOPT bits will return to their default value after power cycle. The RANDEN and RANDOPT bits program flowchart is shown on the **"Figure 30. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)"**.

RANDOPT bit: considering the needs of different applications; there are two options of randomizer coverage providing (as **"Table 5. The definition of RANDOPT bit for the randomized area per page"** (as grey color" shown. The grey data area is covered by the randomizer function for each option; whereas the white area is not.

Note: *the NOP=1 for the randomizer covered data area.*

Table 5. The definition of RANDOPT bit for the randomized area per page

(As grey color)

Density	RANDOPT	Main	Spare 0	Spare 1	Remark
1G/2G	0	0000h~07FFh	0800h~081Fh	0820h~087Fh	NOP=1 for Main/Spare 0/Spare 1
	1	0000h~07FFh	0800h~081Fh	0820h~087Fh	NOP=1 for Main/Spare 1

Density	RANDOPT	Main	Spare 0	Spare 1	Remark
4G	0	0000h~0FFFh	1000h~101Fh	1020h~10FFh	NOP=1 for Main/Spare 0/Spare 1
	1	0000h~0FFFh	1000h~101Fh	1020h~10FFh	NOP=1 for Main/Spare 1

9. SPI NOR Compatible Command

Considering some SoC(or MCU) of host system must adopt the read protocol of SPI NOR like, this device provide the SPI_NOR_EN of configuration register bit to enable the read protocol of SPI NOR like for Read From Cache commands. The SPI_NOR_EN bit is OTP type once it is enable and cannot disable.

It is recommended to set the SPI_NOR_EN bit by programmer machine in advance before power on while attempts to adopt the read protocol of SPI NOR like.

Please refer to the **"Figure 30. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)"**.

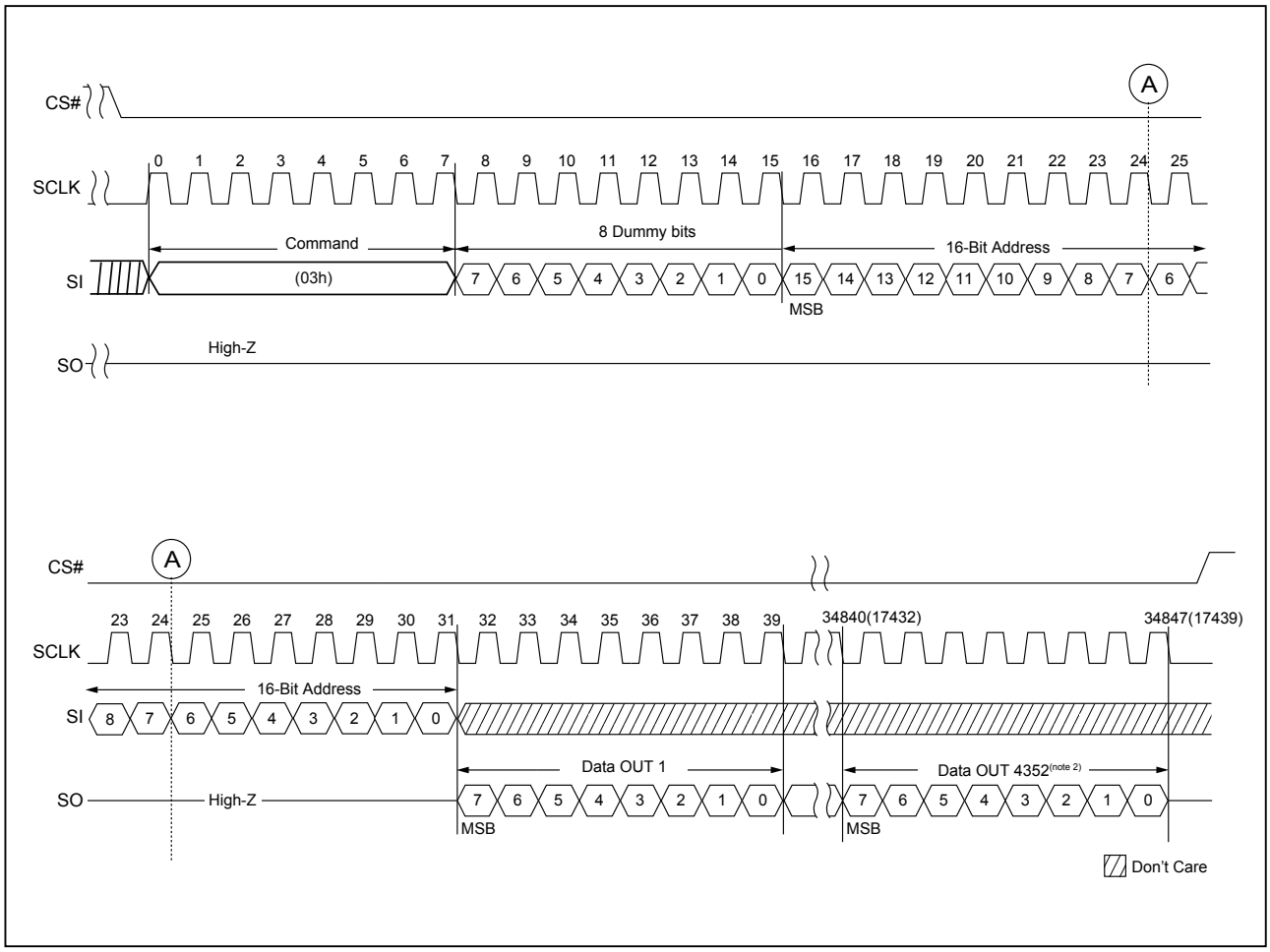
Table 6. Command Set - SPI NOR Like Protocol Enabled

(**SPI_NOR_EN = 1**)

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte
Get Feature	0Fh	ADD	**Data**			
Read Status	05h	Data				
Set Feature	1Fh	ADD	Data			
Page Read	13h	RADD2	RADD1	RADD0		
Page Read Cache Random	30h	RADD2	RADD1	RADD0		
Page Read Cache Sequential	31h					
Page Read Cache Last	3Fh					
Read From Cache x1	03h	DUMMY	CADD1	CADD0	DATA~	
Read From Cache x1 (Alternative)	0Bh	DUMMY	CADD1	CADD0	DUMMY	DATA~
Read From Cache x2[Note]	3Bh	CADD1	CADD0	DUMMY	DATA~[*2]	
Read From Cache x4[Note]	6Bh	CADD1	CADD0	DUMMY	DATA~[*4]	
Read From Cache Dual IO 1-2-2[Note]	BBh	CADD1[*2]	CADD0[*2]	DUMMY[*2]	DATA~[*2]	
Read From Cache Quad IO 1-4-4[Note]	EBh	CADD1[*4]	CADD0[*4]	DUMMY[*4]	DUMMY[*4]	DATA~[*4]
Read ID	9Fh	DUMMY	MID	DID1	DID2	
Block Erase	D8h	RADD2	RADD1	RADD0		
Program Execute	10h	RADD2	RADD1	RADD0		
Program Load x1	02h	CADD1	CADD0	DATA~		
Program Load Random Data x1	84h	CADD1	CADD0	DATA~		
Program Load x4[Note]	32h	CADD1	CADD0	DATA~[*4]		
Program Load Random Data x4[Note]	34h	CADD1	CADD0	DATA~[*4]		
Write Enable	06h					
Write Disable	04h					
Reset	FFh					
Enter Deep Power-down mode	B9h					

Note: **2 stands for the dual I/O phase and *4 for quad I/O mode.*

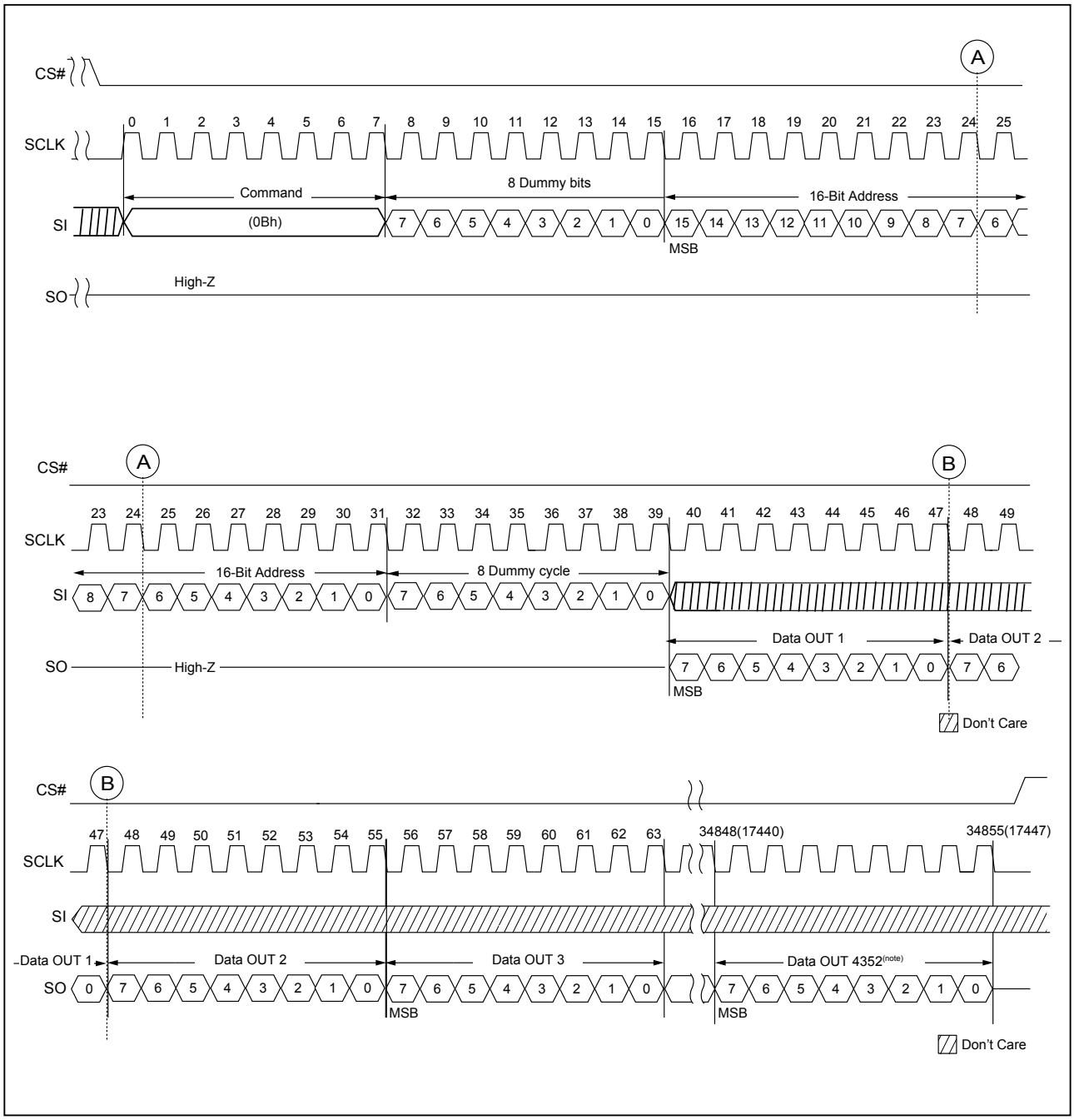
Figure 19. Read From Cache x1 (NOR like)



***Note 1**: For SPI NOR Like Protocol command, the Read From Cache command (03h) can run up to 20MHz only.*

***Note 2**: Data byte is 2176 for 1Gb/2Gb.*

Figure 20. Read From Cache x1 (Alternative, NOR like)



Note*: *Data byte is 2176 for 1Gb/2Gb.

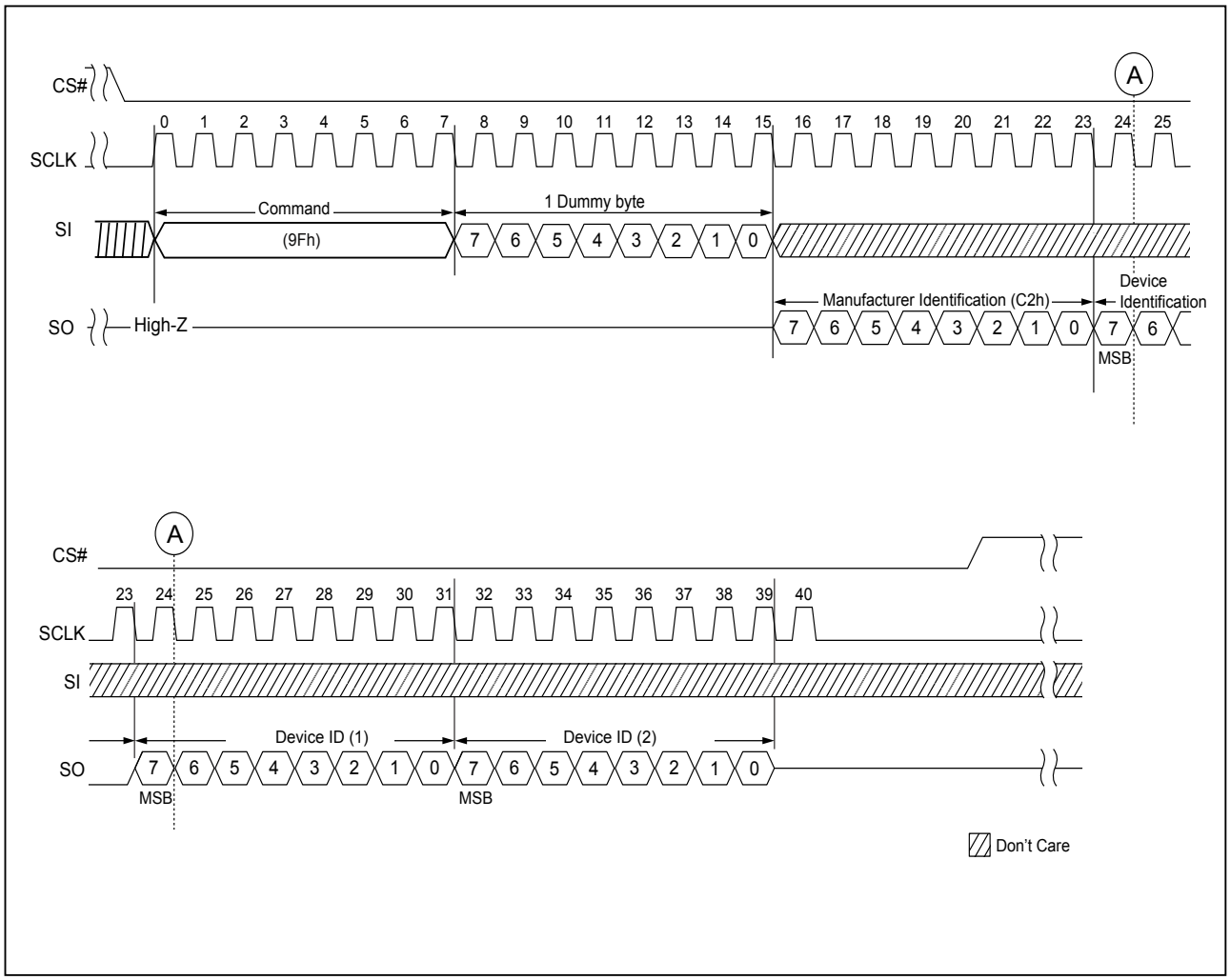
9-3-1.READ ID (9Fh)

The READ ID command is shown as the table below.

Table 7. READ ID Table

Byte	Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Macronix)		1	1	0	0	0	0	1	0	C2h
Byte 1	Device ID 1	1Gb	1	0	0	1	0	1	0	0	94h
		2Gb	1	0	1	0	0	1	0	0	A4h
		4Gb	1	0	1	1	0	1	0	1	B5h
Byte 2	Device ID 2		0	0	0	0	0	0	1	1	03h

Figure 21. READ ID (9Fh) Timing



9-1. Parameter Page

The parameter page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 01h address, issue 0Fh (GET FEATURE) with C0h feature address or 05h (RDSR) to poll the status of read completion. → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP feature (data byte = 00h) [exit parameter page read].

Table 8. Parameter Page Data Structure (MX35UF1G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		26h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35UF1G24AD	4Dh, 58h, 33h, 35h, 55h, 46h, 31h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	128-byte	80h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	32-byte	20h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 04h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		14h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		00h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of special read for data recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

Table 9. Parameter Page Data Structure (MX35UF2G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		26h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35UF2G24AD	4Dh, 58h, 33h, 35h, 55h, 46h, 32h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	128-byte	80h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	32-byte	20h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		01h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of special read for data recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

Table 10. Parameter Page Data Structure (MX35UF4G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		26h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35UF4G24AD	4Dh, 58h, 33h, 35h, 55h, 46h, 34h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	4096-byte	00h, 10h, 00h, 00h
84-85	Number of Spare Bytes per Page	256-byte	00h, 01h
86-89	Number of Data Bytes per Partial Page	1024-byte	00h, 04h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	64-byte	40h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		01h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of special read for data recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte
2048+	Additional Redundant Parameter Pages		

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

9-2. UniqueID Page with PUF Type Code Structure

The UniqueID page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 00h address, issue 0Fh (GET FEATURE) with C0h feature address or 05h (RDSR) to poll the status of read completion → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP function (data byte = 00h) [exit unique ID read].

The unique ID adopts Macronix PUF-like code structure, which is truly random and the numbers of "0" bit almost equal to numbers of "1" bit. The unique ID is 32-byte and with 16 copies for back-up purpose. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, the host needs to repeat the XOR with the next copy of Unique ID data.

9-3. Program Operations

9-3-1.PAGE PROGRAM

With following operation sequences, the PAGE PROGRAM operation programs the page from byte 1 to byte 2176(for 1Gb/2Gb) or 4352(for 4Gb).

WRITE ENABLE (06h) → PROGRAM LOAD (02h) → PROGRAM LOAD RANDOM DATA (84h) if needed → PROGRAM EXECUTE (10h) → GET FEATUR from command to read status (0Fh) or RDSR (05h).

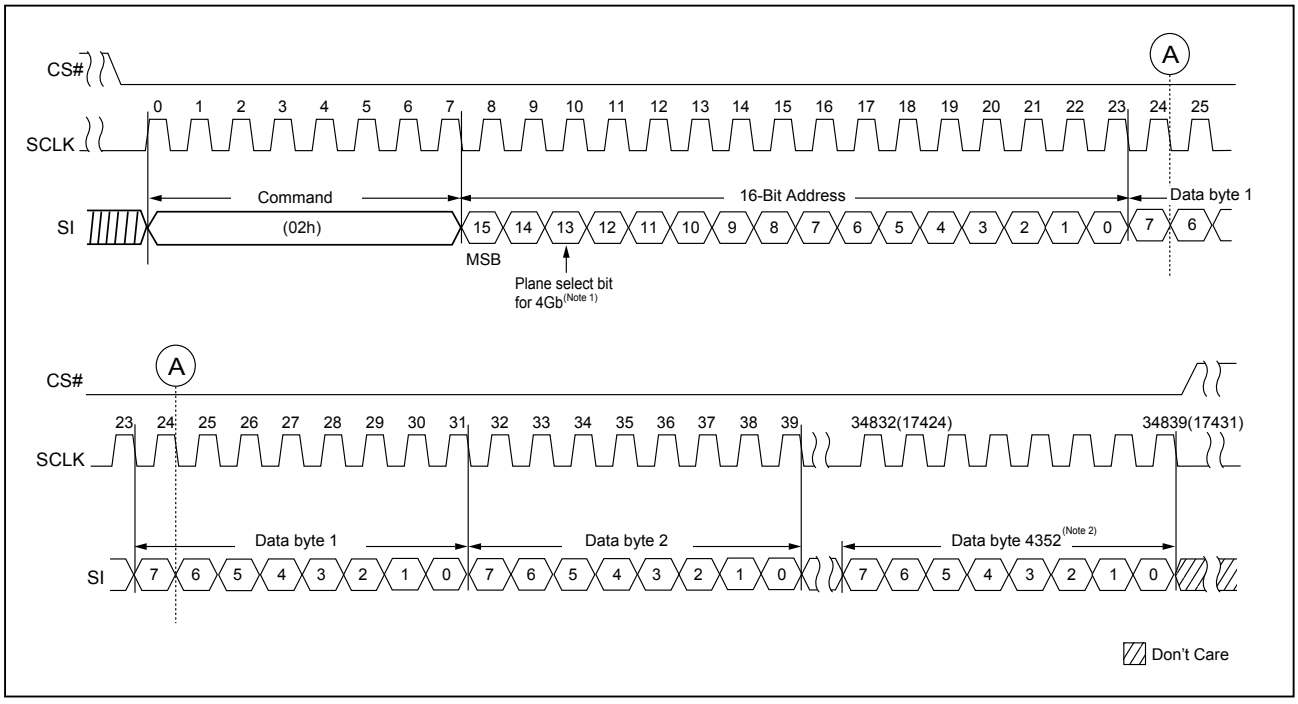
WEL bit is set with the WRITE ENABLE (06h) issued. The program operation will be ignored if 06h command not issued. In a single page, four partial page programs are allowed. Exceeded bytes (Page address is larger than 2176 (for 1G/2G) or 4352 (for 4G) for "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA", the exceeding bytes will be ignored. When CS goes high, the "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA" operation" terminates. Please note the figure below for PROGRAM LOAD.

After PROGRAM LOAD is done, the programming of data should be as following steps: issue 10h (PROGRAM EXECUTE) with 1byte command code, 24 bits address → code programming to memory and busy for tPROG → Program complete.

During programming, status to be polled by the status register.

Operation shows in the Figure below.

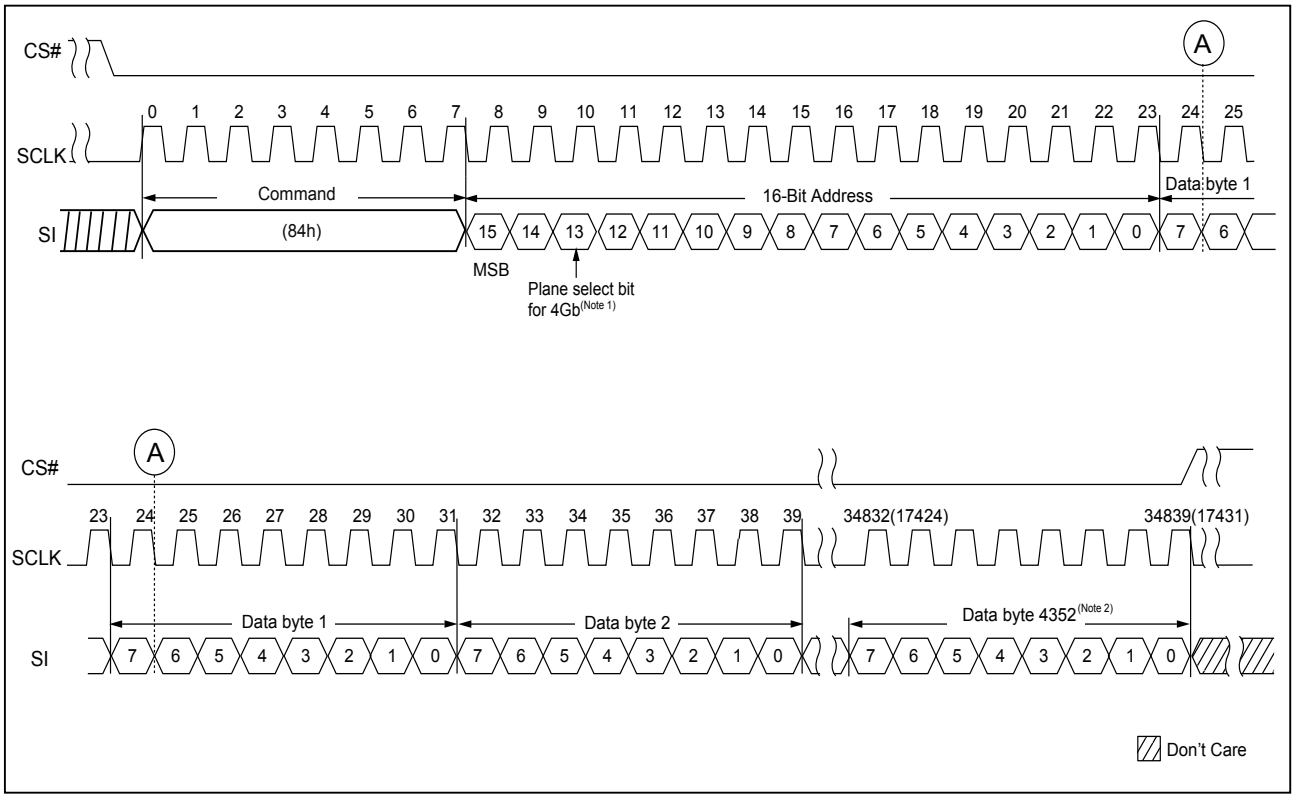
Figure 22. PROGRAM LOAD (02h) Timing



***Note* 1.** *Bit12 is plane select bit for 2Gb.*

***Note* 2.** *Data byte is 2176 for 1Gb/2Gb.*

Figure 23. PROGRAM LOAD RANDOM DATA (84h) Timing



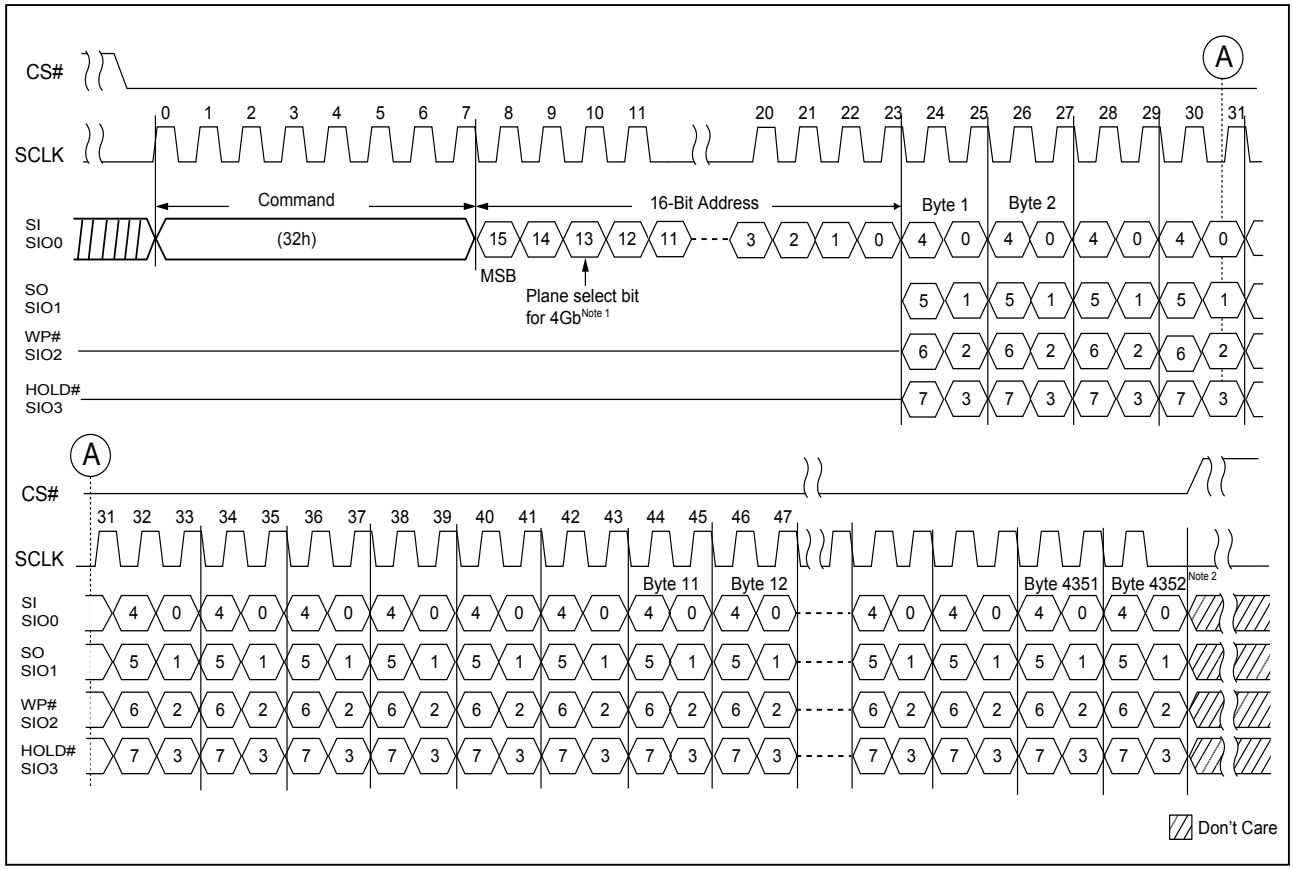
***Note* 1.** *Bit12 is plane select bit for 2Gb.*

***Note* 2.** *Data byte is 2176 for 1Gb/2Gb.*

9-3-2.QUAD IO PAGE PROGRAM

QUAD IO PAGE PROGRAM conducts the 2Kbyte program with 4 I/O mode. The steps are: WRITE ENABLE (06h) → PROGRAM LOAD X4 (32h) → PROGRAM LOAD RANDOM DATA (34h) if needed → PROGRAM EXECUTE (10h) → Poll status by issuing GET FEATURE (0Fh) or RDSR (05h).

Figure 24. PROGRAM LOAD X4 (32h) Timing



***Note* 1.** *Bit12 is plane select bit for 2Gb.*

***Note* 2.** *Data byte is 2176 for 1Gb/2Gb.*

Figure 25. PROGRAM EXECUTE (10h) Timing

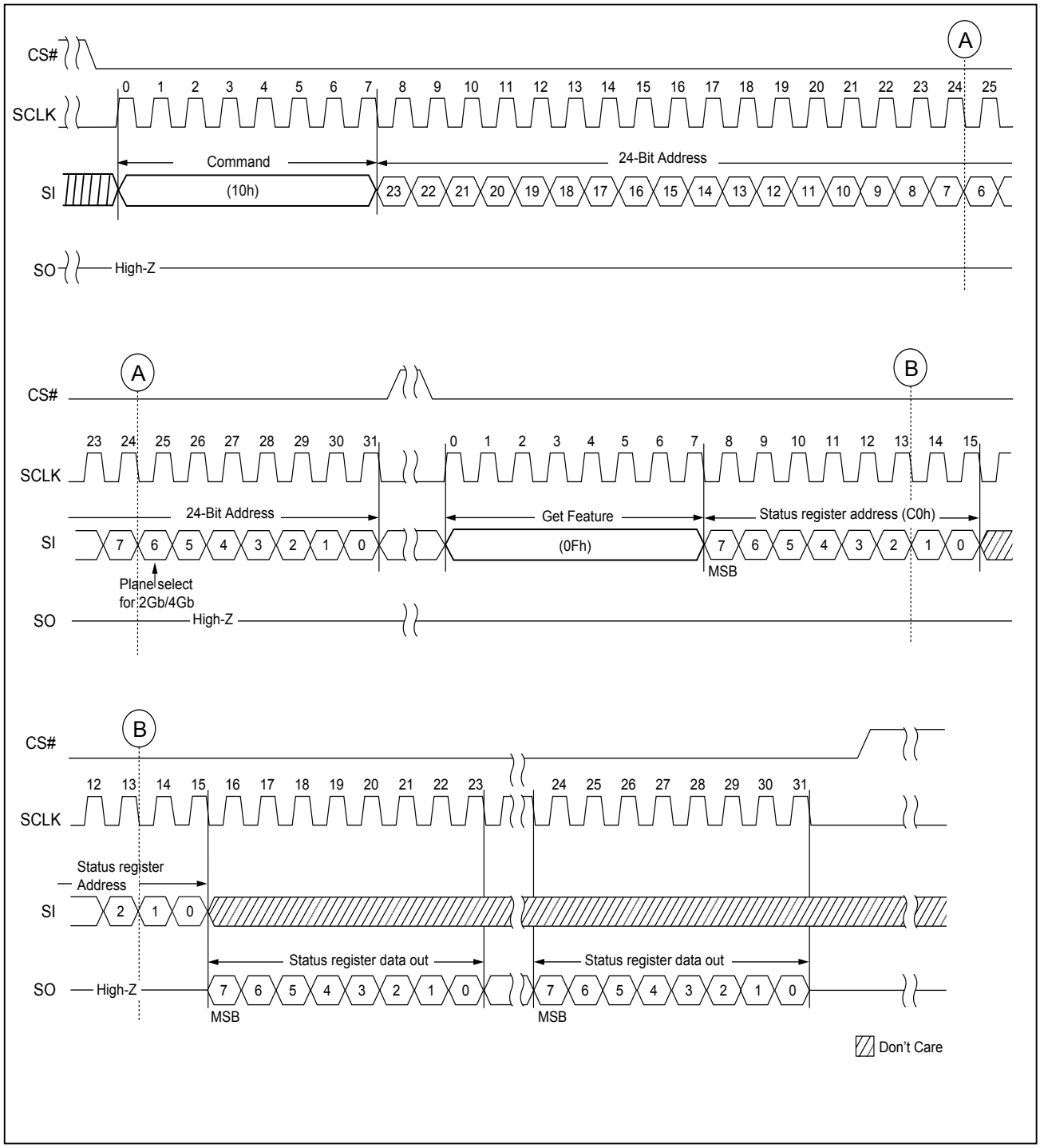
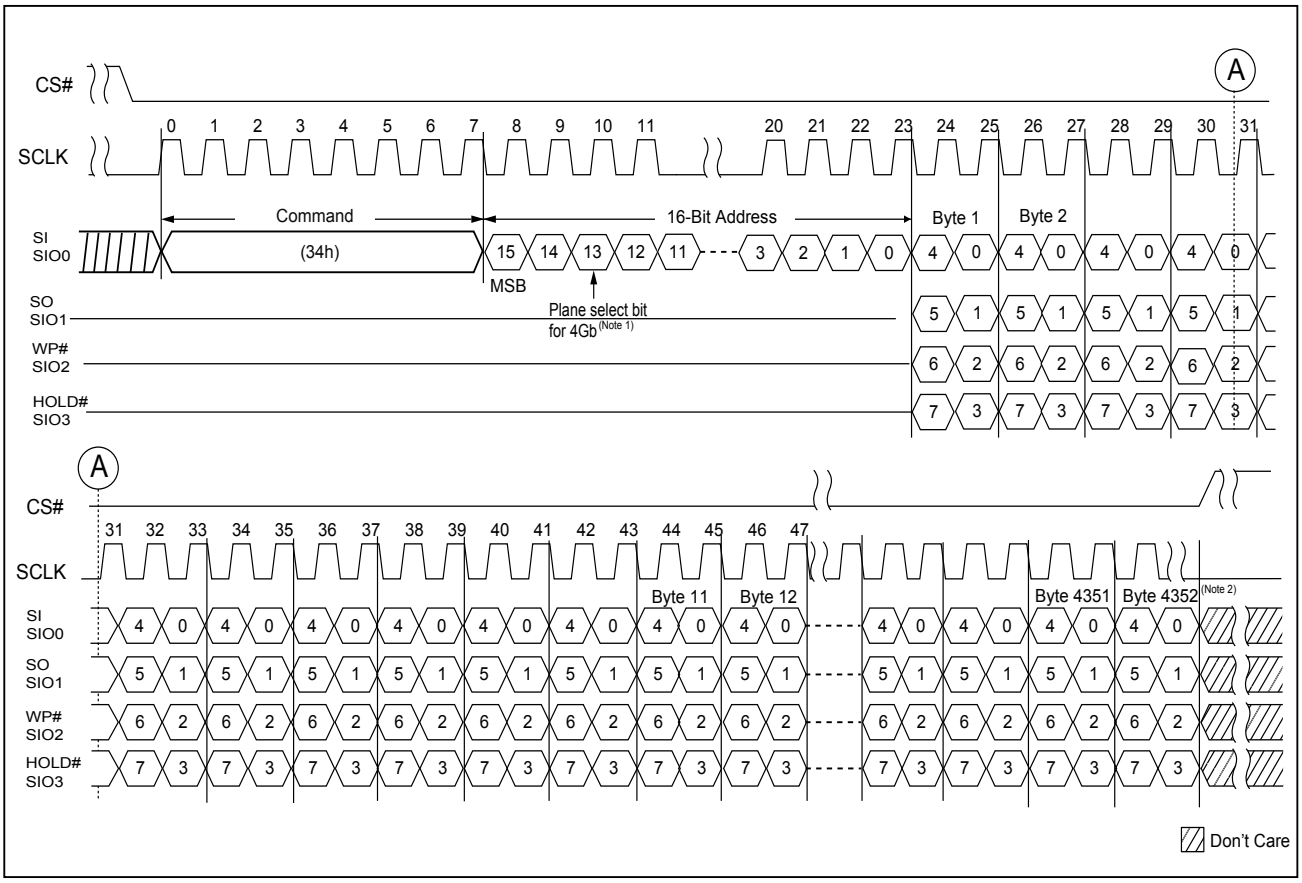


Figure 26. QUAD IO PROGRAM RANDOM INPUT (34h) Timing



***Note* 1.** *Bit12 is plane select bit for 2Gb.*

***Note* 2.** *Data byte is 2176 for 1Gb/2Gb.*

10. BLOCK OPERATIONS

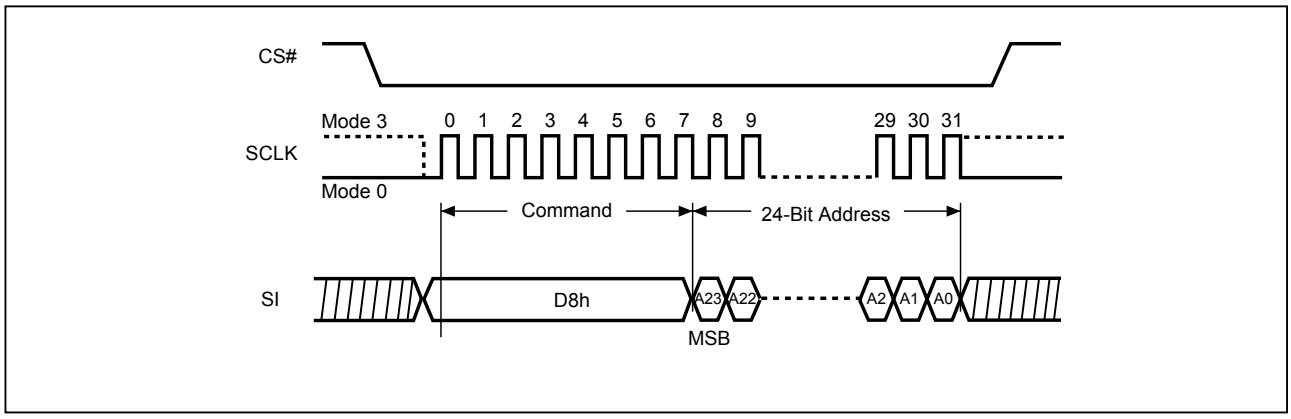
10-1. Block Erase (D8h)

The Block Erase (D8h) instruction is for erasing the data of the chosen block to be "1". The instruction is used for a block of 256K-byte (for 4Gb) or 128K-byte(for 1Gb/2Gb) erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (D8h). Any address of the block is a valid address for Block Erase (D8h) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed. Finally, a Get Feature (0Fh) instruction or RDSR (05h) to check the status is necessary.

The sequence of issuing Block Erase instruction is: CS# goes low→ send Block Erase instruction code→ 24-bit address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Get Feature (0Fh) instruction with Address (C0h) or RDSR (05h) instruction can be used to check the status of the operation during the Block Erase cycle is in progress (please refer to **"Figure 6. GET FEATURE (0Fh) Timing"** and **"Table 4. Feature Settings"**). The OIP bit is "1" during the tBE timing, and is cleared to "0" when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

Figure 27. Block Erase (BE) Sequence



11. Feature Register

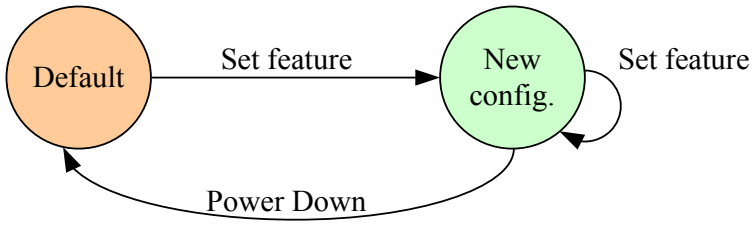
11-1. Configuration Feature Operation

11-1-1. Type: Volatile Register [Symbol: V]

Default value: can not be changed.

Set feature command to change configuration register.

Figure 28. Setting of Volatile Configuration Register

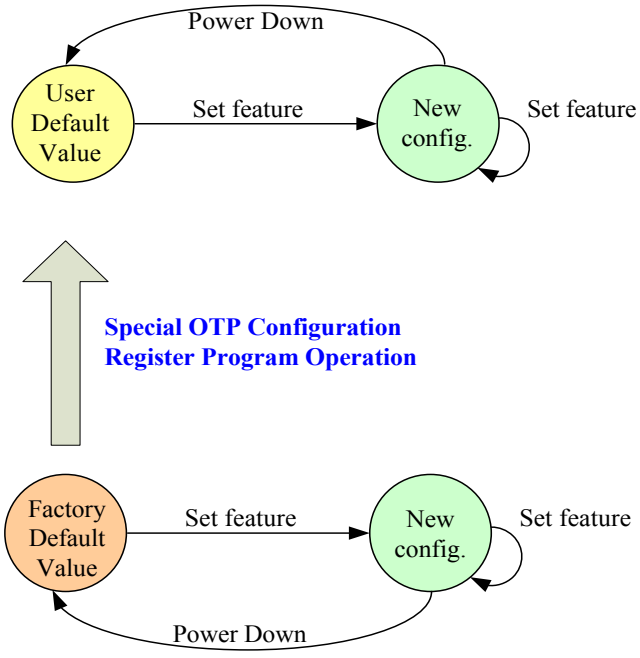


11-1-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2]

Default value: can be changed by special OTP Configuration Register program operation.

Set feature command to change value of configuration register. Those configuration register bits of type V2 are: RANDOPT, RANDEN, DS_IO[1:0] and others (please refer to the **"Table 2. Configuration Registers"**).

Figure 29. Setting of Volatile Configuration Register (Type: V2)

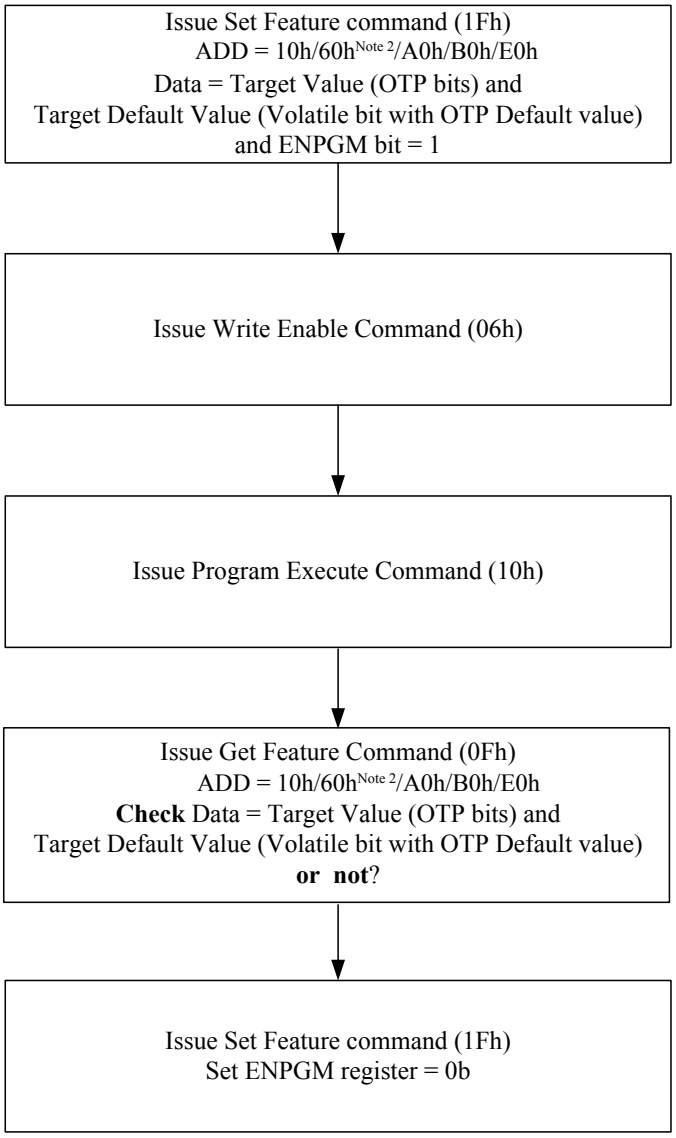


11-1-3. Type: One-time Setting Register [Symbol: OTP]

Configuration register bits of OTP type: SPI_NOR_EN, OTPRWSP bit.

The OTP Configuration Register bits can be only changed from 0 to 1 through Special OTP Configuration Register Program Operation.

Figure 30. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)



Notes:

1. OTP or V2 type Configuration Registers can be programmed together or individually by this programming flow.

2. It is recommended to program OTPRWSP register for V2/OTP type Configuration Register solid protection. The related V2/OTP type Configuration Registers can't be changed anymore, while OTPRWSP=1b.

11-2. OTP "Configuration" Register Solid Protection

To avoid the OTP register bits and OTP Fuse value of V2 type Register bits to be programmed accidentally, this chip provide OTPRWSP (OTP register write solid protection) register to prevent it.

If OTPRWSP register bit is not programmed, the V2/OTP type registers (e.g. RANDOPT, RANDEN, DS_IO[1:0], SPI_NOR_EN) can be programmed; after the OTPRWSP register is programmed, the V2/OTP type registers can not be programmed anymore.

User should program OTPRWSP register even though they do not want to change the V2/OTP register. This can avoid the accidental programming of the V2/OTP register during later usage.

11-3. Block Protection Feature

The Block Protection feature includes three block protection bits (BPx), Block Protection Register Write Disable (BPRWD). Inverse bit (INVERT), complement bit (COMPLEMENTARY) and Solid Protection Bit (SP). These block protection feature bits are volatile bits with its default value can be program once by Special OTP Configuration Register Program Operation.

Soft Protection Mode (SPM)

The SPM uses the BPx bits, INVERT, and COMPLEMENTARY bits to allow part of memory to be protected as read only. The protected area definition is shown as **"Table 11. Definition of Protection Bits"**. The protected areas are more flexible which may protect various area by setting value of BP0-BP2 and Invert bit, and Complementary bit. These are volatile bits and can be modified by set feature command.

After power-up, the chip is in the default state (the factory default state is in protection state), that is, the feature bits BPx is 1, all other bits (BPRWD, INVERT, COMPLEMENTARY and SP) are 0. The Set feature instruction (1Fh) with feature address (A0h) may change the value of the block protection bits and un-protect whole chip or a certain area for further program/erase operation. For example, after the power-on, the whole chip is protected from program/erase operation, the top 1/64 area may be un-protected by using the Set feature instruction (1Fh) with the feature address (A0h) to change the values of BP2 and BP1 from "1" to "0" as **"Table 11. Definition of Protection Bits"** below.

Hardware Protection Mode (HPM) & Solid Protection Mode (SDPM) and Permanent Protection Mode (PPM)

Under the Hardware Protection mode and Solid Protection Mode, the (BPx, INVERT, COMPLEMENTART) bits can not be changed.

Hardware Protection Mode: The device enters HPM if BPRWD bits is set to 1 and WP#/SIO2 is driven to 0.

Note 1: *HPM also requires SP bit to be 0 state .*

Note 2: *The Quad mode is not supported in HPM.*

Solid Protection Mode: If SP bit is set to 1, the device enters SDPM. After that, the selected block is solid protected and can not be un-protected until next power cycle.

Permanent Protection Mode (PPM): If the default value of the SP bit is programmed to 1, the device enters PPM. After that, the selected block is permanently protected and can not be un-protected anymore.

Table 11. Definition of Protection Bits

BP2	BP1	BP0	Invert	Complementary	Protection Area
0	0	0	x	x	all unlocked
0	0	1	0	0	upper 1/64 locked
0	1	0	0	0	upper 1/32 locked
0	1	1	0	0	upper 1/16 locked
1	0	0	0	0	upper 1/8 locked
1	0	1	0	0	upper 1/4 locked
1	1	0	0	0	upper 1/2 locked
1	1	1	x	x	all locked (default)
0	0	1	1	0	lower 1/64 locked
0	1	0	1	0	lower 1/32 locked
0	1	1	1	0	lower 1/16 locked
1	0	0	1	0	lower 1/8 locked
1	0	1	1	0	lower 1/4 locked
1	1	0	1	0	lower 1/2 locked
0	0	1	0	1	lower 63/64 locked
0	1	0	0	1	lower 31/32 locked
0	1	1	0	1	lower 15/16 locked
1	0	0	0	1	lower 7/8 locked
1	0	1	0	1	lower 3/4 locked
1	1	0	0	1	block 0
0	0	1	1	1	upper 63/64 locked
0	1	0	1	1	upper 31/32 locked
0	1	1	1	1	upper 15/16 locked
1	0	0	1	1	upper 7/8 locked
1	0	1	1	1	upper 3/4 locked
1	1	0	1	1	block0

Note: *Block #0 is at lower portion.*

11-4. Secure OTP (One-Time-Programmable) Feature

There is an Secure OTP area which has 30 full pages (30 x 2176-byte for 1Gb/2Gb or 30 x 4352-byte for 4Gb) from page 02h to page 1Fh guarantee to be good for system device serial number storage or other fixed code storage. The Secure OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows partial page program to be “0”, once the Secure OTP protection mode is set, the Secure OTP area becomes read-only and cannot be programmed again. The OTP area is scrambled if randomizer function is enabled.

The Secure OTP operation is operated by the Set Feature instruction with feature address (B0h) to access the Secure OTP operation mode and Secure OTP protection mode.

To check the NAND device is ready or busy in the Secure OTP operation mode, the status register bit 0 (OIP bit) may report the status by Get Feature command operation.

To exit the Secure OTP operation or protect mode, it can be done by writing "0" to both Bit7 (Secure OTP protect bit) and bit6 (Secure OTP enable bit) for returning to the normal operation.

Secure OTP Read

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing normal Page Read command (13h)

Secure OTP Program (if the "Secure OTP Protection Bit" is "0") for

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing Page Program command (02h)
4. Issuing program execute command (10h)

Secure OTP Protection

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set both the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" as "1".
3. Issuing program execute command (10h)

Table 12. Secure OTP States

Secure OTP Protection Bit(Note1)	Secure OTP Enabled Bit	State
0	0	Normal operation
0	1	Access the Secure OTP for reading or programming
1	0	Not applicable
1	1	Secure OTP Protection by using the Program Execution command (10h)Note2

Note 1. *OTP protection bit is volatile.*

Note 2. *Once the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" are set as "1", the secure OTP becomes read only.*

11-5. Status Register

11-5-1. Get Feature command (0Fh)

The MX35UFxG24AD provides a status register that outputs the device status by writing a Get Feature command (0Fh) with the feature address (C0h), and then the IO pins output the status.

The Get Feature (0Fh) command with the feature address(C0h) will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in the table below.

11-5-2. Read Status command (RDSR)

In additional to read the chip status by Get Feature command, this device also supports the SPI NOR Read Status command (05h). The Read Status command can be issued any time (even during read/program/ erase operation), it is recommended to check the Operation in Program (OIP) bit or Cache Read Busy (CRBSY) before sending a new instruction when a read, program or erase operation is in progress.

The sequence of issuing RDSR instruction is CS# goes low→ send RDSR instruction code →Status register data out on SO.

Figure 31. Read Status Register (RDSR)

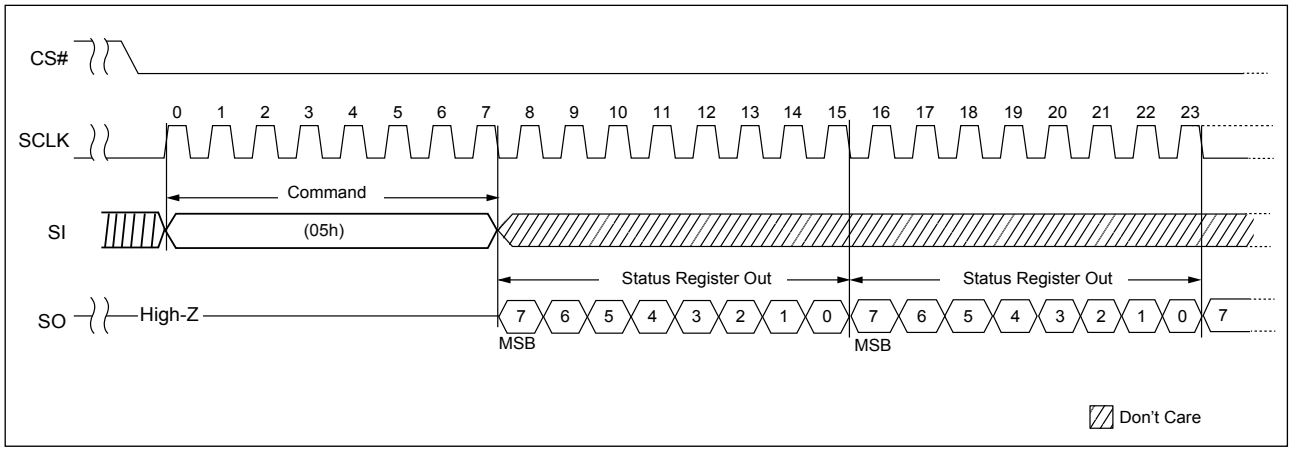


Table 13. Status Register Bit Descriptions

SR Bit	Bit Name	Description
SR[0] (OIP)	Operation in progress	The bit value indicates whether the device is busy in operations of read/ program execute/ erase/ reset command. 1: Busy, 0: Ready
SR[1] (WEL)	Write enable latch	The bit value indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, and then the device can accept program/ erase/write status register instruction. 1: write enable, 0: not write enable. The bit value will be cleared (as "0") by issuing Write Disable command(04h) or after the program/erase operation completion.
SR[2] (ERS_Fail)	Erase fail	The bit value shows the status of erase failure or if host erase any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed. The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation.
SR[3] (PGM_Fail)	Program fail	The bit value shows the status of program failure or if host program any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed. The bit value will be cleared (as "0") by RESET command or during the program execute command operation.
SR[6:4]	Reserved	
SR[7] (CRBSY)	Cache Status Bit	The bit value indicates whether the internal cache is busy in Page Read Cache Operations. 1: Busy- internal cache is busy on data transfer 0: Ready- device is ready for cache data out

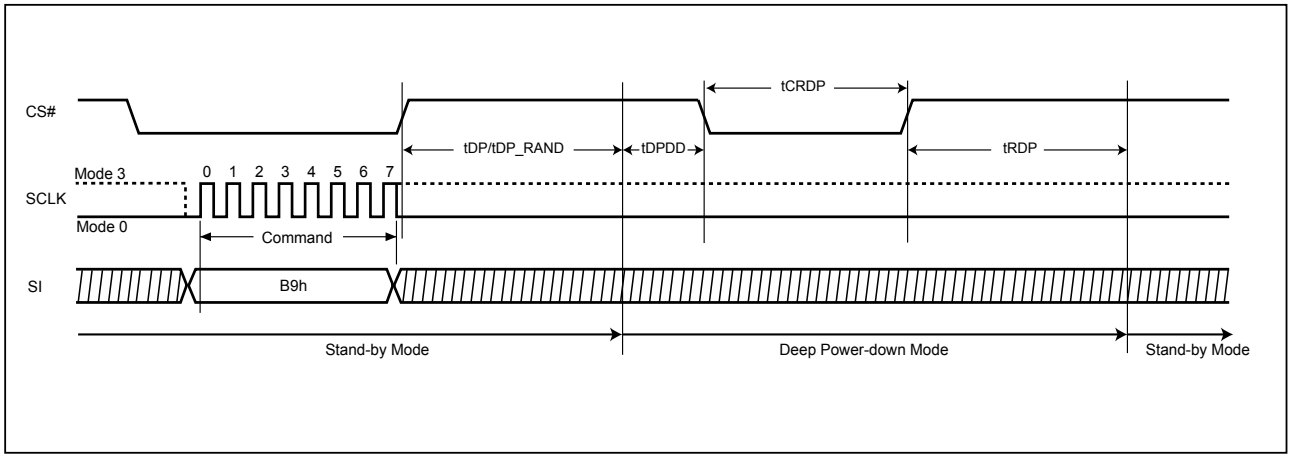
12. Deep Power-down Mode

The Deep Power-down mode places the device into a minimum power consumption state, in which the quiescent current is reduced from ISB1 to ISB2.

The Deep Power-down command (B9h) may enter the deep power down mode of NAND device. The CS# pin should keep high during the deep power-down period. The chip will exit the Deep Power-down Mode with simply CS# toggling. The following waveform shows the timing waveform for Deep Power-down operation.

To recover from the Deep Power-down mode, a recovery time tRDP is required. The detailed specification is shown as **"Table 21. General Timing Characteristics"**.

Figure 32. Deep Power-down (DP) Sequence and Release from Deep Power-down Sequence

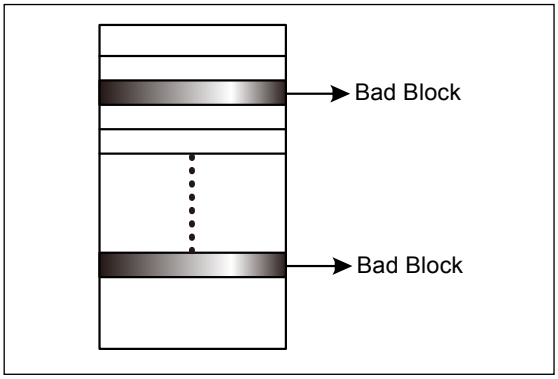


13. SOFTWARE ALGORITHM

13-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is necessary to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since the bad block marks may be cleared by any erase operation.

Figure 33. Bad Blocks



While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **"Figure 34. Bad Block Test Flow"** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

Table 14. Valid Blocks

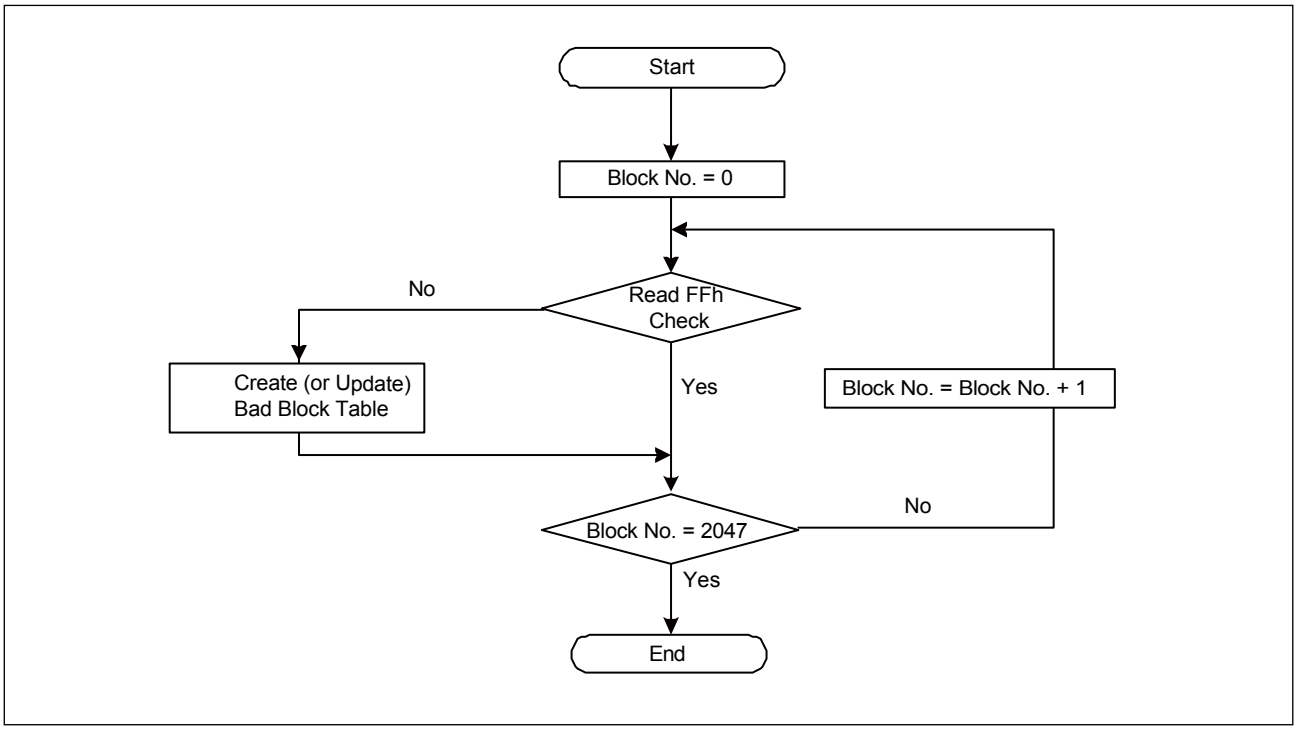
	Density	Min.	Typ.	Max.	Unit	Remark
Valid (Good) Block Number	1Gb	1004		1024	Block	Block 0-7 is guaranteed to be good at the time of shipment (with ECC implementation by host)
	2Gb	2008		2048	Block	Block#0-7 are guaranteed to be good at the time of shipment (with ECC implementation by host)
	4Gb	2008		2048	Block	Block#0-7 are guaranteed to be good at the time of shipment (with ECC implementation by host)

Note: *The total good block numbers will not be less than minimum good block numbers during the NAND device lifetime.*

13-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **"Figure 34. Bad Block Test Flow"** shows the recommended flow for creating a bad block table.

Figure 34. Bad Block Test Flow



13-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

Table 15. Failure Modes

Failure Mode	Detection and Countermeasure	Sequence
Erase Failure	Status Read after Erase	Block Replacement
Programming Failure	Status Read after Program	Block Replacement
Read Failure	Read Failure	ECC

14. DEVICE POWER-UP

14-1. Power-up

After the Chip reaches the power on level, the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. The device can be fully accessible when VCC reaches the power-on level and wait 5ms.

During the power on and power off sequence, it is necessary to keep the WP# = Low for internal data protection.

Figure 35. Power Up/Down and Voltage Drop

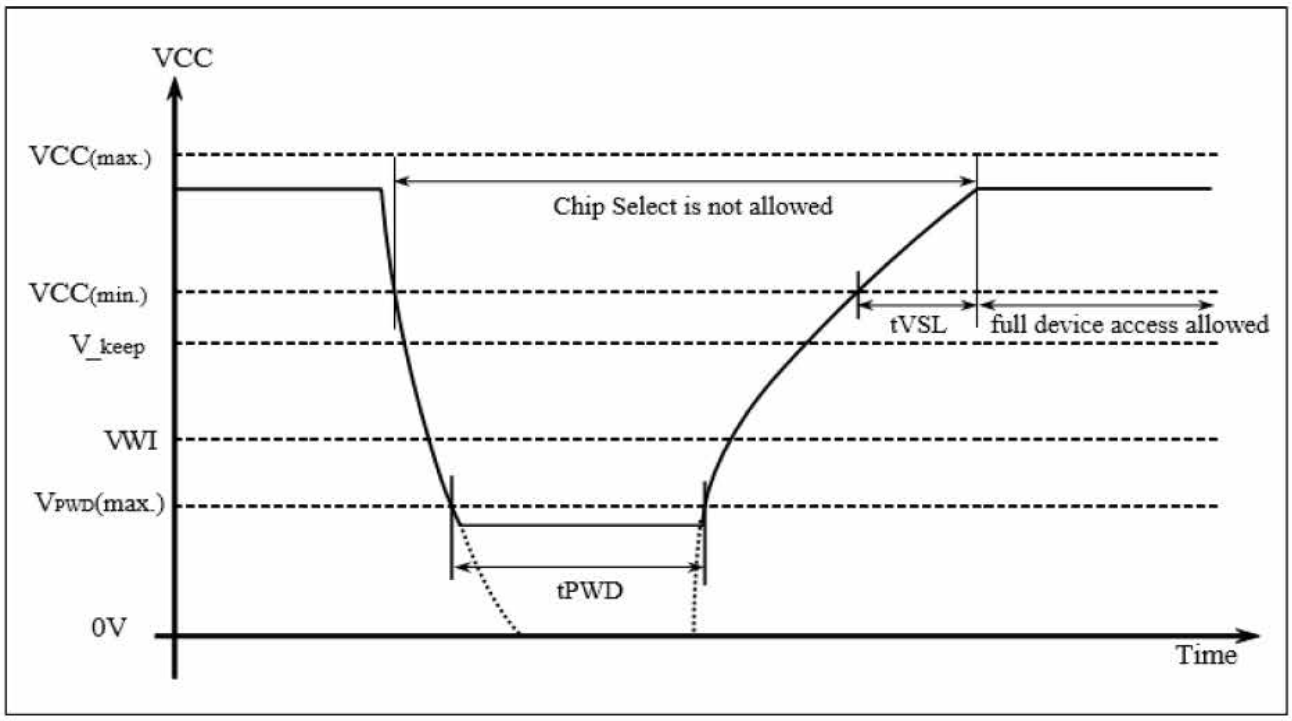


Table 16. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needs to be below V_{PWD} for proper initialization to occur		0.8	V
$V_{_keep}$	Voltage threshold where re-initialization is necessary if VDD drop below to $V_{_KEEP}$	1.5		V
tPWD	The minimum duration to ensure initialization occurs	300		us
tVSL	VCC(min.) to device operation	5000		us
VCC	VCC Power Supply	1.7	1.95	V
VWI	Write Inhibit Voltage	1.0	1.5	V

Note: *These parameters are characterized only.*

15. PARAMETERS

15-1. ABSOLUTE MAXIMUM RATINGS

Temperature under Bias	-50°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages with respect to ground (Note 2)	-0.6V to 2.4V
VCC supply voltage with respect to ground (Note 2)	-0.6V to 2.4V
ESD protection	>2000V

Notes:

1. The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.

2. Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.

3. During voltage transitions, all pins may overshoot to VCC +1.0V or -1.0V for period up to 20ns. Please refer to the two waveforms as below.

Figure 36. Maximum Negative Overshoot Waveform

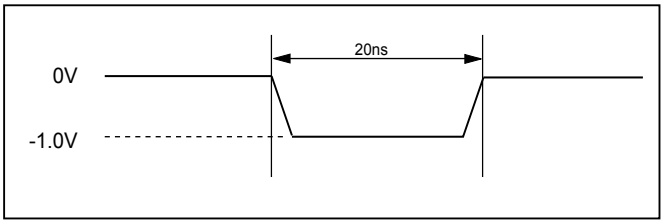
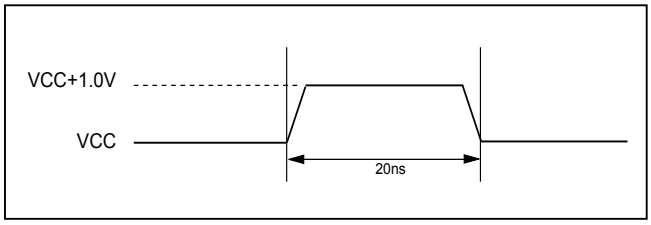


Figure 37. Maximum Positive Overshoot Waveform



15-2. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input current with respect to GND on all non-power pins	-100mA	+100mA
Test conditions are compliant to JEDEC JESD78 standard		

Table 17. AC Testing Conditions

Testing Conditions	Value	Unit
Input pulse level	0 to VCC	V
Output load capacitance	1TTL+CL(30)	pF
Input rising & falling time	1.5	ns
Input timing measurement reference levels	VCC/2	V
Output timing measurement reference levels	VCC/2	V

Table 18. Capacitance

TA = +25°C, F = 1 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
CIN	Input capacitance			10	pF	VIN = 0V
COUT	Output capacitance			10	pF	VOUT = 0V

Table 19. Operating Range

Temperature	VCC	Tolerance
-40°C to + 85°C	+1.8V	1.7 - 1.95V

Figure 38. SCLK TIMING DEFINITION

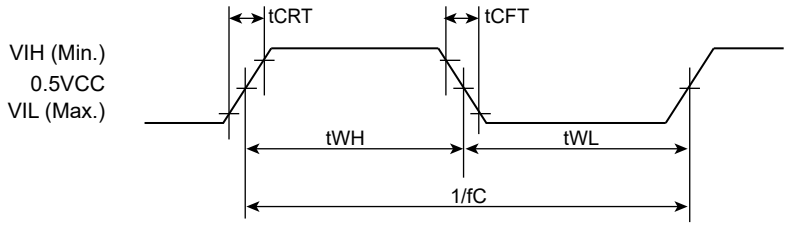


Table 20. DC Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Test Conditions
ILI	Input leakage current			+/- 10	uA	VIN= 0 to VCC Max.
ILO	Output leakage current			+/- 10	uA	VOUT= 0 to VCC Max.
ISB1	VCC standby current (CMOS)		10	50	uA	VIN=VCC or GND, CS#=VCC
ISB2	VCC deep power down current (CMOS)		1	15	uA	VIN=VCC or GND, CS#=VCC
ICC1	VCC active current (Sequential Read)		TBD	30	mA	f= max. fC, Iout = 0mA
ICC2	VCC active current (Program)		TBD	30	mA	
ICC3	VCC active current (Erase)		TBD	30	mA	
VIL	Input low level	-0.3		0.2VCC	V	
VIH	Input high level	0.8VCC		VCC + 0.3	V	
VOL	Outout low voltage			0.2	V	IOL= -1mA
VOH	Outout high voltage	VCC-0.2V			V	IOH= -20uA

Table 21. General Timing Characteristics

Symbol	Parameter		Note	fC=133MHz		fC=166MHz		Unit
				Min.	Max.	Min.	Max.	
fC	Serial Clock Frequency for all command		1	D.C.	133	D.C.	166	MHz
tCHHH	HOLD# Hold Time (relative to SCLK)			3.375	-	2.7	-	ns
tCHHL	HOLD Hold Time (relative to SCLK)			3.375	-	2.7	-	ns
tCS	CS# Diselect Time			30	-	30	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)			3.375	-	3	-	ns
tSLCH	CS# Active Setup Time (relative to SCLK)			3.375	-	3	-	ns
tSHCH	CS# Not Active Setup Time (relative to SCLK)			3.375	-	3	-	ns
tCHSL	CS# Not Active Hold Time (relative to SCLK)			3.375	-	3	-	ns
tDIS	Output Disable Time			-	6	-	6	ns
tHC	HOLD Setup Time (relative to SCLK)			3.375	-	2.7	-	ns
tHD	HOLD# Setup Time (relative to SCLK)			3.375	-	2.7	-	ns
tHDDAT	Data Input Hold Time			2	-	2	-	ns
tHO	Data Output Hold time			1		1		ns
tHZ	HOLD# to Output High-Z			-	12	-	12	ns
tLZ	HOLD# to Output Low-Z			-	7	-	7	ns
tSUDAT	Data In Setup Time			2	-	2	-	ns
tV	Serial Clock Low to Output Valid	30pF		-	6	-	6	ns
		10pF		-	5	-	5	ns
tWH	Serial Clock High Time			0.45 x 1/fC	-	0.45 x 1/fC	-	ns
tWL	Serial Clock Low Time			0.45 x 1/fC	-	0.45 x 1/fC	-	ns
tCRT	Clock Rise Time (peak to peak)			0.5	-	0.5	-	V/ns
tCFT	Clock Fall Time (peak to peak)			0.5	-	0.5	-	V/ns
tWPH	Write protect Hold Time			100	-	100	-	ns
tWPS	Write protect Setup Time			20	-	20	-	ns
tVSL	VCC(min.) to device operation			5	-	5	-	ms
tRST	Device reset time (Idle/ Read/ Program/ Erase)		2		5/5/10/500		5/5/10/500	us
tDP	CS# high to deep power-down mode (Idle/Read/ Program/Erase)			-	1/25/700 /5000	-	1/25/700 /5000	us
tDP_RAND	CS# high to deep power-down mode with randomizer enable (Idle/Read/Program/Erase)			-	1/25/740/5000	-	1/25/740/5000	us
tDPDD	Delay time for release from deep power-down mode once entering deep power down mode			100	-	100	-	us
tCRDP	CS# toggling time before release from deep power-down mode to enter Standby Mode			20	-	20	-	ns
tRDP	Recovery time for release from deep power-down mode			35	-	35	-	us

Notes:

1*: Max. clock rate=108MHz for BBh/EBh command with 4-dummy cycle, and max. clock rate=166MHz with 8-dummy cycle, and 20MHz for 03h command. Before running above 108MHz on (1-2-2, 1-4-4), please set the DC bit as "1" for 8-dummy cycle option.*

2: *the tRST is 5ms for the first RESET command after Power-on.*

Table 22. Program/ Read/ Erase Characteristics

Symbol	Parameter	Note	Typical	Max.	Unit
tRD	The data transfering from array to buffer			25	us
tPROG	Page programming time (Randomizer disabled)		320	700	us
tPROG_RAND	Page programming time (Randomizer enabled)		360	740	us
tRCBSY (Read)	Dummy busy time for cache read		4.5	25	us
tERASE	Block Erase Time		4	6	ms
NOP[Note]	Number of partial program cycles in same page			4	times

Note: *NOP=1 for the randomizer covered data area when the randomizer is enabled.*

Figure 39. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1

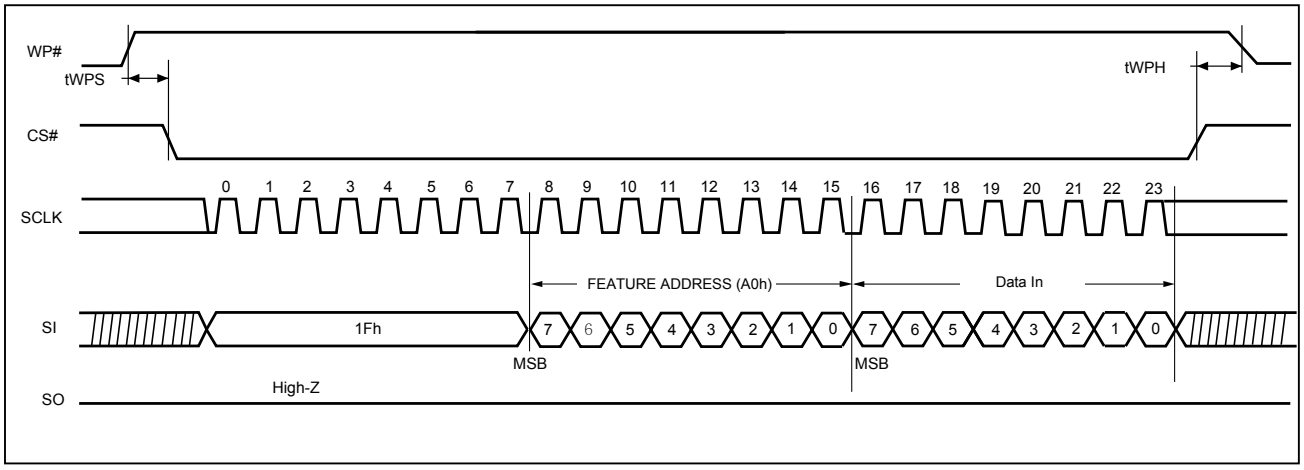


Figure 40. Serial Input Timing

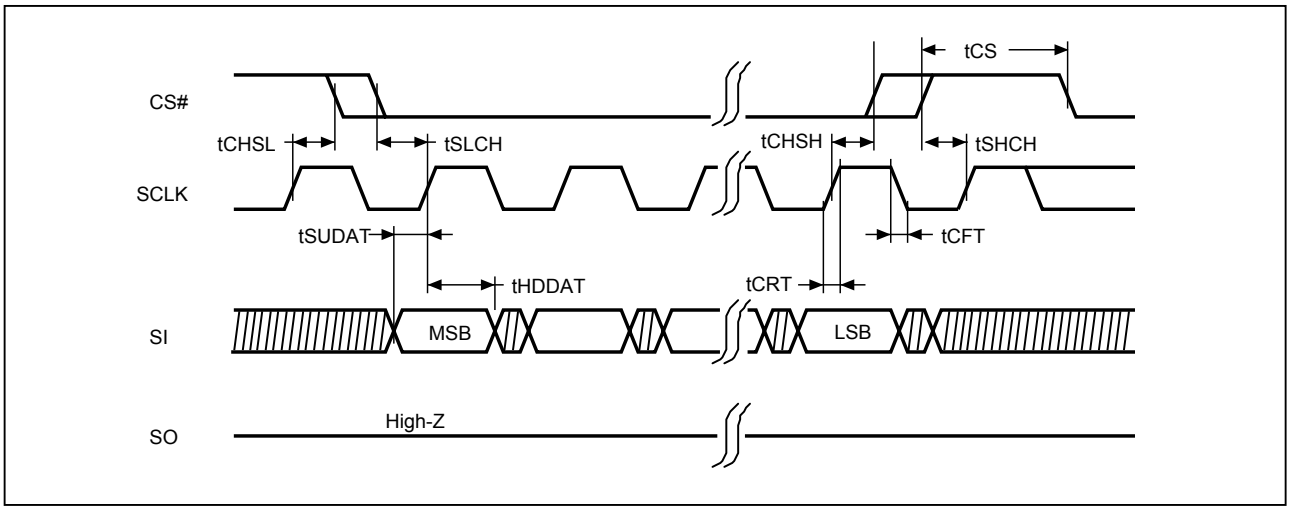


Figure 41. Serial Output Timing

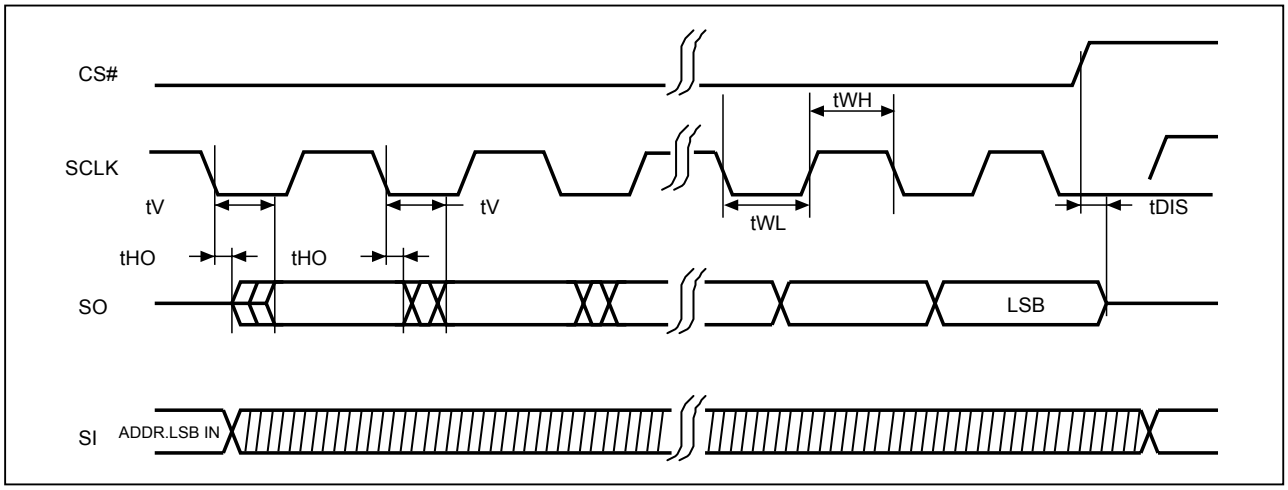
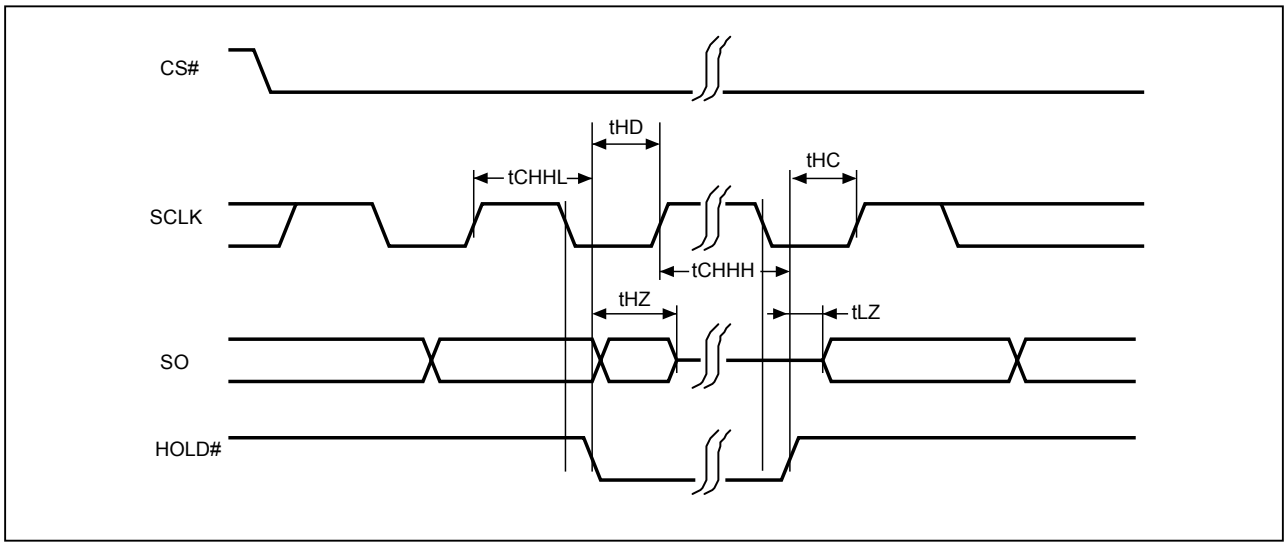


Figure 42. Hold Timing

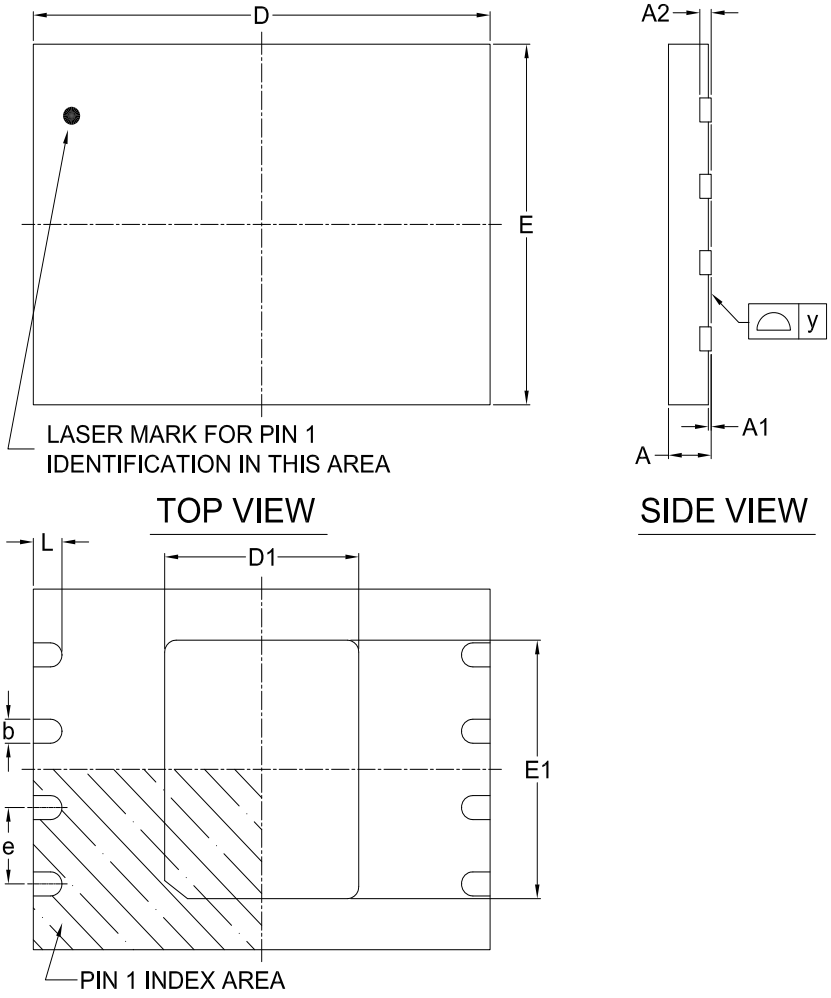


Note: *SI is "don't care" during HOLD operation.*

16. PACKAGE INFORMATION

16-1. 8-WSON (8x6x0.8mm)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	3.35	5.90	4.25	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	3.40	6.00	4.30	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	3.45	6.10	4.35	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.132	0.232	0.167	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.134	0.236	0.169	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.136	0.240	0.171	0.022	---	0.002

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