MX30LF1G08AA

1G-bit NAND Flash Memory

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1G-bit (128 M x 8 bit) NAND Flash Memory

1. FEATURES

- **1 Gbit SLC NAND Flash**
  - 128 M x 8 bit
  - 64 K pages of (2,048+64) bytes each
  - 1K blocks of 64 pages each
- **Multiplexed Command/Address/Data**
- **4 MByte User Redundancy**
  - 64 bytes attached to each page
- **Fast Read Access**
  - First-byte latency: 25us
  - Sequential read: 30ns/byte
- **Cache Read Support**
- **Page Program Operation**
- **Cache Program**
  - Internal cache of (2,048+64) bytes
- **Program Time:** Page program 250us (typ.)
- **Single Voltage Operation:** 3.3V
- **Low Power Dissipation** - Max. 30mA active current (RD/PGM/ERS)
- **Automatic Sleep Mode**
  - 50uA (Max) standby current
- **Block Erase Architecture**
  - Block size: (128K+4K) bytes per block
  - 1K blocks, 64 pages each
  - Block Erase Time: 2ms (Typ.)
- **Hardware Data Protection:** WP# pin
- **Multiple Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Status Register**
- **Electronic Signature (Four Cycles)**
- **High Reliability**
  - Endurance: 100K cycles (with 1-bit ECC per 528-byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range:**
  -40°C to +85°C
- **Package:**
  - 48-TSOP(I) (12mm x 20mm),
  - 63-ball 9mmx11mm VFBGA
  - All packaged devices are RoHS Compliant & Halogen-free.

2. GENERAL DESCRIPTIONS

The MX30LF1G08AA is a 1Gb SLC NAND Flash memory device. Its standard NAND Flash features and reliable quality make it most suitable for embedded system code and data storage usage.

The MX30LF1G08AA is typically accessed in pages of 2,112 bytes, both for read and for program operations.

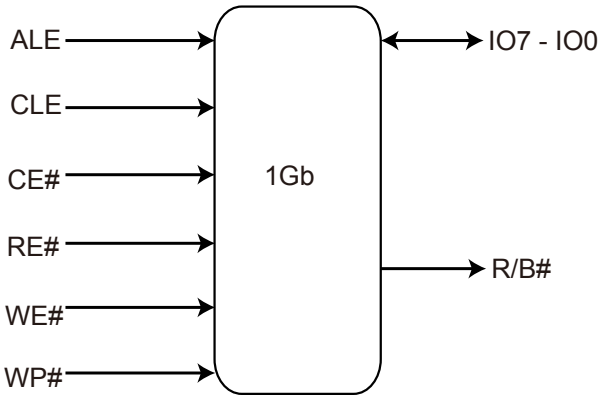
The MX30LF1G08AA array is organized as 1024 blocks, which is composed by 64 pages of (2,048+64) byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for ECC and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access.

The Cache Read Operation of the MX30LF1G08AA enable first-byte read-access latency of 25us and sequential read of 30ns per byte.

Fast programming is supported, enabling page programming at a rate of 8MB/sec (approx.)

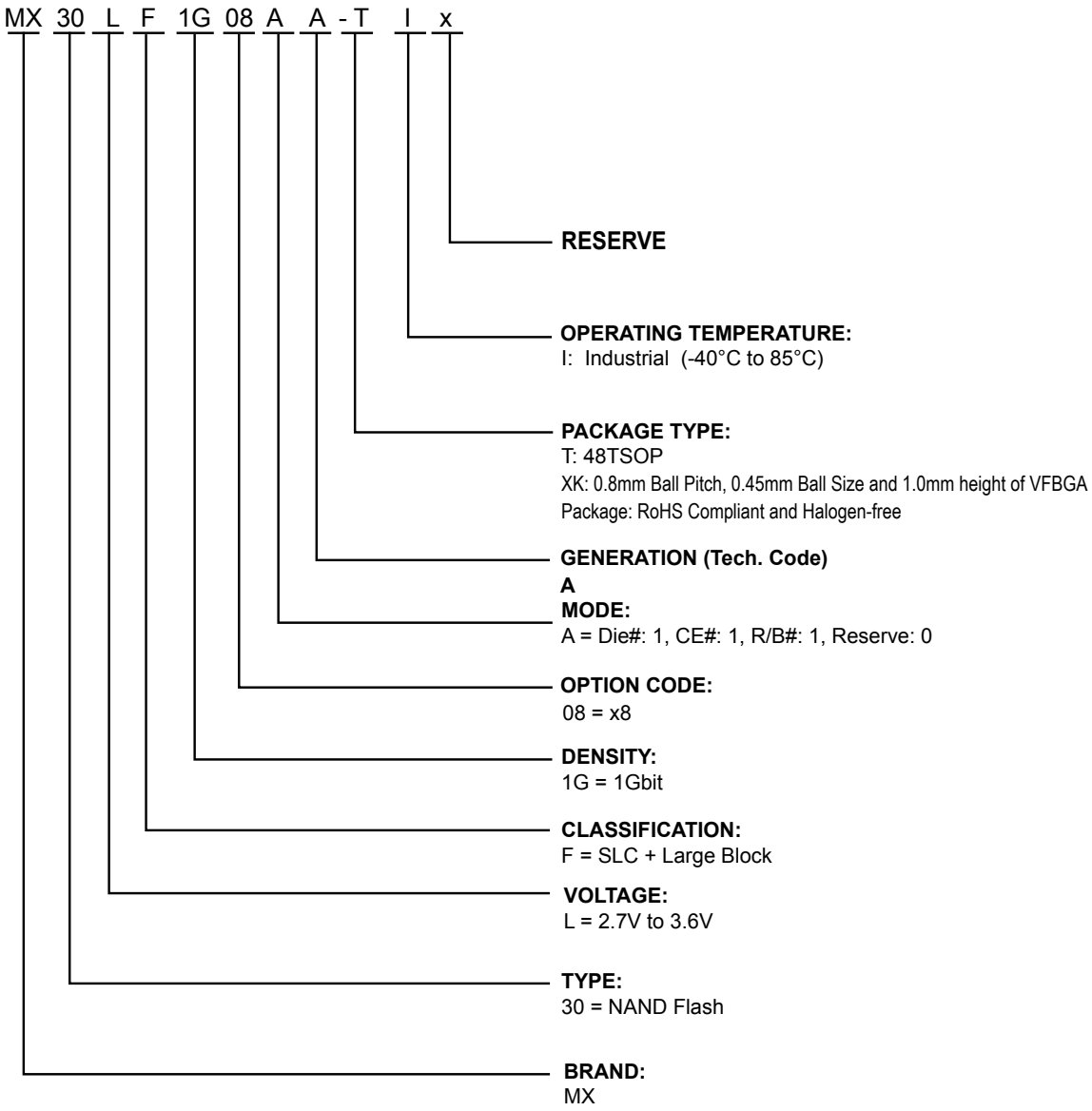
The MX30LF1G08AA power consumption is 30 mA during all modes of operations (Read/ Program/Erase), and 50uA in standby mode.

Figure 1. MX30LF1G08AA Logic Diagram



2-1. ORDERING INFORMATION

Part Name Description



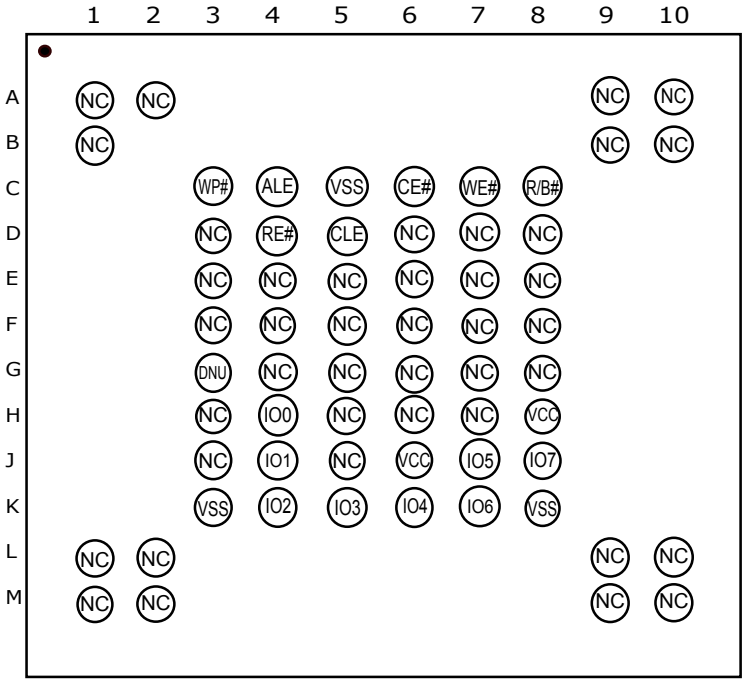
PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE	TEMPERATUR GRADE
MX30LF1G08AA-TI	x8	2.7V - 3.6 Volt	48-TSOP	Industrial (-40° to 85°C)
MX30LF1G08AA-XKI	x8	2.7V - 3.6 Volt	63-VFBGA	Industrial (-40° to 85°C)

3. PIN CONFIGURATIONS

48-TSOP



63-ball 9mmx11mm VFBGA



3-1. PIN DESCRIPTIONS

SYMBOL	PIN NAME
IO7 - IO0	Data I/O port
CE#	Chip Enable (Active Low)
RE#	Read Enable (Active Low)
WE#	Write Enable (Active Low)
CLE	Command Latch Enable
ALE	Address Latch Enable
WP#	Write Protect (Active Low)
R/B#	Ready/Busy (Open Drain)
VSS	Ground
VCC	Power Supply for Device Operation
NC	Not Connected Internally
DNU	Do Not Use (Do Not Connect)

4. PIN FUNCTIONS

The MX30LF1G08AA device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

I/O PORT: IO7 - IO0

The IO7 to IO0 pins are for address/command input and data output to and from the device.

CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes High during a Read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. when the ALE goes high, the address is latched at the rising edge of WE#.

WRITE PROTECT: WP#

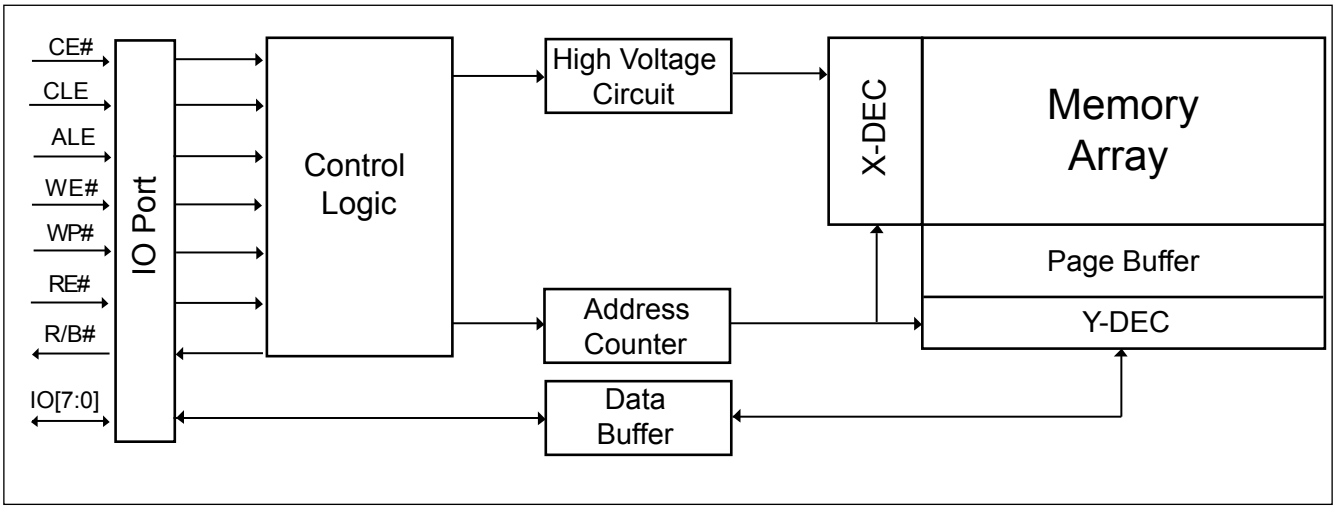
The WP# signal keeps low and then the memory will not accept the program/erase operation. The WP# pin is not latched by WE# for ensuring of the data can be protected during power-on. It is recommended to keep WP# pin low during power on/off sequence. Please refer to the waveform of "Power On/Off Sequence".

READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

Please refer to **Section 9.1** for details.

5. BLOCK DIAGRAM



6. DEVICE OPERATIONS

ADDRESS INPUT / COMMAND INPUT / DATA INPUT

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

Figure 2. AC Waveform for Command / Address / Data Latch Timing

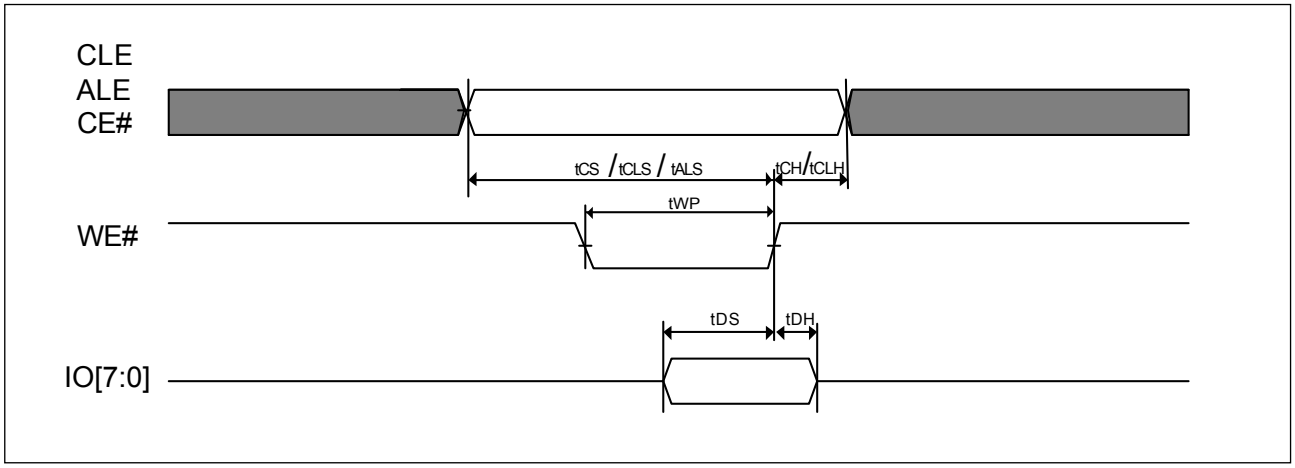


Figure 3. AC Waveforms for Address Input Cycle

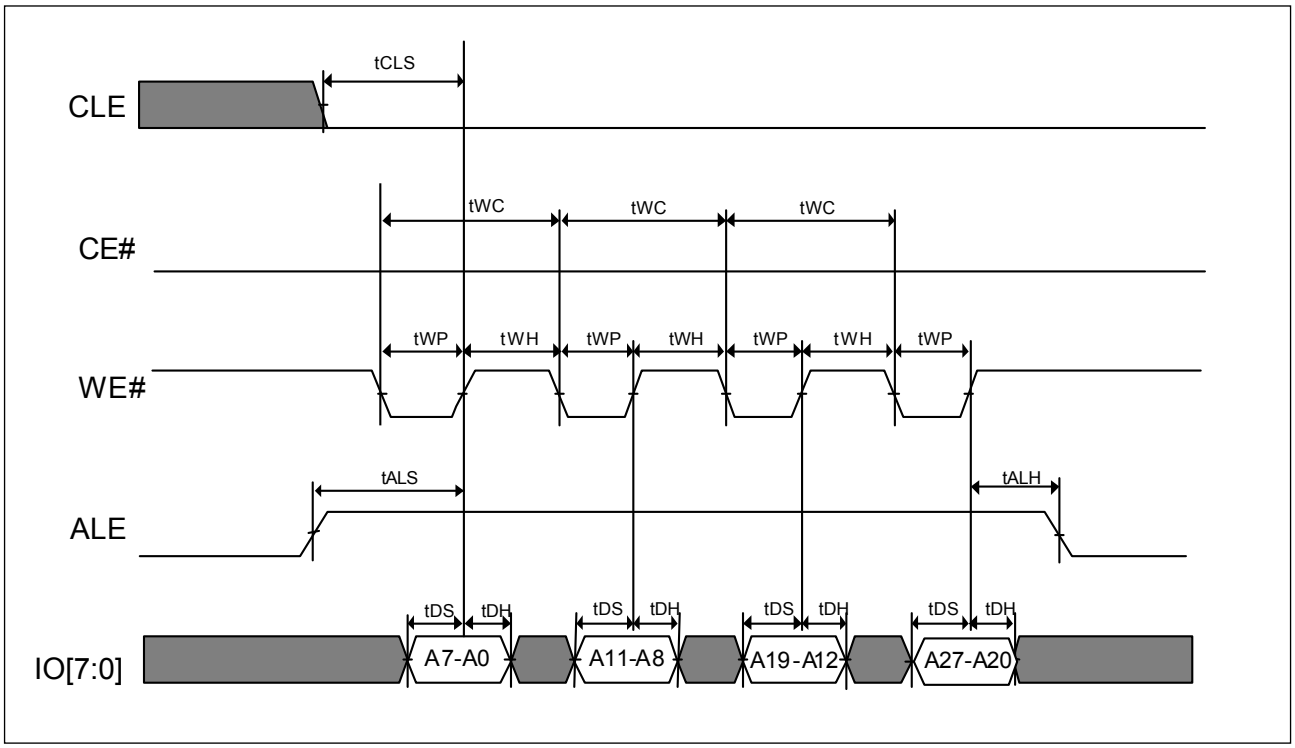


Figure 4. AC Waveforms for Command Input Cycle

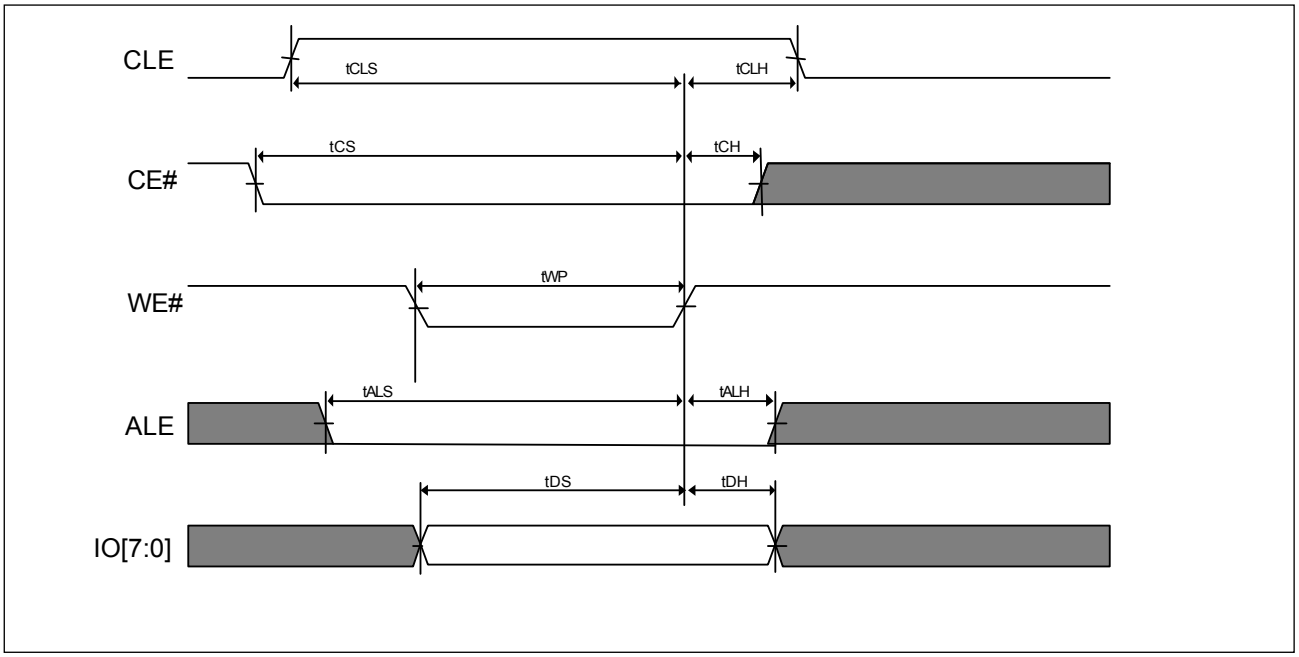
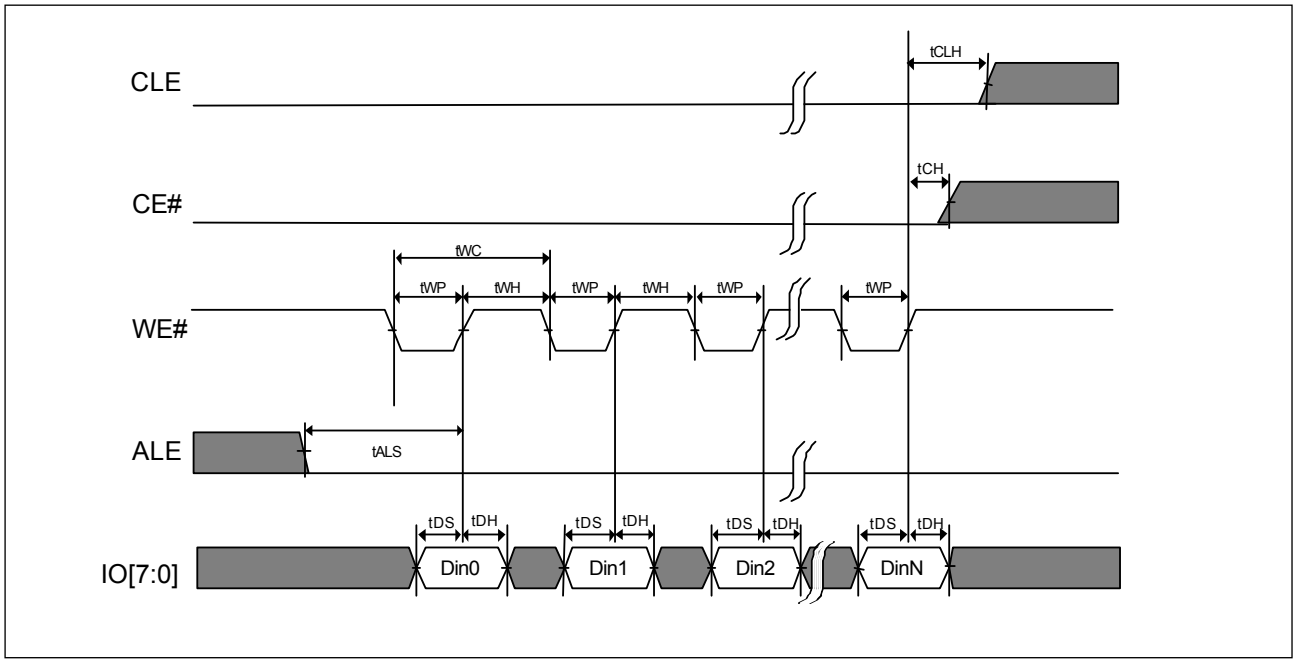


Figure 5. AC Waveforms for Data Input Cycle



PAGE READ

When power is on, the default stage of the NAND flash memory is at read mode, so the 00h command cycle is not needed for the read operation. The MX30LF1G08AA array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the MX30LF1G08AA begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to the waveform for Read Operation as below.

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command. The random read mode is not supported during cache read operation.

Figure 6. AC Waveforms for Read Cycle

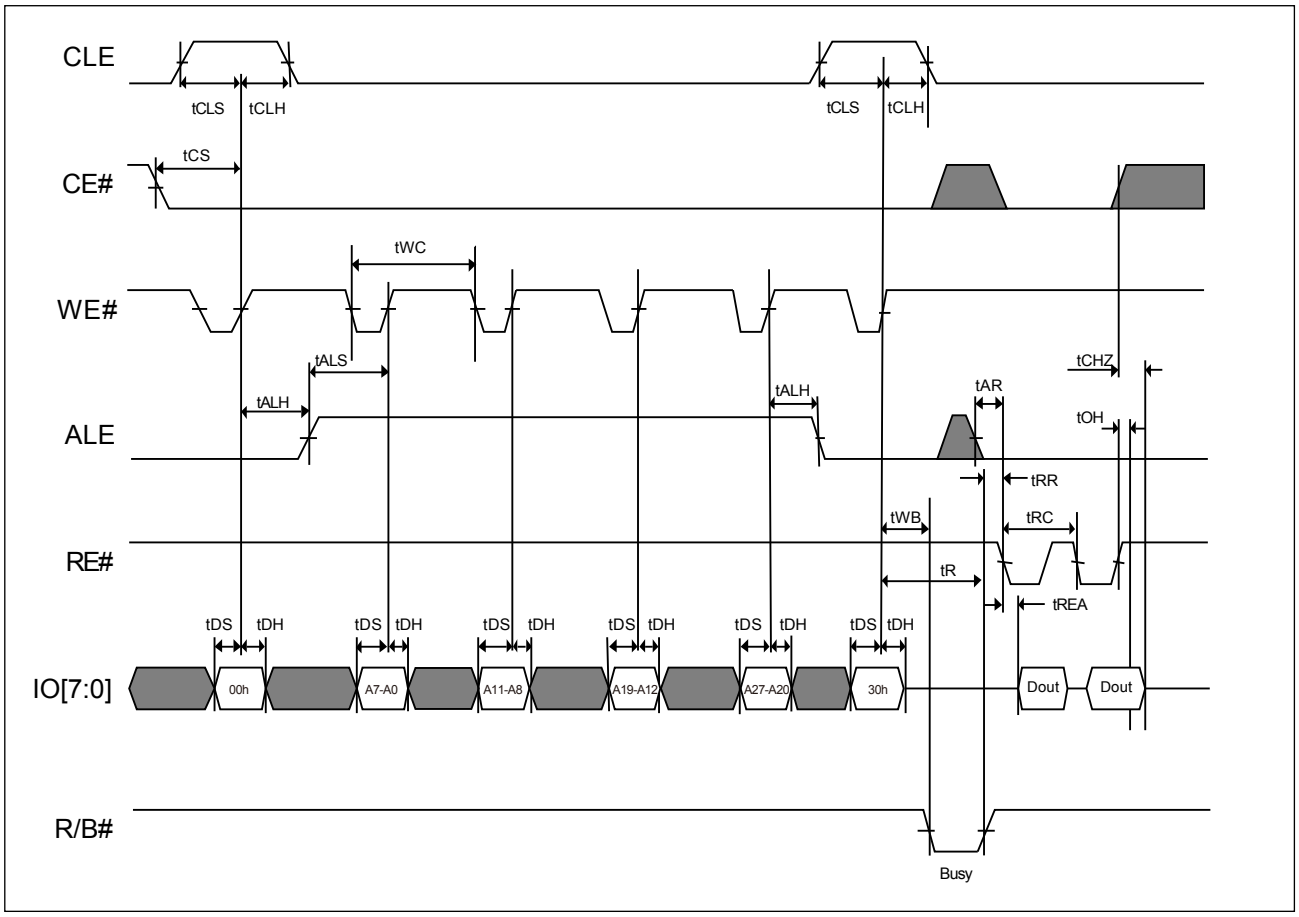


Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)

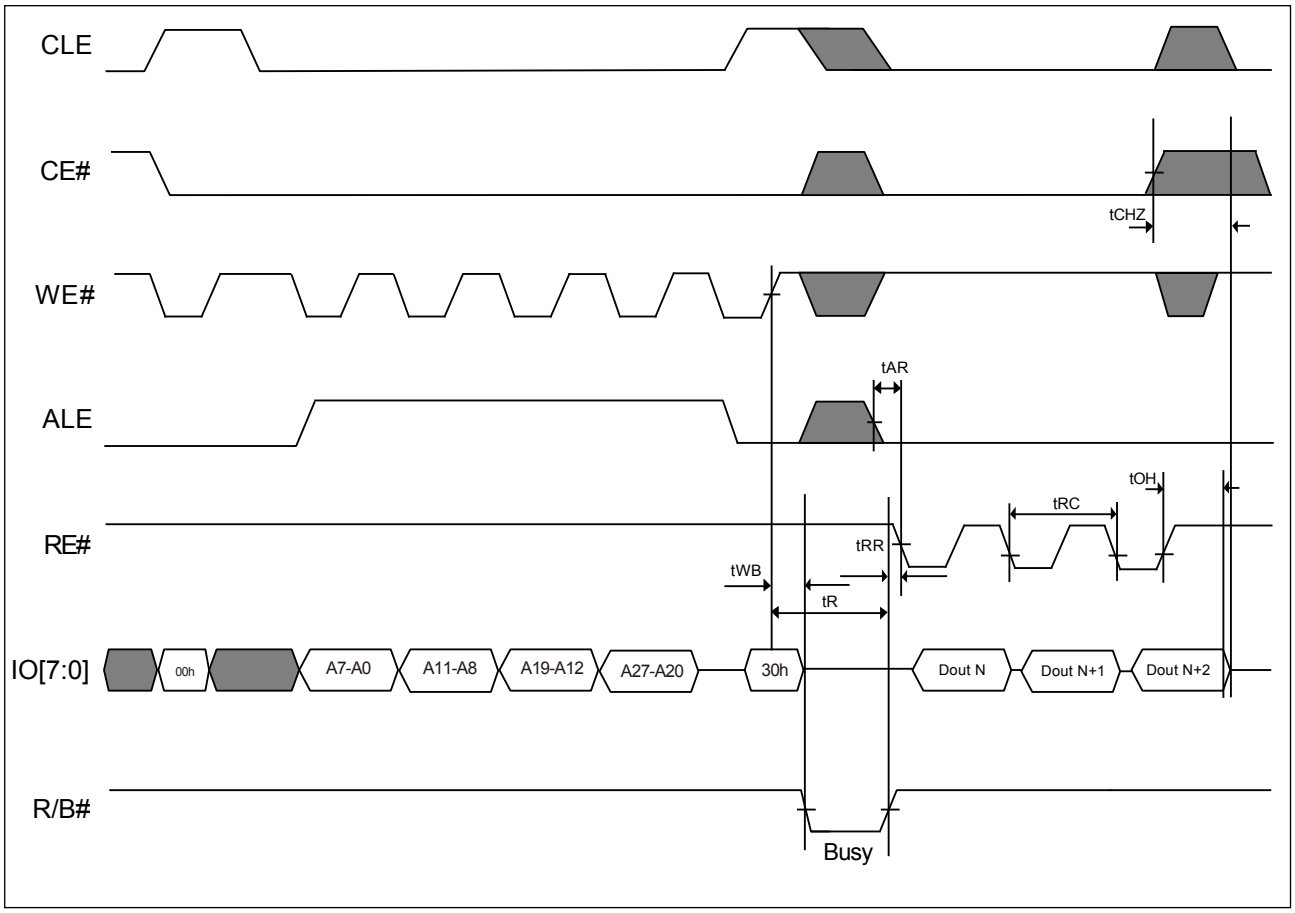
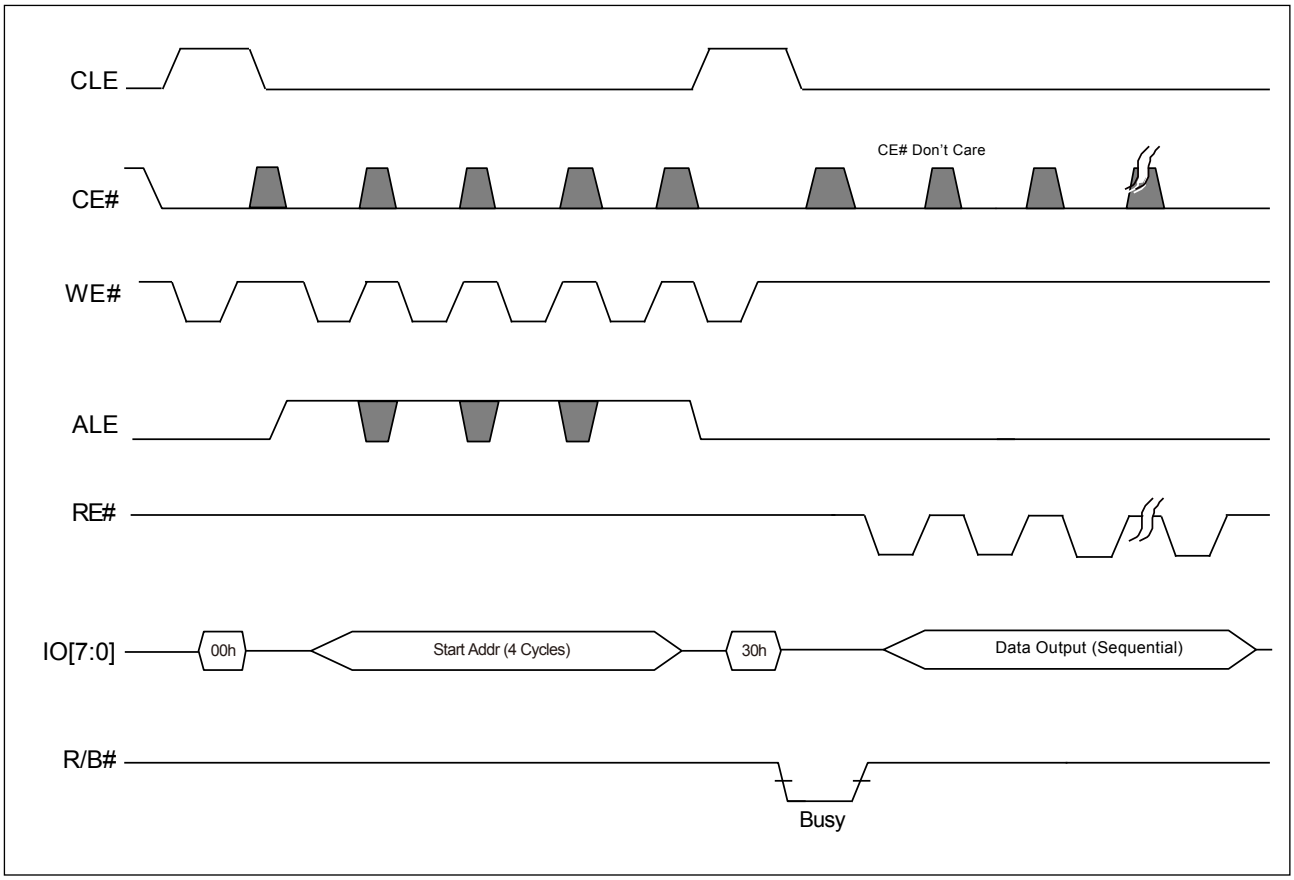


Figure 8. Read Operation with CE# Don't Care



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

Figure 9. AC Waveforms for Sequential Data Out Cycle (After Read)

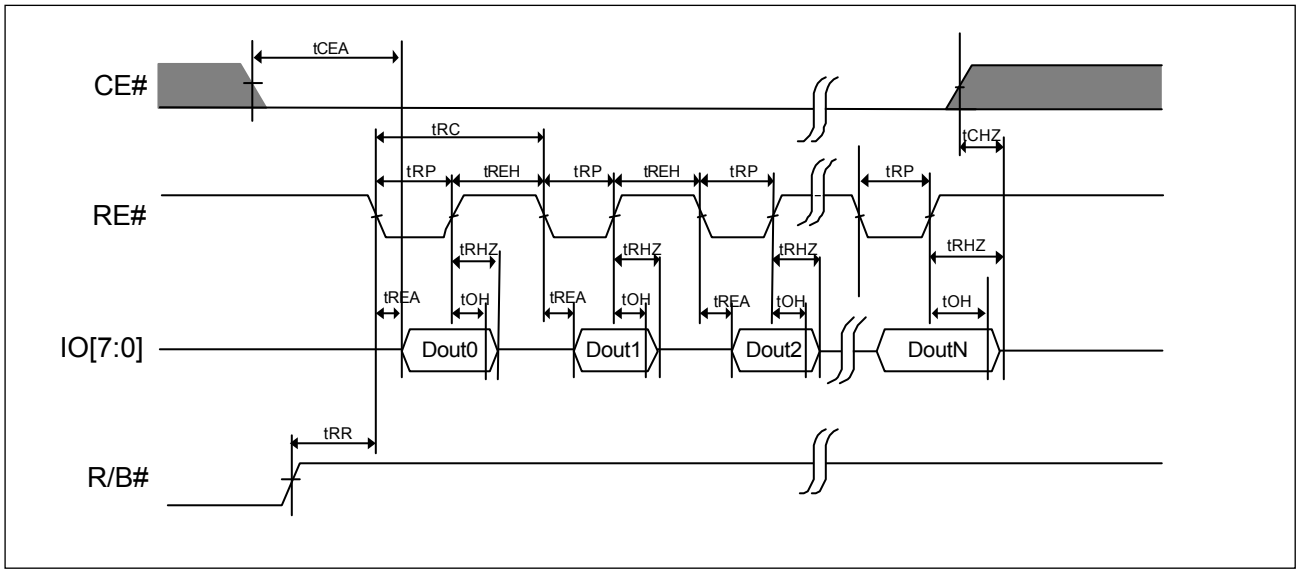
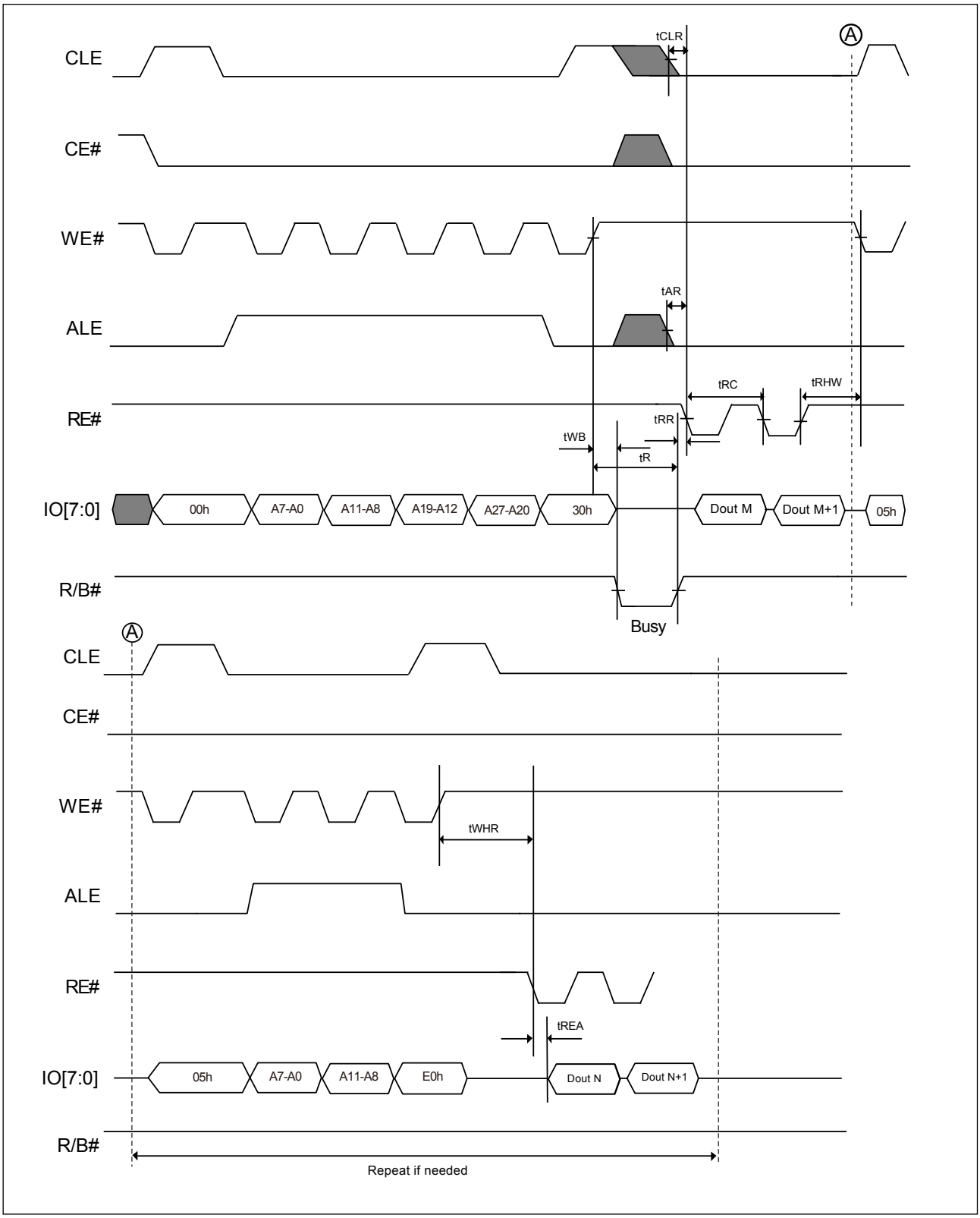


Figure 10. AC Waveforms for Random Data Output



CACHE READ

The cache read operation is for throughput enhancement by using the internal cache buffer. It allows automatic downloading of the consecutive pages and reading the entire flash memory, no additional dead time between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 00h command, the column and row address should be given for the start page selection. The address A[11:0] for the start page should be 000h. Cache read begin command 31h should be issued to start the cache read operation.

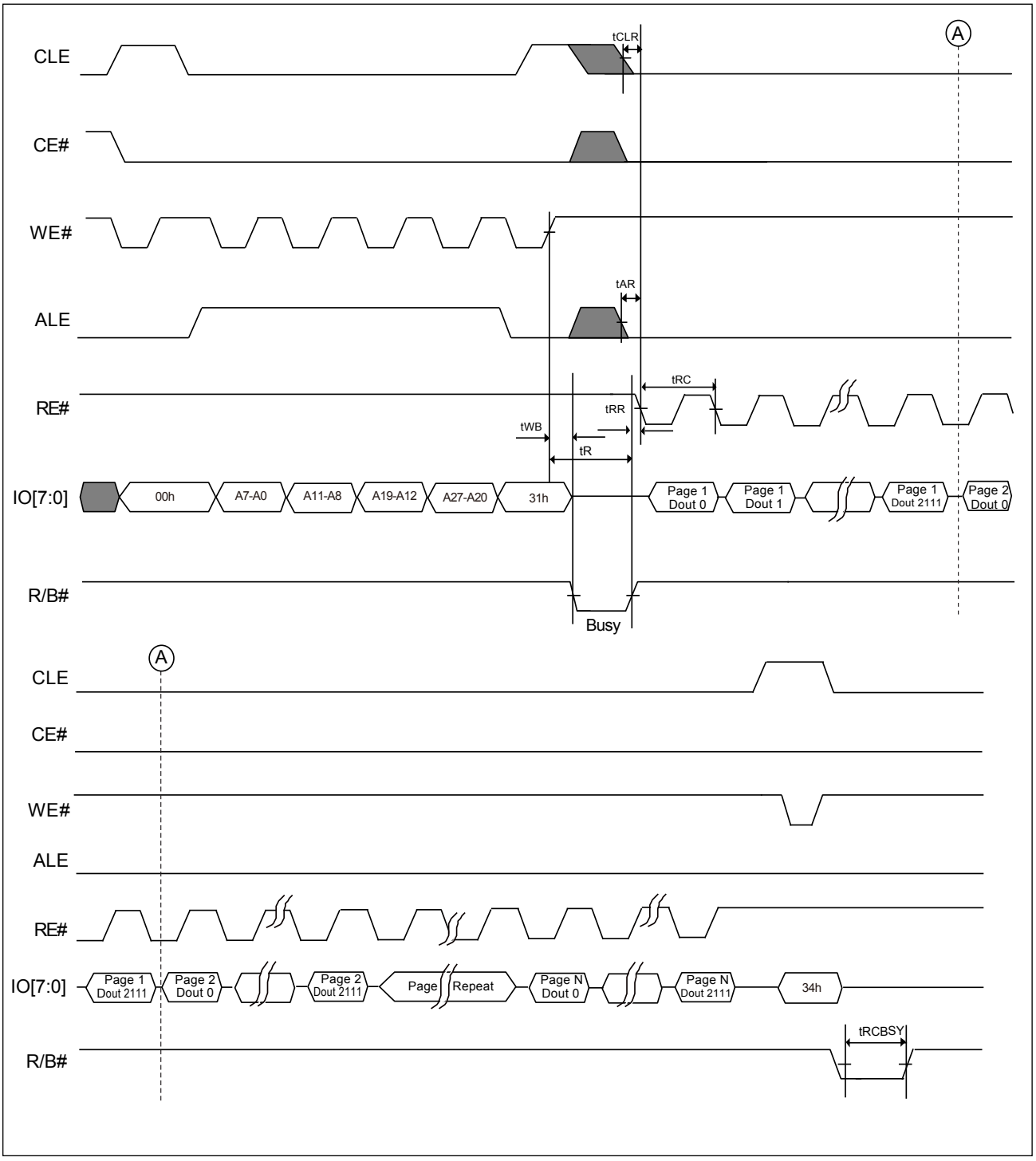
The random data out is not available for cache read operation. After the latency time tR, the data can be read out continuously.

The user can check the chip status by the following method:

- R/B# pin ("0" means the data is not ready, "1" means the user can read the data)

- Status Register (SR[6] behaves the same as R/B# pin, SR[5] indicates the internal chip operation, "0" means the chip is in internal operation and "1" means the chip is idle.) Status Register can be checked after the Read Status command (70h) is issued. Command 00h should be given to return to the cache read operation. To exit the cache read operation, the user needs to issue cache read end command (34h) or Reset command. After the command is issued, the device will become idle within 5 us.

Figure 11. AC Waveforms for Cache Read



PAGE PROGRAM

The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. Partial program in a page is allowed up to 4 times. However, the random data input mode for programming a page is allowed and number of times is not limited.

The status of the program completion can be detected by R/B# pin or Status register bit (IO6).

The program result is shown in the chip status bit (SR[0]). SR[0] = 1 indicates the Page Program is not successful and SR[0] = 0 means the program operation is successful.

During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

Figure 12. AC Waveforms for Program Operation after Command 80H

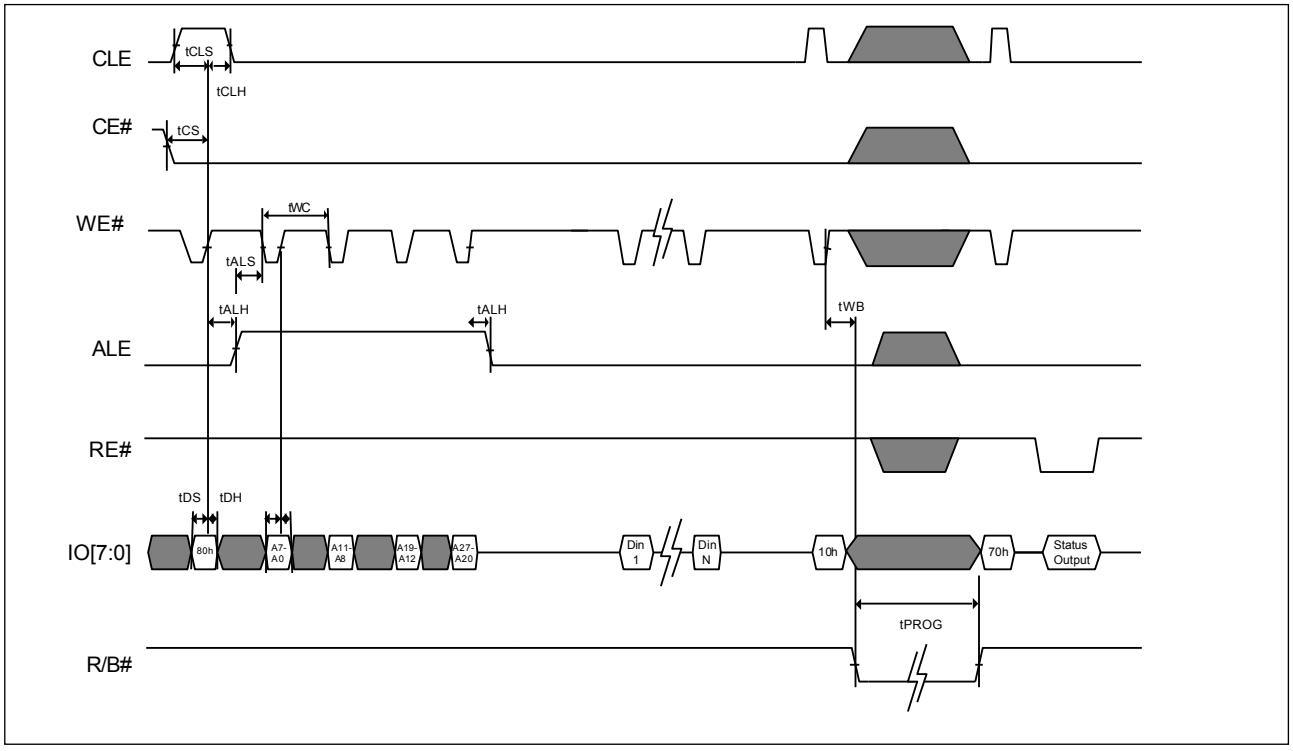
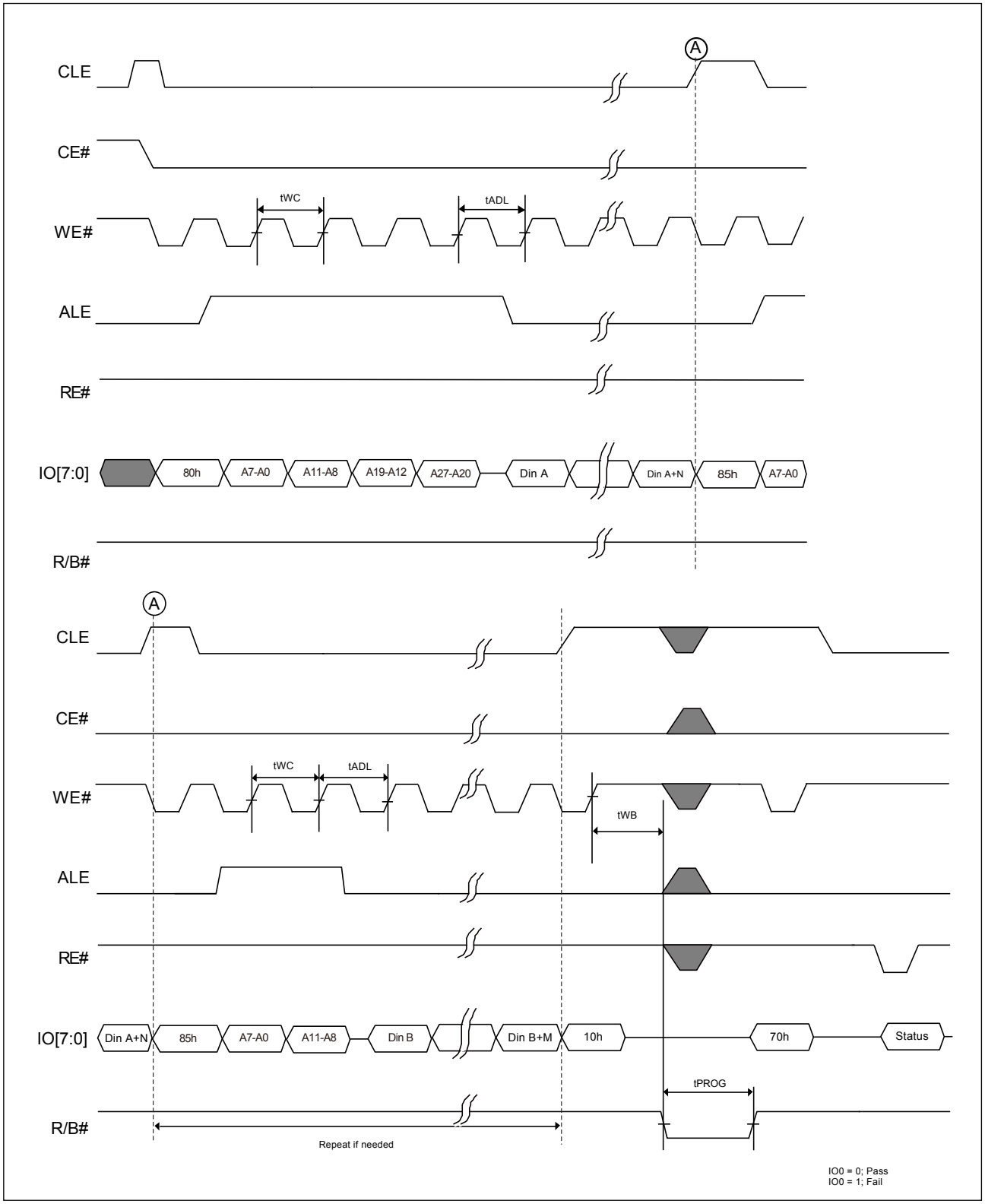
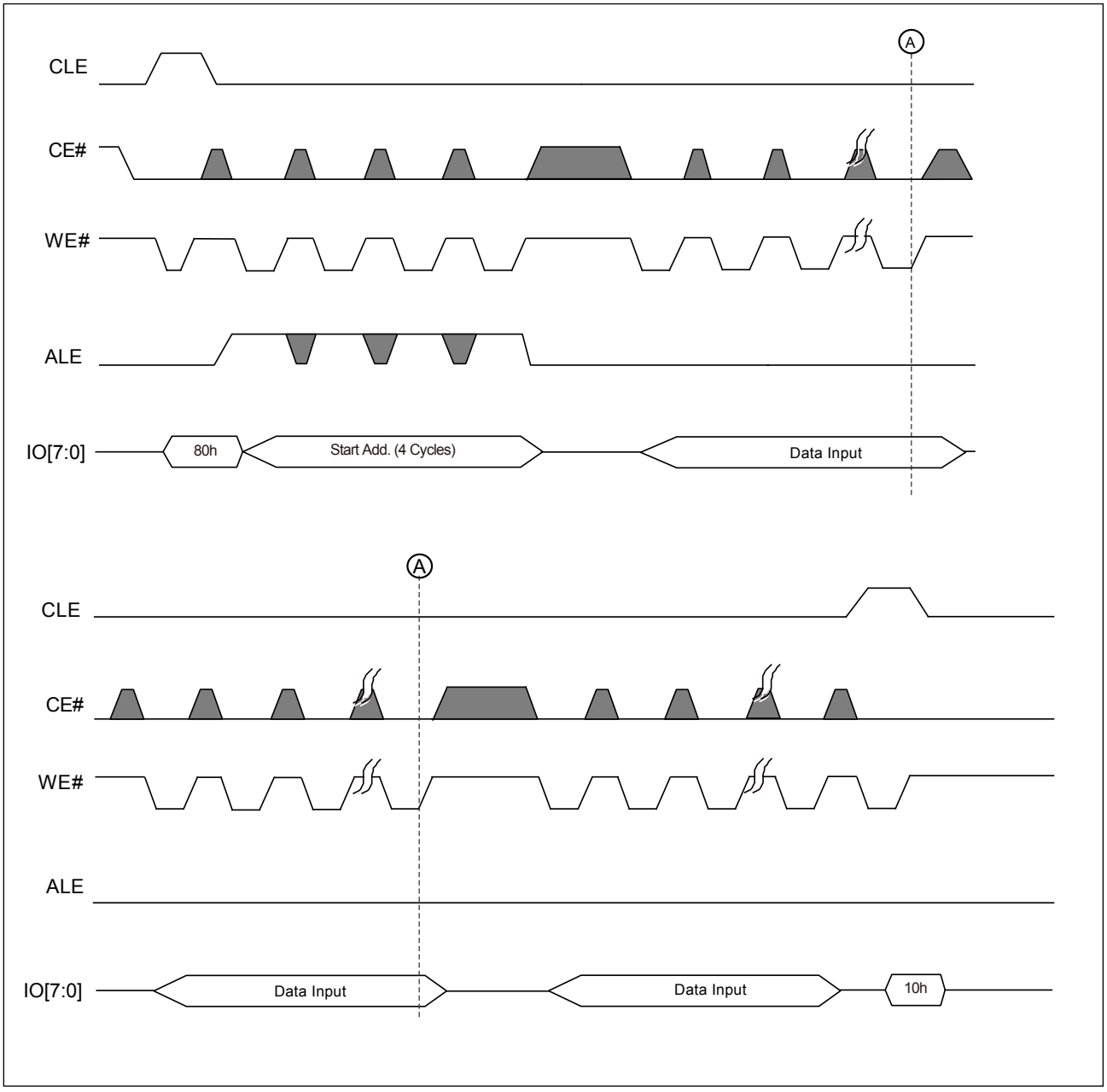


Figure 13. AC Waveforms for Random Data In (For Page Program)



Note: *Random Data In is also supported in cache program.*

Figure 14. Program Operation with CE# Don't Care



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows the controller to directly write data into flash device, and the CE# transitions will not stop the program operation during the latency time.*

CACHE PROGRAM

The cache program feature enhances the program performance by using the cache buffer of 2,112-byte. The serial data can be input to the cache buffer while the previous data stored in the buffer are programming into the memory cell. Cache Program command sequence is almost the same as page program command sequence. Only the Program Confirm command (10h) is replaced by cache Program command (15h).

After the Cache Program command (15h) is issued. The user can check the status by the following methods.

- R/B# pin

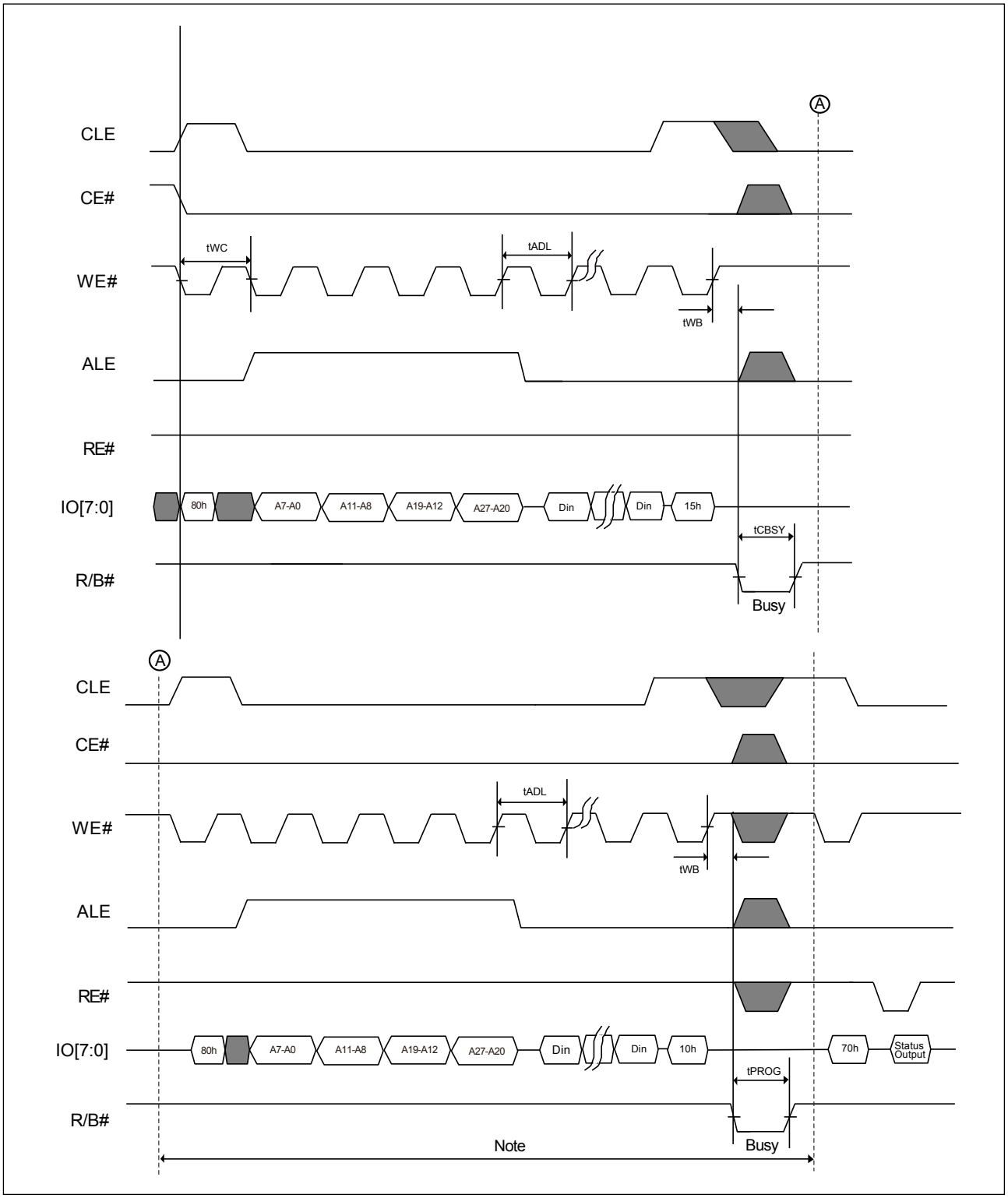
- Cache Status Bit (SR[6] = 0 indicates the cache is busy; SR[6] = 1 means the cache is ready).

The user can issue another Cache Program Command Sequence after the Cache is ready. The user can always monitor the chip state by Ready/Busy Status Bit (SR[5]). The user can issues either program confirm command (10h) or cache program command (15h) for the last page if the user monitor the chip status by issuing Read Status Command (70h).

However, if the user only monitors the R/B# pin, the user needs to issue the program confirm command (10h) for the last page.

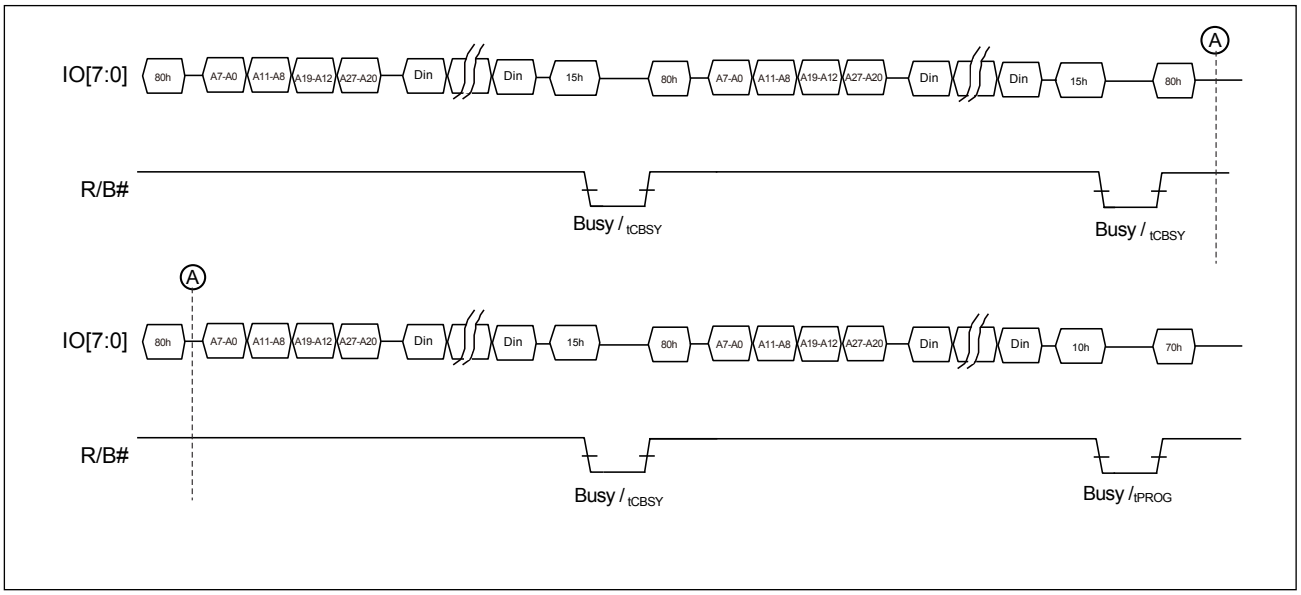
The user can check the Pass/Fail Status through P/F Status Bit (SR[0]) and Cache P/F Status Bit (SR[1]). SR[1] represents Pass/Fail Status of the previous page. SR[1] is updated when SR[6] change from 0 to 1 or Chip is ready. SR[0] shows the Pass/Fail status of the current page. It is updated when SR[5] change from "0" to "1" or the end of the internal programming. For more details, please refer to the related waveforms.

Figure 15-1. AC Waveforms for Cache Program



Note: *It indicates the last page Input & Program.*

Figure 15-2. Sequence of Cache Program



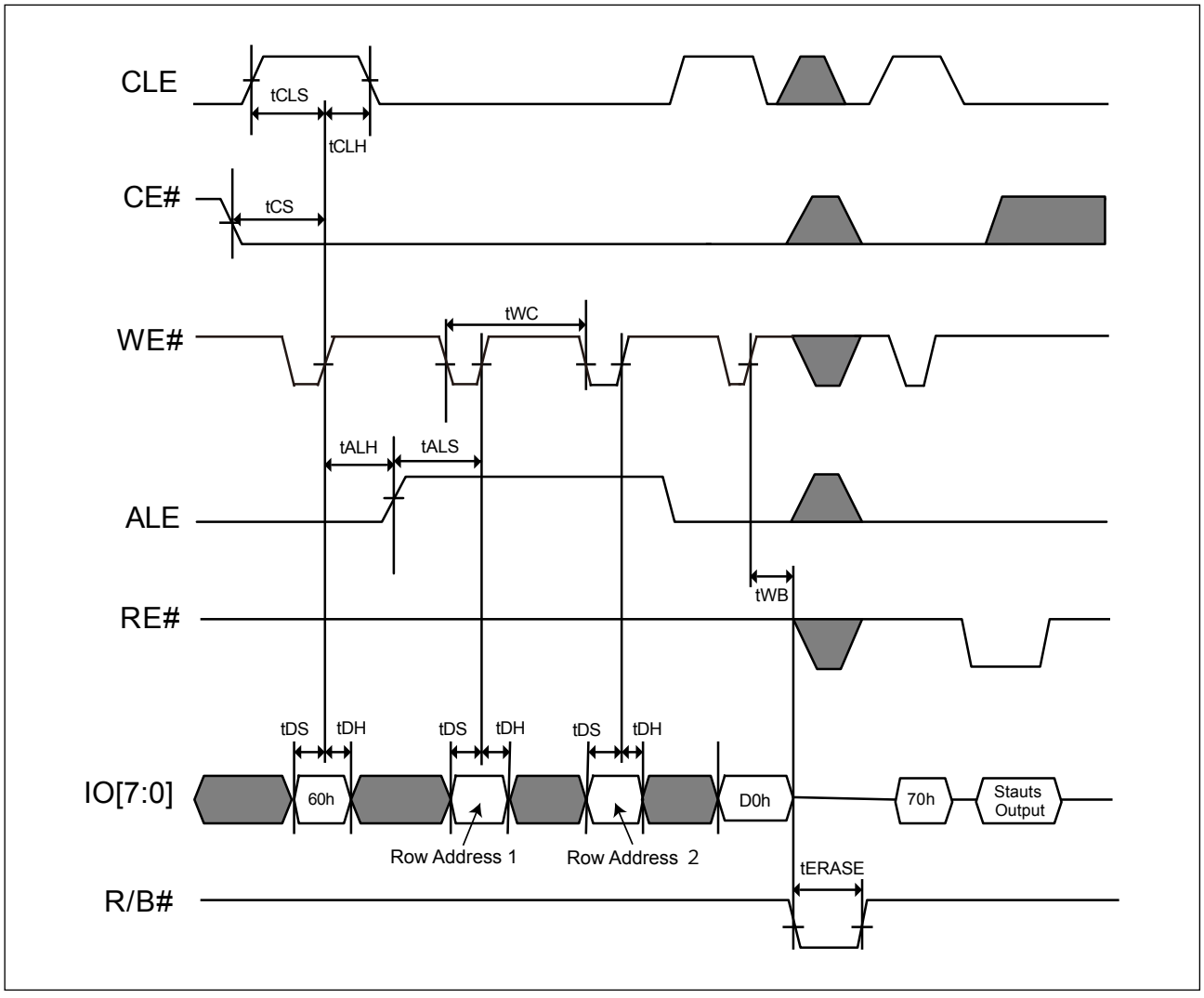
BLOCK ERASE

The MX30LF1G08AA supports a block erase command. This command will erase a block of 64 pages associated with the 10 most significant address bits (A27-A18).

The completion of the erase operation can be detected by R/B# pin or Status register bit (IO6). Recommend to check the status register bit IO0 after the erase operation completes.

During the erasing process, only the read status register command and reset command can be accepted, others are ignored.

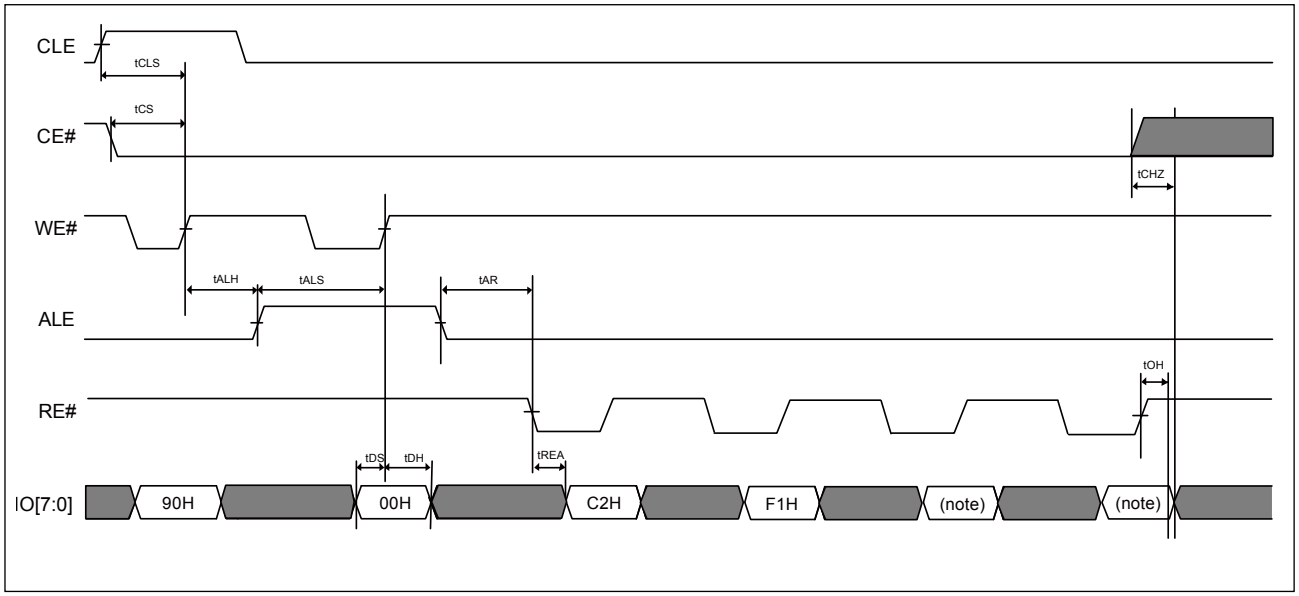
Figure 16. AC Waveforms for Erase Operation



ID READ

The device contains ID codes that identify the device type and the manufacturer. The ID READ command sequence includes one command Byte (90h), one address byte (00h). The Read ID command 90h may provide the manufacturer ID (C2h) of one-byte and device ID (F1h) of one-byte, also 3rd and 4th ID code are followed.

Figure 17. AC Waveforms for ID Read Operation



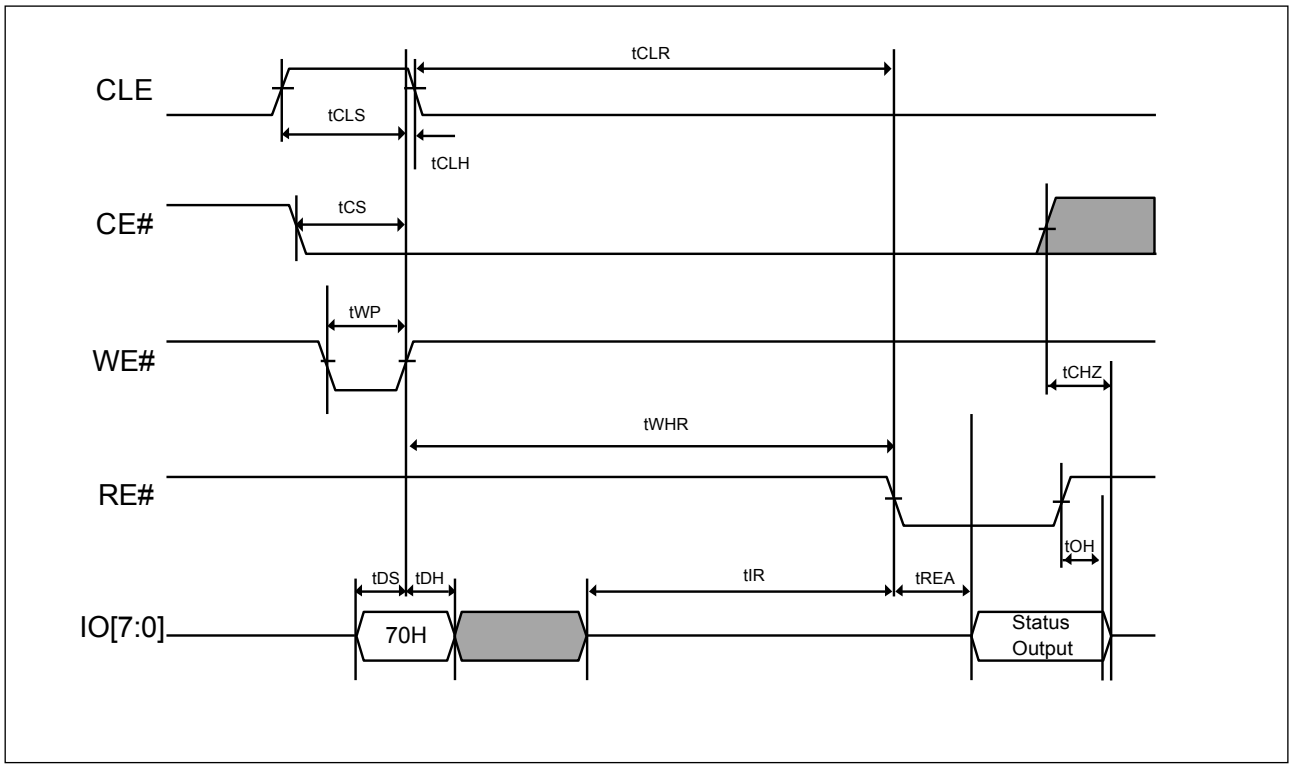
Note: *Also see* ***Table 12. ID Codes Read Out by ID Read Command 90H***.

STATUS READ

The MX30LF1G08AA provides a status register that outputs the device status by writing a command code 70h, and then the IO pins output the status at the falling edge of CE# or RE# which occurs last. Even though when multiple flash devices are connecting in system and the R/B#pins are common-wired, the two lines of CE# and RE# may be checked for individual devices status separately. It is not required to toggle the CE# or RE# for getting the status.

The status read command 70h will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in **Table 11.**

Figure 18. AC Waveforms for Status Read Operation

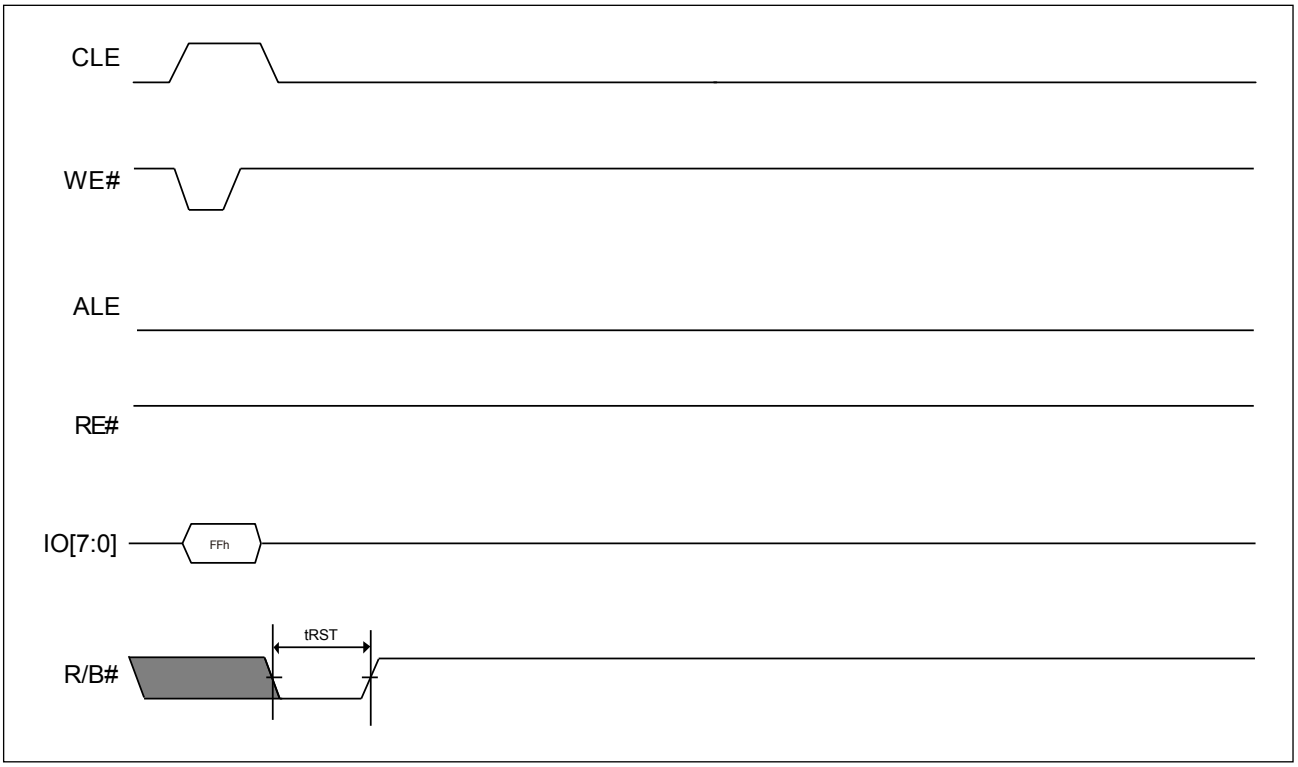


RESET

The reset command FFh resets the read/program/erase operation and clear the status register to be E0h (when WP# is high). The reset command during the program/erase operation will result in the content of the selected locations(perform programming/erasing) might be partially programmed/erased.

If the Flash memory has already been set to reset stage with reset command, the additional new reset command is invalid.

Figure 19. Reset Operation



7. PARAMETERS

7-1. ABSOLUTE MAXIMUM RATINGS

Temperature under Bias	-50°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages with respect to ground (Note 2)	-0.6V to 4.6V
VCC supply voltage with respect to ground (Note 2)	-0.6V to 4.6V
ESD protection	>2000V
All output voltages with respect to ground (Note 2)	-0.6V to 4.6V

Notes:

1. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Minimum voltage may undershoot to -2V for the period of time less than 20ns.*

Table 1. Operating Range

Temperature	VCC	Tolerance
-40°C to +85°C	+3.3 V	2.7 ~ 3.6 V

Table 2. DC Characteristics

Symbol	Parameter	Test Conditions	Min.	Typical	Max.	Unit
VIL	Input low level		-0.3		0.2VCC	V
VIH	Input high level		0.8VCC		VCC+0.3	V
VOL	Output low voltage	IOL =2.1 mA, VCC=VCC MIN			0.4	V
VOH	Output high voltage	IOH= -400uA, VCC=VCC MIN	2.4			V
ISB1	VCC standby current (CMOS)	CE# = VCC - 0.2 V, WP#= 0/VCC		10	50	uA
ISB2	VCC standby current (TTL)	CE# = VIH MIN, WP#= 0/VCC			1	mA
ICC1	VCC active current (Sequential Read)	tRC Minimum CE#= VIL, IOUT=0mA		15	30	mA
ICC2	VCC active current (Program)			15	30	mA
ICC3	VCC active current (Erase)			15	30	mA
ILI	Input leakage current	VIN = 0 to VCC MAX			±10	uA
ILO	Output leakage current	VOUT = 0 to VCC MAX			±10	uA
ILO (R/B#)	Output current of R/B# pin	VOUT = VOL, VCC = VCC MAX	8	10		mA

Table 3. Capacitance

TA = +25°C, F = 1 MHz

Symbol	Parameter	Typ.	Max.	Units	Conditions
CIN	Input capacitance		10	pF	VIN = 0 V
COUT	Output capacitance		10	pF	VOUT = 0 V

Table 4. AC Testing Conditions

Testing Conditions	Value	Unit
Input pulse level	0 to VCC	V
Output load capacitance	1 TTL + CL (50)	pF
Input rise and fall time	5	ns
Input timing measurement reference levels	VCC/2	V
Output timing measurement reference levels	VCC/2	V

Figure 20. Device Under Test

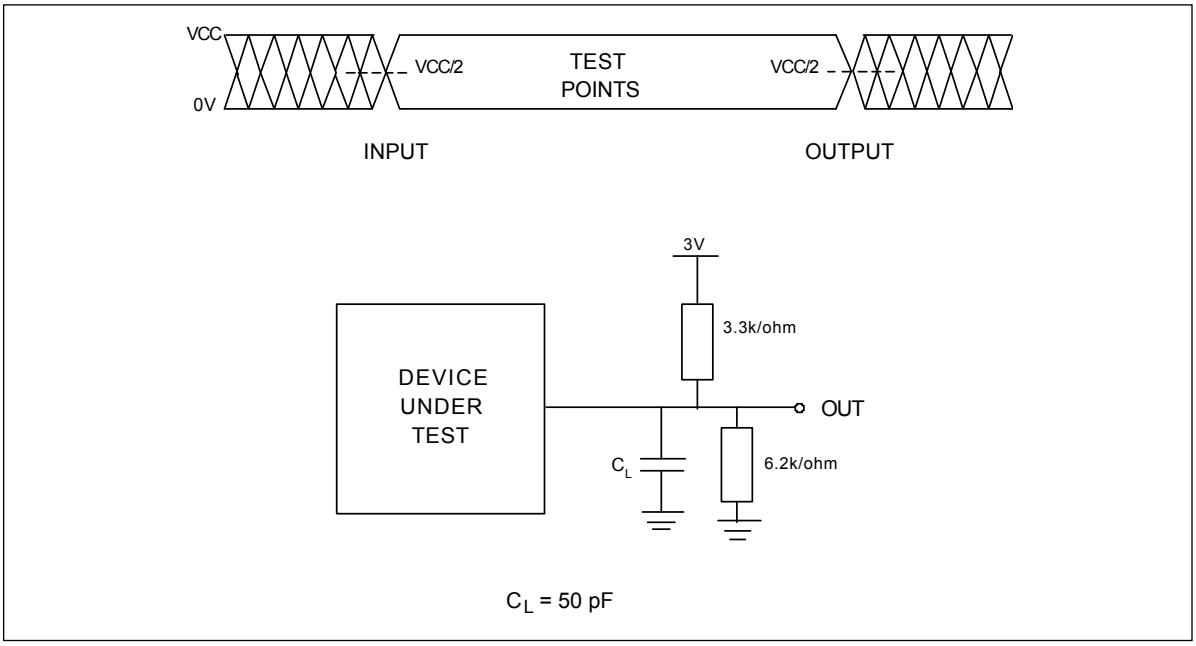


Table 5. Program, Read and Erase Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
tPROG	Page programming time		250	700	us
tCBSY (Program)	Dummy busy time for cache		4	700	us
tRCBSY (Read)	Dummy busy time for cache read			5	us
NOP	Number of partial program cycles in same page			4	cycles
tERASE (Block)	Block erase time		2	3	ms
P/E	Number of program/erase cycles per block	100,000			cycles

Table 6. AC Characteristics over Operating Range

Symbol	Parameter	Min.	Max.	Unit	Notes
tCLS	CLE setup time	15	-	ns	
tCLH	CLE hold time	5	-	ns	
tCS	CE# setup time	20	-	ns	
tCH	CE# hold time	5	-	ns	
tWP	Write pulse width	15	-	ns	
tALS	ALE setup time	15	-	ns	
tALH	ALE hold time	5	-	ns	
tDS	Data setup time	5	-	ns	
tDH	Data hold time	5	-	ns	
tWC	Write cycle time	30	-	ns	
tWH	WE# high hold time	10	-	ns	
tADL	Last address latched to data loading time during program operations	100	-	ns	
tWW	WP# transition to WE# high	100	-	ns	
tRR	Read -to- RE# falling edge	20	-	ns	
tRP	Read pulse width	15	-	ns	
tRC	Read cycle time	30	-	ns	
tREA	RE# access time (serial data access)	-	20	ns	
tCEA	CE# access time	-	25	ns	
tOH	Data output hold time	10	-	ns	
tRHZ	RE# -high-to-output-high impedance	-	50	ns	
tCHZ	CE#-high-to-output-high impedance	-	50	ns	
tREH	RE# -high hold time	10	-	ns	
tIR	Output-high-impedance-to- RE# falling edge	0	-	ns	
tRHW	RE# high to WE# low	0	-	ns	
tWHR	WE# high to RE# low	60	-	ns	
tR	First byte latency	-	25	us	
tWB	WE# high to busy	-	100	ns	
tCLR	CLE low to RE# low	10	-	ns	
tAR	ALE low to RE# low	15	-	ns	
tRST	Device reset time (Idle/Read/Program/Erase)	-	5/5/10/500	us	

Note: *A maximum 5us time is required for the device goes "busy" mode if the FFh (reset command) is setting at ready stage.*

8. SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

The MX30LF1G08AA array is organized as 1024 blocks, which is composed by 64 pages of (2,048+64)-byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for ECC and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access. Each 2K-Byte page has the two area, one is the main area which is 2048-bytes and the other is spare area which is 64-byte.

There are four address cycles for the address allocation, please refer to **Table 7**.

Table 7. Address Allocation

Addresses	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Column address - 1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
Column address - 2nd cycle	*L	*L	*L	*L	A11	A10	A9	A8
Row address - 3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
Row address - 4th cycle	A27	A26	A25	A24	A23	A22	A21	A20

Note: *IO7 to IO4 must be set to Low in the second cycle.*

9. OPERATION MODES: LOGIC AND COMMAND TABLES

Address input, command input and data input/output are managed by the CLE, ALE, CE#, WE#, RE# and WP# signals, as shown in **Table 8.**

Program, Erase, Read and Reset are four major operations modes controlled by command sets, please refer to **Table 9**.

Table 8. Logic Table

Mode	CE#	RE#	WE#	CLE	ALE	WP#
Address Input (Read Mode)	L	H	↑	L	H	X
Address Input (Write Mode)	L	H	↑	L	H	H
Command Input (Read Mode)	L	H	↑	H	L	X
Command Input (Write Mode)	L	H	↑	H	L	H
Data Input	L	H	↑	L	L	H
Data Output	L	↓	H	L	L	X
During Read (Busy)	X	H	H	L	L	X
During Programming (Busy)	X	X	X	X	X	H
During Erasing (Busy)	X	X	X	X	X	H
Program/Erase Inhibit	X	X	X	X	X	L
Stand-by	H	X	X	X	X	0V/VCC

Notes:

1. *H = VIH; L = VIL; X = VIH or VIL*
2. *WP# should be biased to CMOS high or CMOS low for stand-by.*

Table 9. HEX Command Table

	First Cycle	Second Cycle	Acceptable While Busy
Read Mode	00H	30H	
Random Data Input	85H	-	
Random Data Output	05H	E0H	
Cache Read Begin	00H	31H	
Cache Read End	34H		V
Read ID	90H	-	
Reset	FFH	-	V
Page Program	80H	10H	
Cache Program	80H	15H	
Block Erase	60H	D0H	
Read Status	70H	-	V

***Caution**: Any undefined command inputs are prohibited except for above command set.*

The following is an example of a HEX data bit assignment:

Figure 21. Bit Assignment (HEX Data)

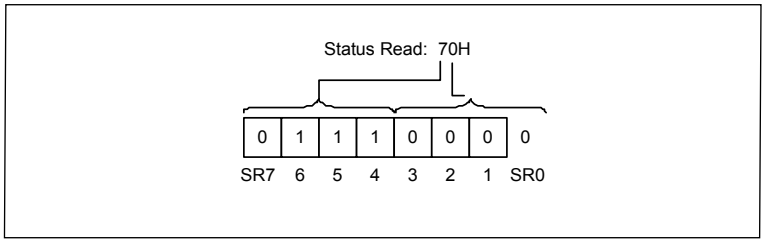


Table 10. Status Output

Pin	Status	Related Mode	Value	
SR[0]	Chip Status	Page Program, Cache Program (Page N), Block Erase	0: Passed	1: Failed
SR[1]	Cache Program Result	Cache Program (Page N-1)	0: Passed	1: Failed
SR[2] - SR[4]	Not Used			
SR[5]	Ready / Busy (For P/E/R Controller)	Cache Program/Cache Read operation, other Page Program/Block Erase/Read are same as IO6	0: Busy	1: Ready
SR[6]	Ready / Busy	Page Program, Block Erase, Cache Program, Read, Cache Read	0: Busy	1: Ready
SR[7]	Write Protect	Page Program, Block Erase, Cache Program, Read	0: Protected	1: Unprotected

Table 11. ID Codes Read Out by ID Read Command 90H

Data	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Hex
Maker Code	1	1	0	0	0	0	1	0	C2H
Device Code	1	1	1	1	0	0	0	1	F1H
3rd Code	1	0	0	0	0	0	0	0	80H
4th Code	0	0	0	1	1	1	0	1	1DH

Table 12. The Definition of 3rd Code of ID Table

Definition	Information	Value
Die number	1 Die	IO1, IO0= 0,0
	2 Die	IO1, IO0= 0,1
	4 Die	IO1, IO0= 1,0
	Reserved	IO1, IO0= 1,1
Cell Structure	Single level cell	IO3, IO2= 0,0
	2x Mult-level cell	IO3, IO2= 0,1
	Reserved	IO3, IO2= 1,0
	Reserved	IO3, IO2= 1,1
Number of concurrently programmed pages	1	IO5, IO4= 0,0
	2	IO5, IO4= 0,1
	3	IO5, IO4= 1,0
	4	IO5, IO4= 1,1
Interleaved programming between diverse devices	Not supported	IO6=0
	Supported	IO6=1
Cache Program	Not supported	IO7=0
	Supported	IO7=1

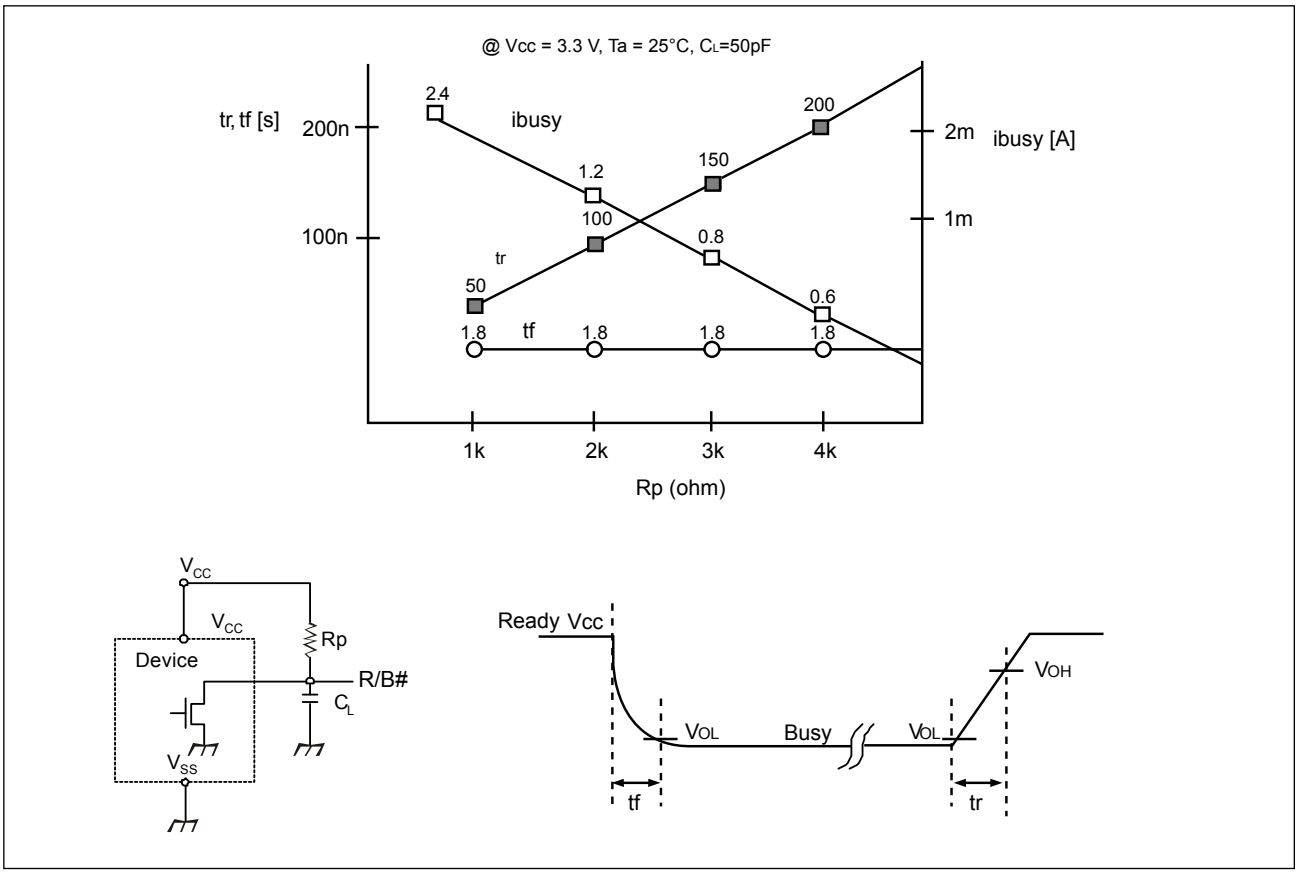
Table 13. The Definition of 4th Code of ID Table

Definition	Information	Value
Page Size (exclude spare area)	1K-byte	IO1, IO0= 0,0
	2K-byte	IO1, IO0= 0,1
	4K-byte	IO1, IO0= 1,0
	Reserved	IO1, IO0= 1,1
Size of spare area (byte per 512-byte)	8	IO2=0
	16	IO2=1
Sequential Read Cycle Time	50ns	IO7, IO3= 0,0
	30ns	IO7, IO3= 0,1
	25ns	IO7, IO3= 1,0
	Reserved	IO7, IO3= 1,1
Block Size (exclude spare area)	64K-byte	IO5, IO4= 0,0
	128K-byte	IO5, IO4= 0,1
	256K-byte	IO5, IO4= 1,0
	512K-byte	IO5, IO4= 1,1
Organization	8-bit	IO6=0
	16-bit	IO6=1

9-1. R/B#: TERMINATION FOR THE READY/BUSY# PIN (R/B#)

The R/B# is an open-drain output pin and a pull-up resistor is necessary to add on the R/B# pin. The R/B# outputs the ready/busy status of read/program/ erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

Figure 22. R/B# Pin Timing Information



Rp Value Guidence

$$Rp\ (min.) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where IL is the sum of the input currnts of all devices tied to the R/B pin.

Rp (max) is determined by maximum permissible limit of tr.

Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.

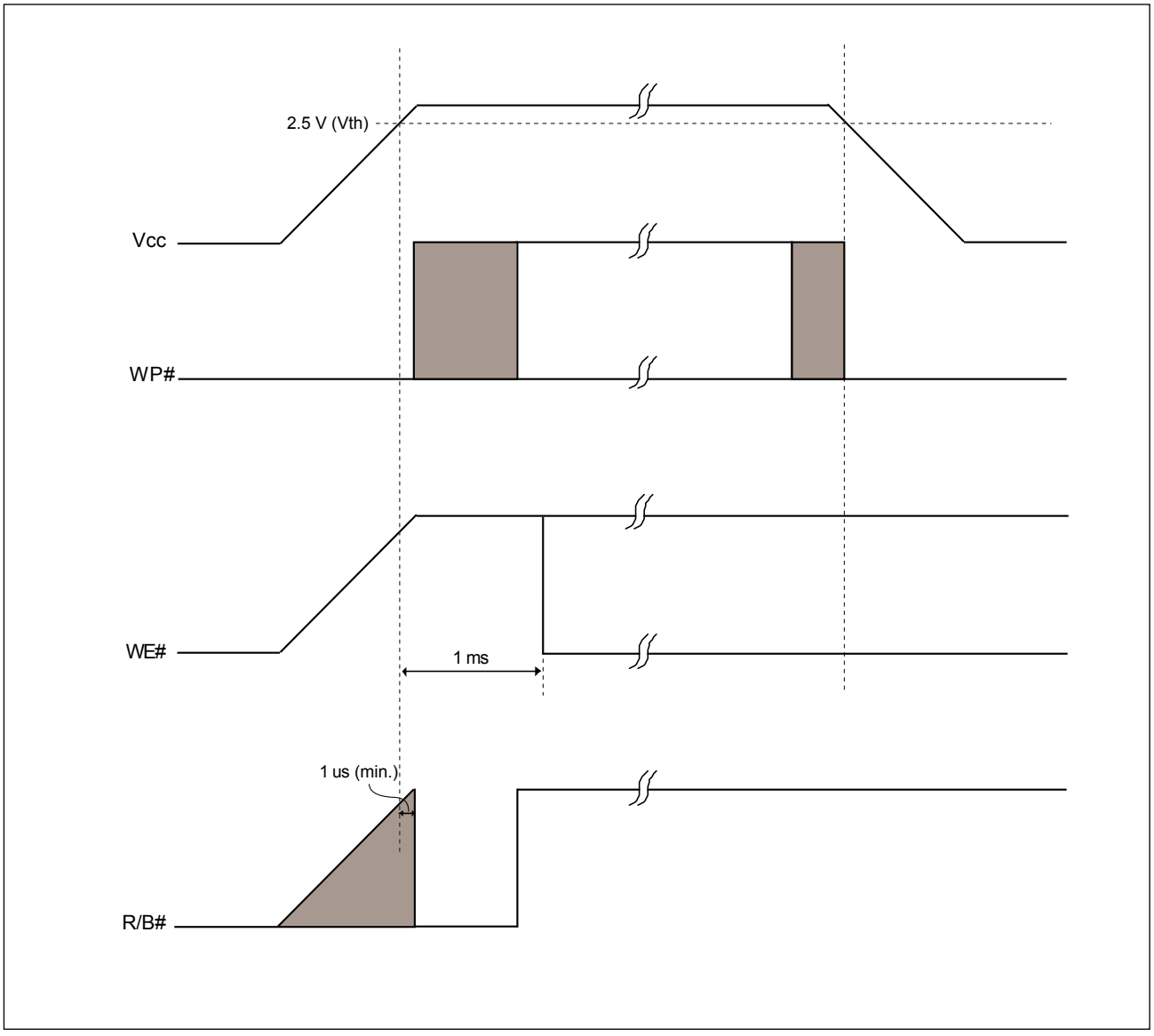
9-2. POWER ON/OFF SEQUENCE

After the Chip reaches the power on level (Vth = 2.5 V), the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. There are two ways to identify the termination of the internal power on reset sequence. Please refer to the “power on/off sequence” waveform.

- R/B# pin
- Wait 1 ms

During the power on and power off sequence, it is recommended to keep the WP# = Low for internal data protection.

Figure 23. Power On/Off Sequence



9-2-1. WP# Signal

Below figures show the relationship between WP# signal and the four operations of the enabled/disable program and enabled/disabled erase.

Figure 24. Enable Programming

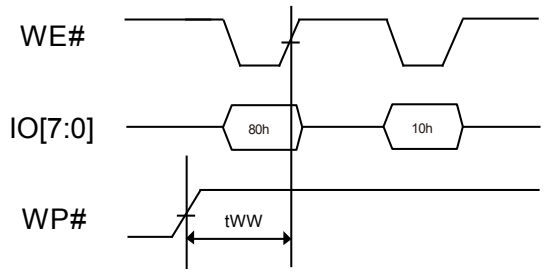


Figure 25. Disable Programming

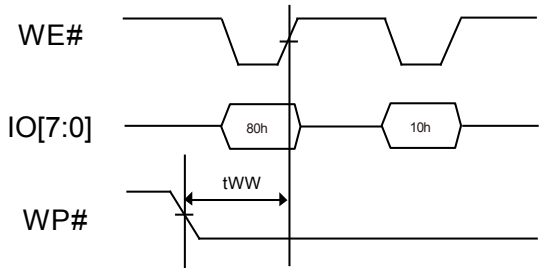


Figure 26. Enable Erasing

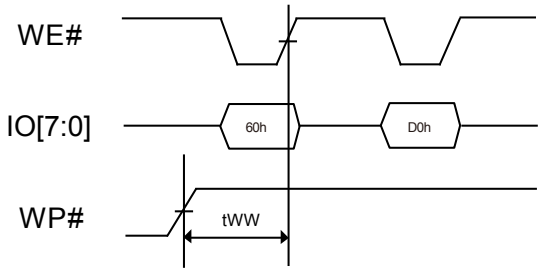
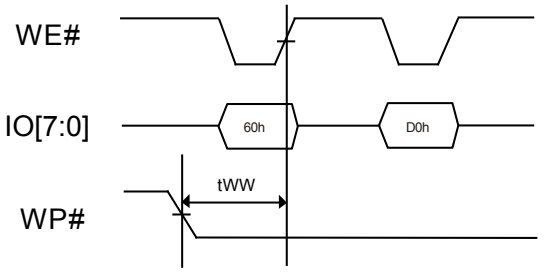


Figure 27. Disable Erasing

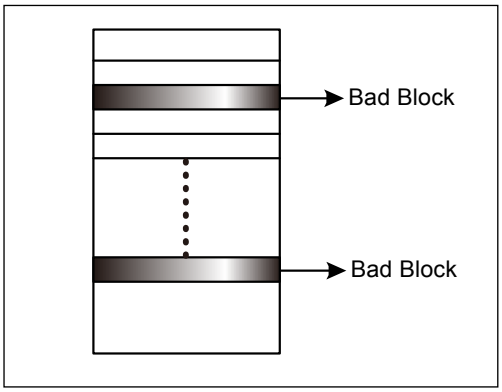


10. SOFTWARE ALGORITHM

10-1. INVALID BLOCKS (BAD BLOCKS)

The bad blocks are included in the device while it is shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is recommended to check the bad block marks and avoid to use the bad blocks. Furthermore, please read out the bad block information before any erase operation since it may be cleared by any erase operation.

Figure 28. Bad Blocks



While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st or 2nd page in the spare area for bad block will not be FFh. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. The figure shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

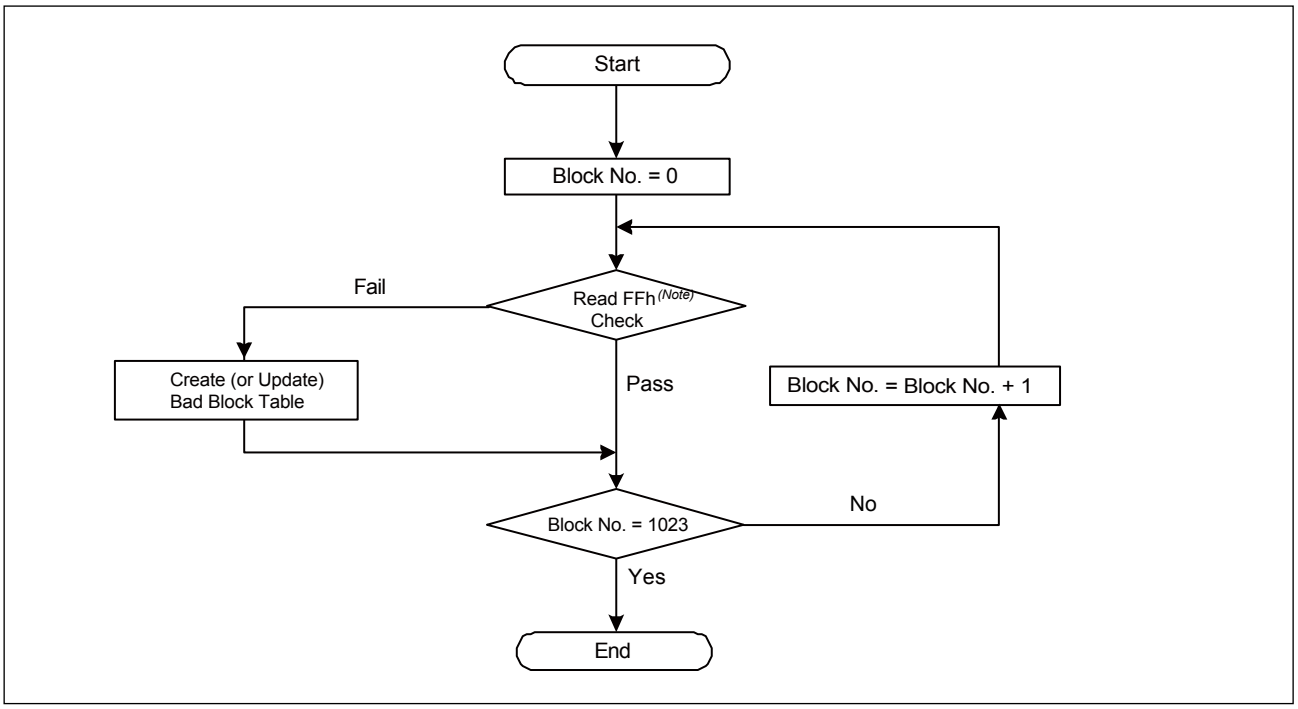
Table 14. Valid Blocks

	Min	Typ.	Max	Unit	Remark
Valid (Good) Block Number	1004		1024	Block	Block 0 is guaranteed to be good up to 1K cycles with 1 bit ECC per 528-byte

10-2. BAD BLOCK TEST FLOW

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. The following section shows the recommended flow for creating a bad block table.

Figure 29. Bad Block Test Flow



Note: *Read FFh check is at the 1st byte of the 1st and 2nd pages of the block spare area.*

10-3. FAILURE PHENOMENA FOR READ/PROGRAM/ERASE OPERATIONS

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

Table 15. Failure Modes

Failure Mode	Detection and Countermeasure	Sequence
Erase Failure	Status Read after Erase	Block Replacement
Programming Failure	Status Read after Program	Block Replacement
Read Failure	Read Failure	ECC

10-4. PROGRAM

When an error occurs in page A, please re-load the data from the data buffer to re-program data to other good page (e.g. page B) of other good blocks. It is recommended to create the bad block table or other method by system software to avoid using the bad blocks.

Figure 30. Failure Modes

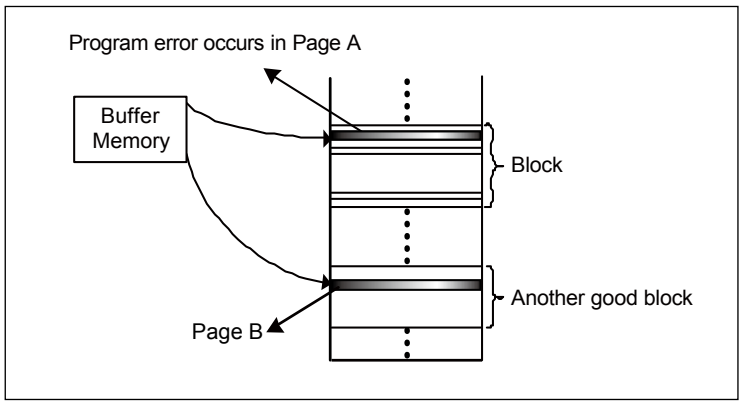
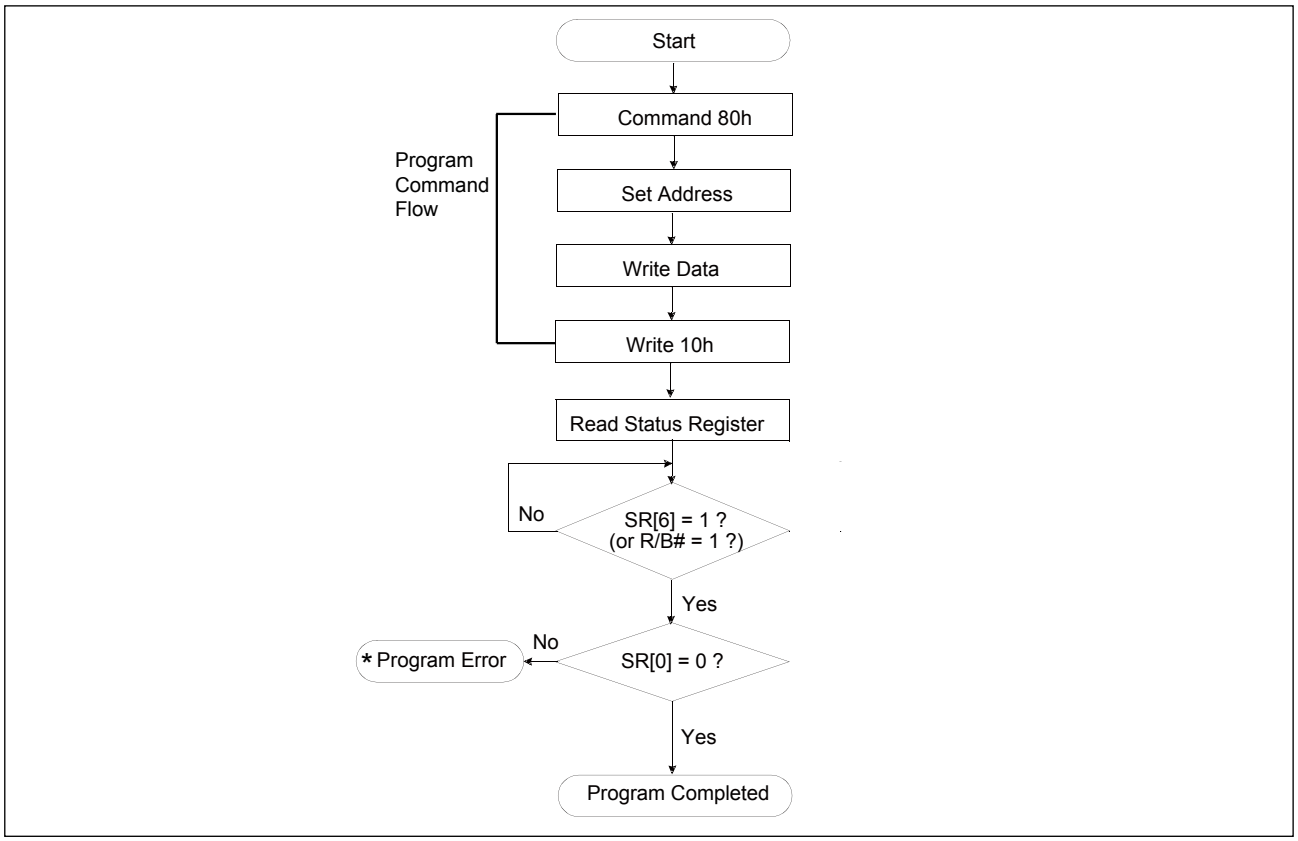


Figure 31. Program Flow Chart



10-5. ERASE

When an error occurs during erase operation, it is recommended to create the bad block table or other method by system software to avoid using the bad blocks.

Figure 32. Erase Flow Chart

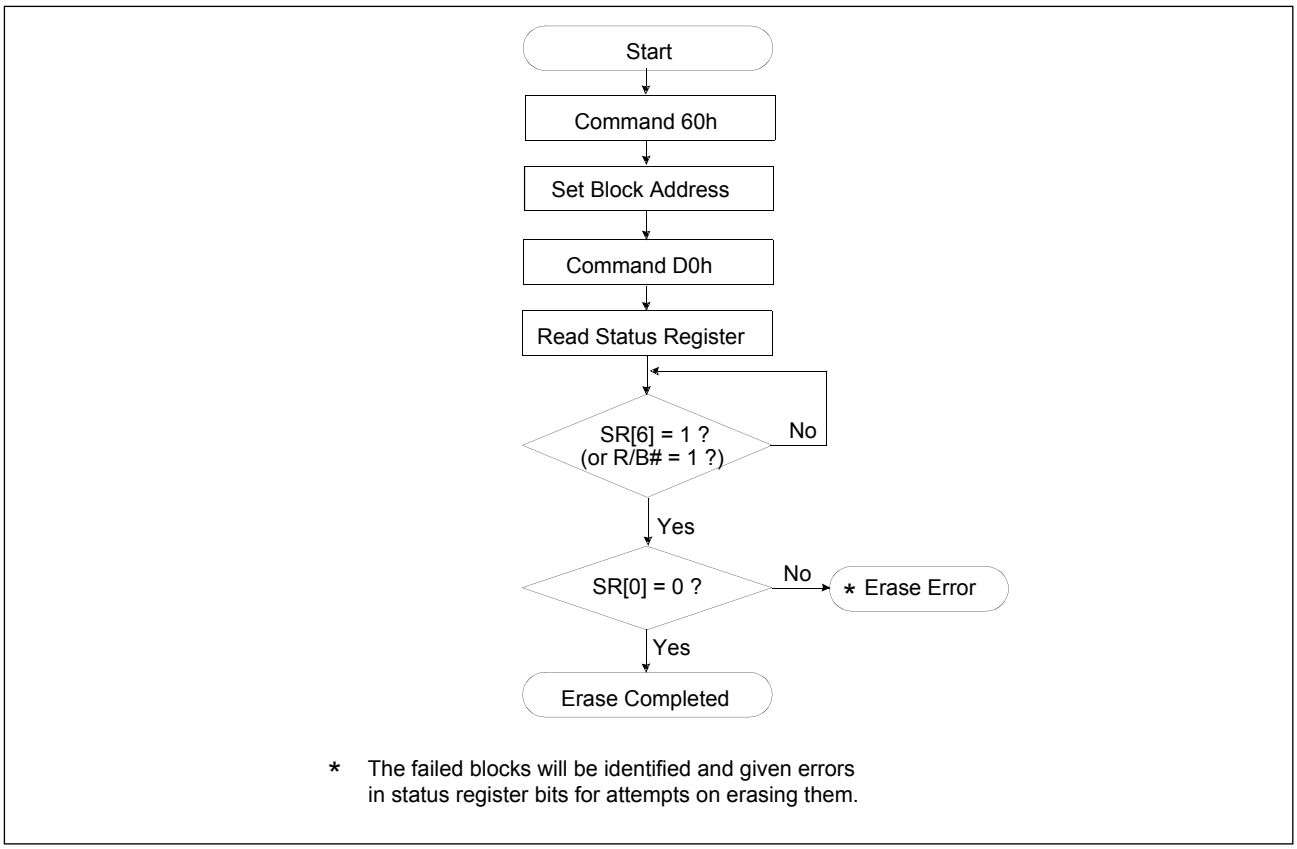
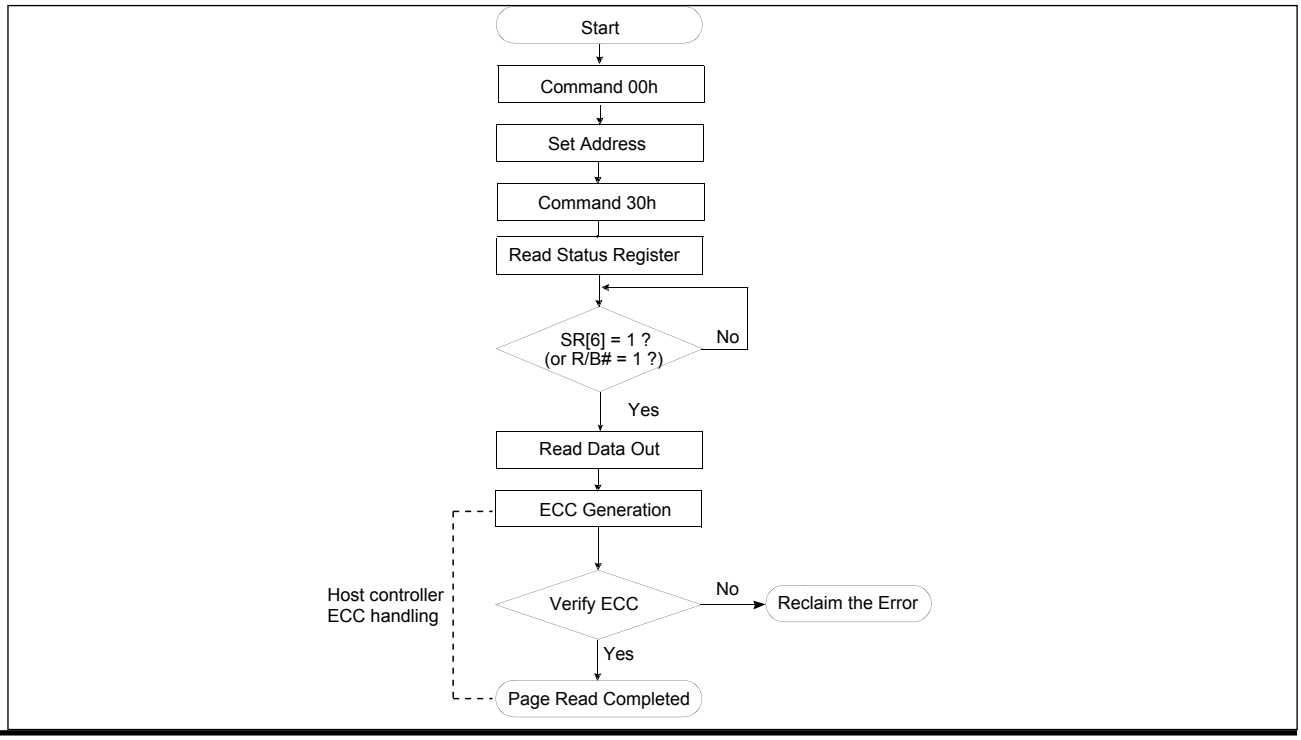


Figure 33. Read Flow Chart



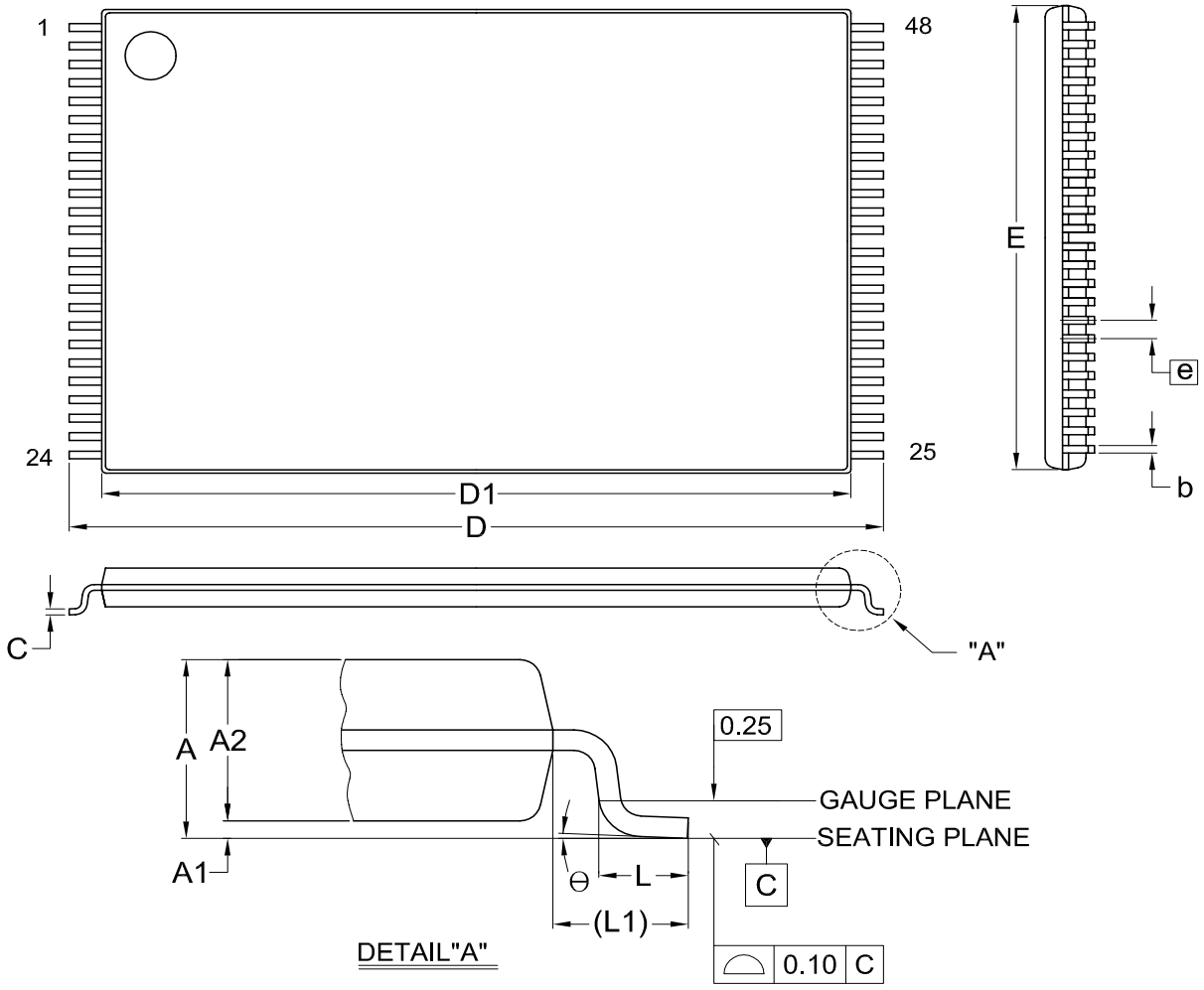
Application Notes

1) Ready time depends on the pull-up resistor tied to the R/B# pin.

2) No programming is allowed on an un-erased page. If this is done no PGM is performed and a status register is given to the user. User then needs only to choose a different address and not to insert the data again. It is recommended to forbid cosecutive programming on its own controller.

11. PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM

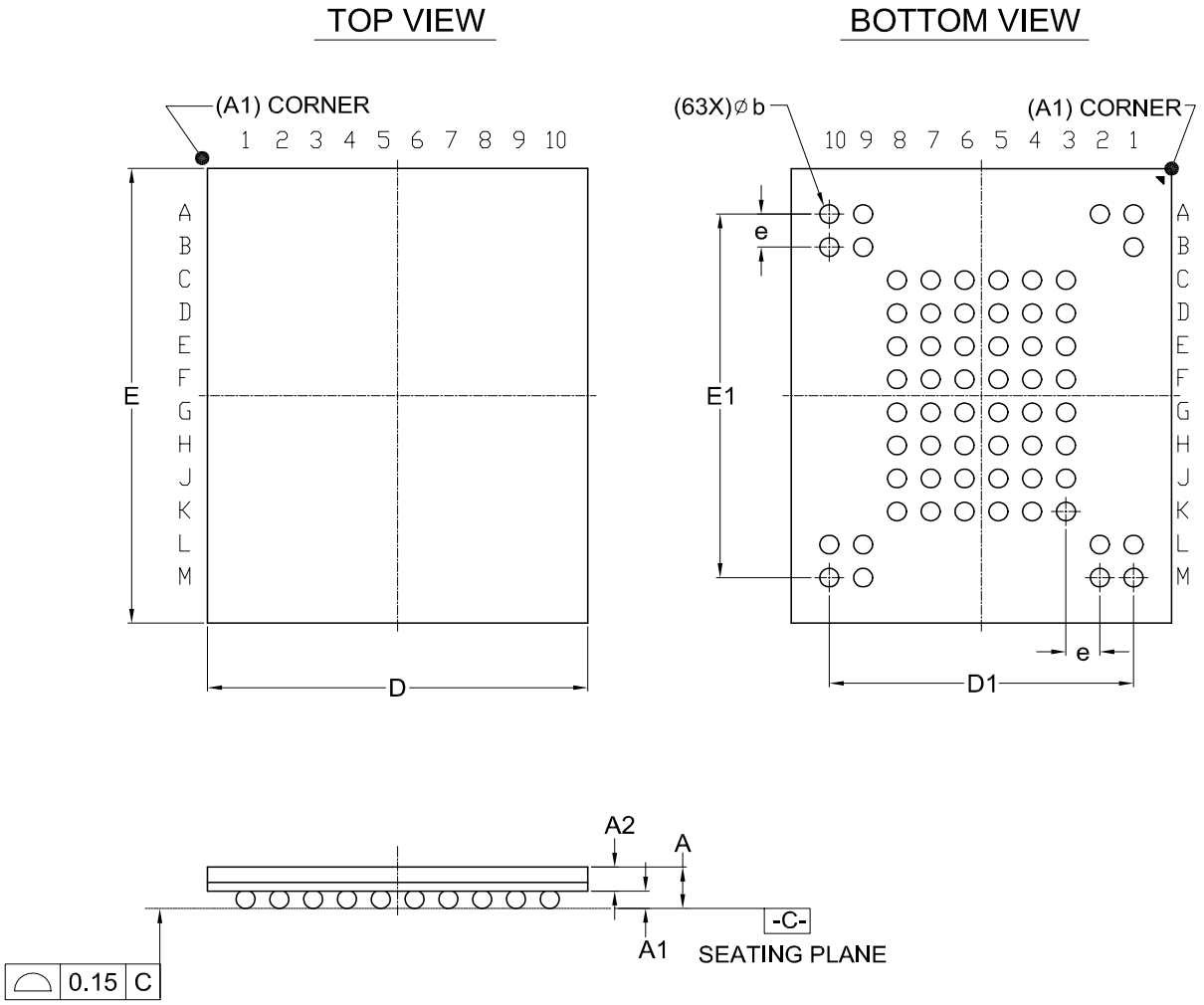


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	—	0.05	0.95	0.17	0.10	19.80	18.30	11.90	—	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	—	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	—	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	—	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

Title: Package Outline for 63-VFBGA (9x11x1.0mm, Ball-pitch: 0.8mm, Ball-diameter: 0.45mm)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.55	0.40	8.90	---	10.90	---	---
	Nom.	---	0.30	---	0.45	9.00	7.20	11.00	8.80	0.80
	Max.	1.00	0.40	---	0.50	9.10	---	11.10	---	---
Inch	Min.	---	0.010	0.022	0.016	0.350	---	0.429	---	---
	Nom.	---	0.012	---	0.018	0.354	0.283	0.433	0.346	0.031
	Max.	0.039	0.016	---	0.020	0.358	---	0.437	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4267	0				

12. REVISION HISTORY

Rev. No.	Descriptions	Page	Date
0.01	1. Figures 3, 5, 6, 7, 8, 10, 12, 15, 16, 17, 18, 22, 24, modified	P10, 12 to 14, 16, 17, P22 to 25, 31 to 33, 37, 39 to 43	OCT/19/2011
	2. Chapter 8 & 9: description updated	P32, 33	
	3. Table 8. Logic & Command Table modified	P33	
0.02	1. "Optional code" added in part number	All	APR/18/2011
	2. NOP modified from 8 (main area plus spare area) to 4	P16, 28	
	3. Typical program time modified from 200us to 250us	P4, 28	
	4. Ready/busy pin timing information axis adjustment	P37	
	5. Power on timing spec modified from 2ms to 1ms	P38	
0.03	1. Changed datasheet title to Preliminary	P4	MAY/05/2011
0.04	1. Ordering information revised due to part name changed from MX30LF1G08AM to MX30LF1G08AA	All	AUG/19/2011
	2. Wording-rephrase & capitalization	All	
	3. Waveforms adjustment	All	
	4. Table 2. VLKO specifications removed	P30	
0.05	1. Rephrased and adjusted waveform sequences	All	DEC/28/2011
	2. Added "DNU" ball for VFBGA	P6	
	3. Modified Figure "AC Waveform for Cache Read"	P17	
	4. Added the check mark of "Acceptable while busy" for Cache Read End item in Command Table	P34	
	5. Added "Read Failure" in table of Failure Modes	P41	
	6. Marked the VFBGA as "Advanced Information"	P4, 5	
	7. Removed "Secure OTP (Optional)"	P4	
	8. Removed C grade descripton	P4, 5, 29	
	9. Added R/B# timing in Power On/Off Waveform	P38	
0.06	1. Modified the VFBGA ball-out: H8 from "NC" to "VCC"	P6	FEB/08/2012
1.0	1. Removed "Preliminary" from Datasheet title	P4	JUN/04/2012
1.1	1. Removed "Advanced Information" for VFBGA package	P4, 5	AUG/13/2012
1.2	1. Content wording rephrased	P9, 32, 37, 39, 40, 42	MAR/28/2013
	2. Flow chart modifications	P42,43	
1.3	Added "Bad Block Table Build up" descriptions	P41	DEC/18/2013
1.4	Changed tCLR from 15ns to 10ns	P31	FEB/27/2014

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