MX29SL400C T/B

DATASHEET

The MX29SL400C T/B product will be phase-out, and is not recommended for new design.

4M-BIT [512K x 8 / 256K x 16] SINGLE VOLTAGE 1.8V ONLY FLASH MEMORY

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FEATURES

GENERAL FEATURES

- Single Power Supply Operation
  - 1.65 to 2.2 volt for read, erase, and program operations
- 524,288 x 8 / 262,144 x 16 switchable
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Sector Structure
  - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1, and 64K-Byte x 7
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotected allows code changes in previously locked sectors
- Latch-up protected to 100mA from -1V to Vcc + 1V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Access time: 90ns
  - Byte/Word program time: 12us/18us (typical)
  - Erase time: 1.3s/sector, 9s/chip (typical)
- Low Power Consumption
  - Low active read current: 6mA (maximum) at 5MHz
  - Low standby current: 1uA (typical)
- Minimum 100,000 erase/program cycle
- 10 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

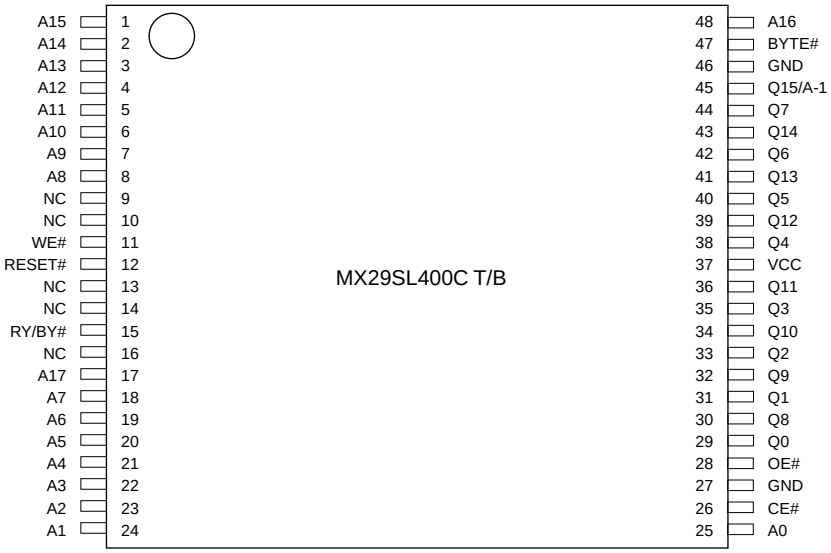
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode

PACKAGE

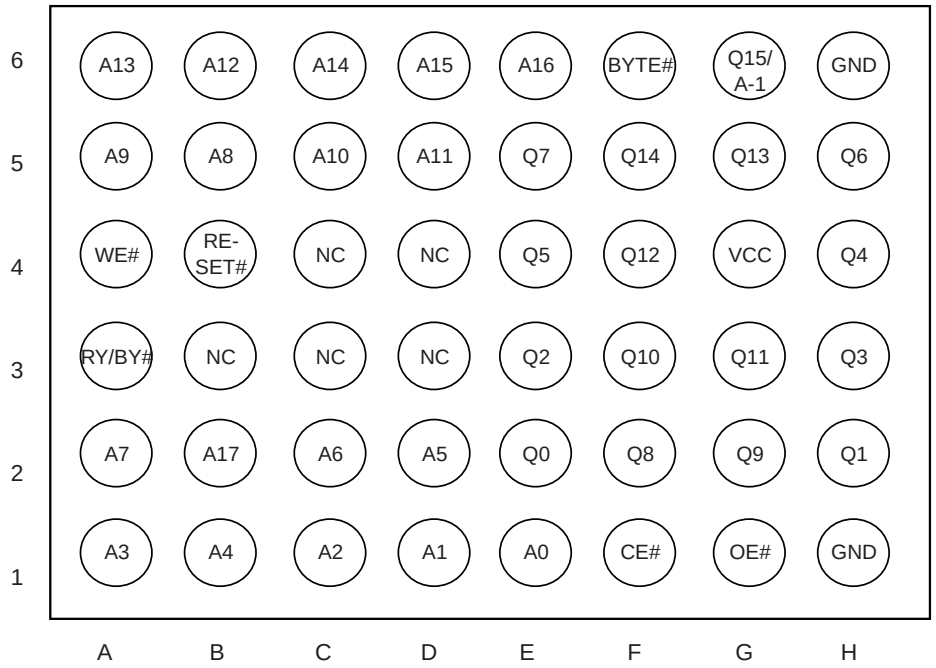
- 48-Pin TSOP
- 48-Ball CSP (6x8x1.2mm, 6x8x1.3mm, 4x6x0.75mm)
- 48-Ball XFLGA (4x6x0.5mm)
- **All Pb-free devices are RoHS Compliant**

PIN CONFIGURATIONS

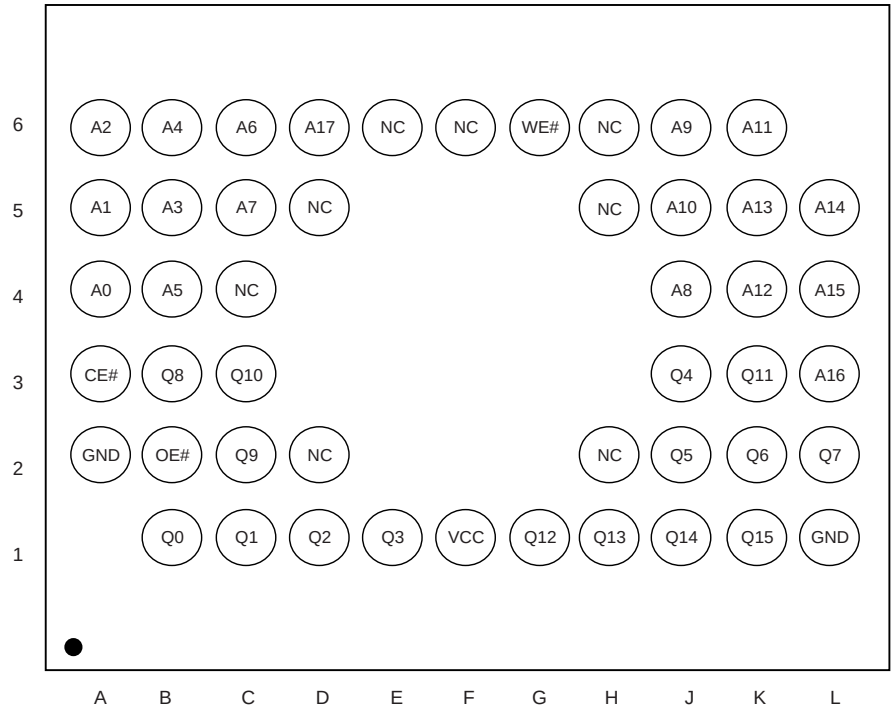
48 TSOP (Standard Type) (12mm x 20mm)



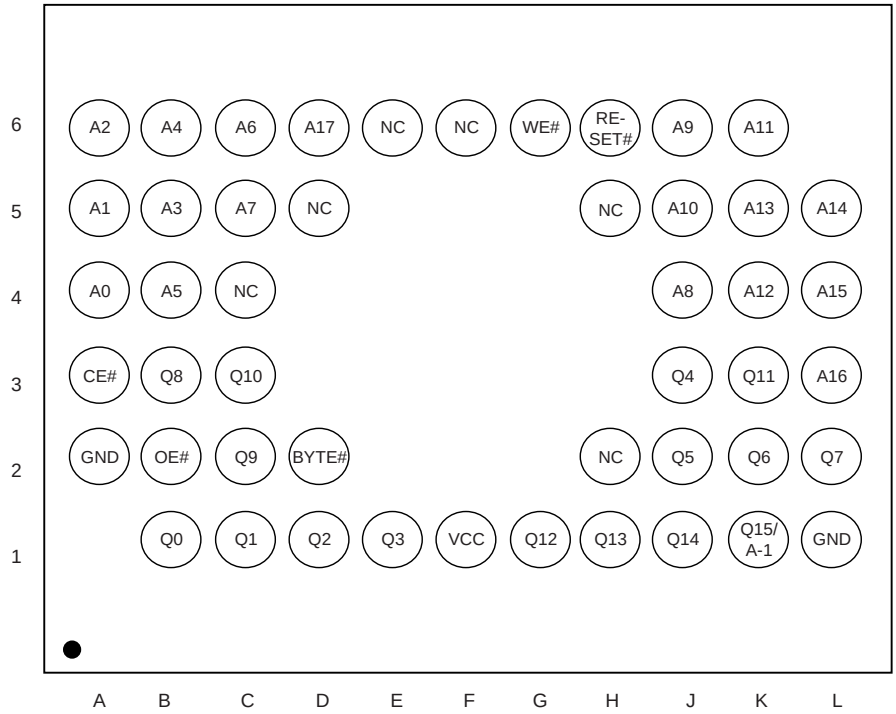
48-Ball CSP (6x8x1.2mm/ 6x8x1.3mm, Ball Pitch = 0.8 mm), Top View, Balls Facing Down



48-Ball CSP(4x6x0.75mm, Ball Pitch = 0.5 mm), Top View, Balls Facing Down



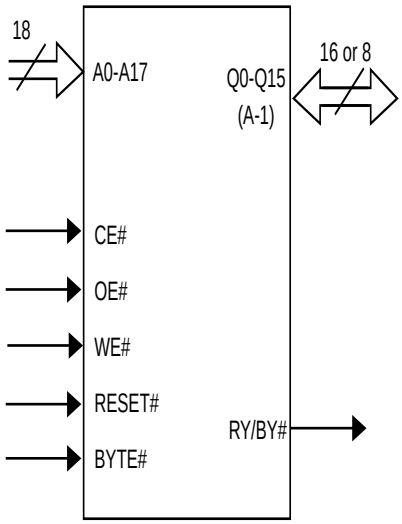
48-Ball XFLGA (4x6x0.5mm, Land Pitch = 0.5mm), Top View, Balls Facing Down



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15 (data input/output, word mode)/ A-1(LSB address input, byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (1.65V~2.2V)
GND	Ground Pin

LOGIC SYMBOL



BLOCK DIAGRAM

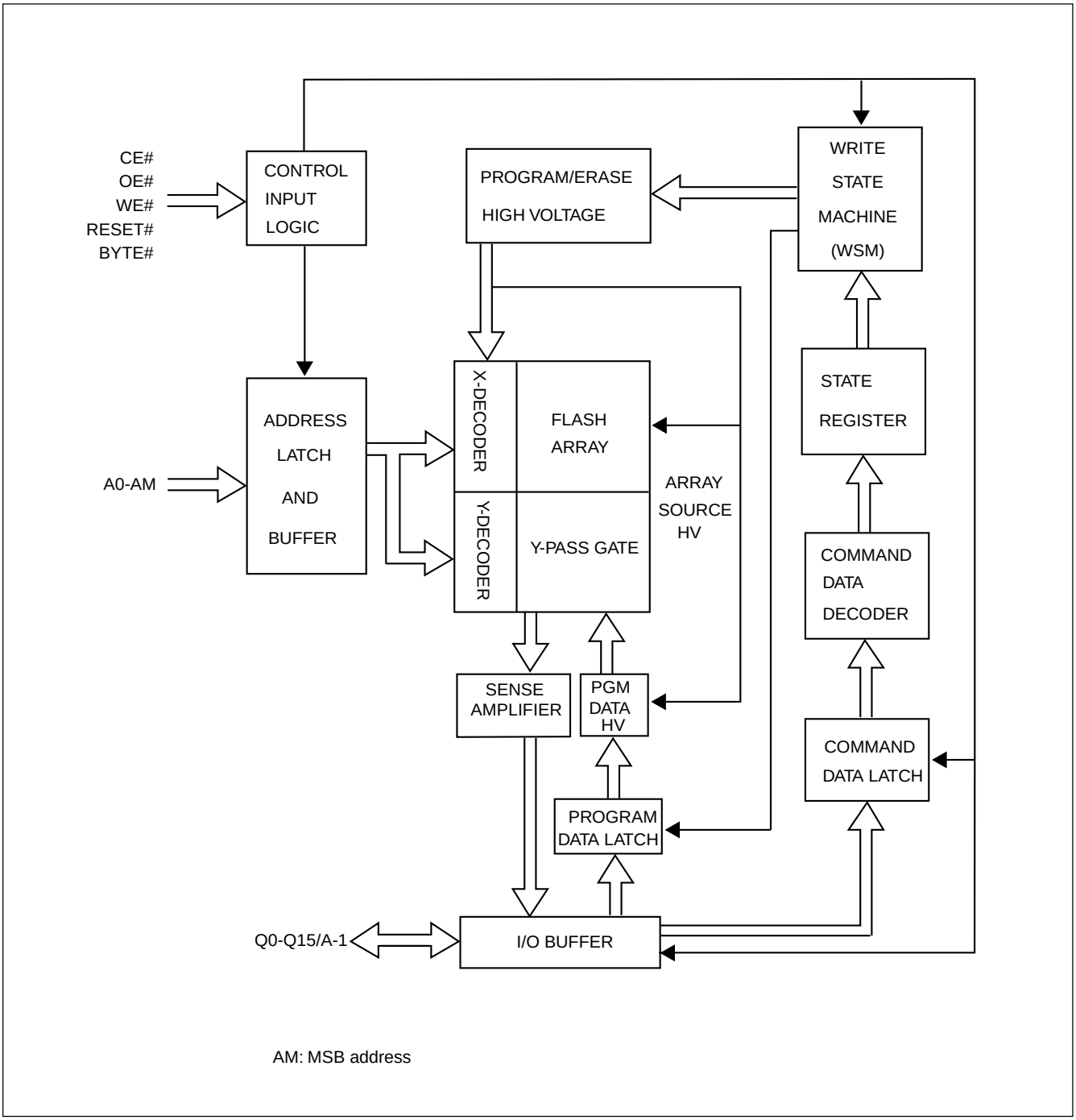


Table 1. BLOCK STRUCTURE

MX29SL400CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000h-0FFFFh	00000h-07FFFh	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	1	1	0	X	X	X
SA7	32Kbytes	16Kwords	70000h-77FFFh	38000h-3BFFFh	1	1	1	0	X	X
SA8	8Kbytes	4Kwords	78000h-79FFFh	3C000h-3CFFFh	1	1	1	1	0	0
SA9	8Kbytes	4Kwords	7A000h-7BFFFh	3D000h-3DFFFh	1	1	1	1	0	1
SA10	16Kbytes	8Kwords	7C000h-7FFFFh	3E000h-3FFFFh	1	1	1	1	1	X

MX29SL400CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	04000h-05FFFh	02000h-02FFFh	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	06000h-07FFFh	03000h-03FFFh	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	08000h-0FFFFh	04000h-07FFFh	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	1	1	1	X	X	X

Table 2. BUS OPERATION

DESCRIPTION	CE#	OE#	WE#	RESET#	ADDRESS								Q0~Q7	Q8~Q15		
					A17 | A12	A11 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0		BYTE# =Vih	BYTE#=Vil	
																Q8~Q14	Q15/A-1
Read	L	L	H	H	AIN									Dout	Dout	Q8~Q14 =High Z	A-1
Write	L	H	L	H	AIN									DIN	DIN		
Reset	X	X	X	L	X									High Z	High Z	High Z	X
Temporary sector Unprotection	X	X	X	Vhv	AIN									DIN	DIN	High Z	X
Output Disable	L	H	H	H	X									High Z	High Z	High Z	X
Standby	VCC± 0.3V	X	X	VCC± 0.3V	X									High Z	High Z	High Z	X
Sector Protect	L	H	L	Vhv	SA	X	X	X	L	X	H	L		DIN	X	X	L
Chip Unprotected	L	H	L	Vhv	X	X	X	X	H	X	H	L		DIN	X	X	X
Sector Protection Verify	L	L	H	H	SA	X	Vhv	X	L	X	H	L		CODE(4)	X	X	L

Notes:

1. Vhv is the very high voltage, 10V to 11V.
2. X means input high (Vih) or input low (Vil).
3. SA means sector address: A12~A17.
4. Code=00H/XX00H means unprotected.
   Code=01H/XX01H means protected.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array out. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready1 for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on these sectors. MX29SL400C T/B provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29SL400C T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29SL400C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires V_{hv} on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A17 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is still not being protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29SL400C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29SL400C T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select						Program	
				Silicon ID		Device ID		Sector Protect Verify			
	Hex			Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cyc	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cyc	Addr			2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55
3rd Bus Cyc	Addr			555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	A0	A0
4th Bus Cyc	Addr			X00	X00	X01	X02	(Sector) X02	(Sector) X04	Addr	Addr
	Data			C2H	C2H	ID	ID	00/01	00/01	Data	Data
5th Bus Cyc	Addr										
	Data										
6th Bus Cyc	Addr										
	Data										

Command		Chip Erase		Sector Erase		CFI Read		Erase Suspend	Erase Resume
	Hex	Word	Byte	Word	Byte	Word	Byte	Word/Byte	Word/Byte
1st Bus Cyc	Addr	555	AAA	555	AAA	55	AA	XXX	XXX
	Data	AA	AA	AA	AA	98	98	B0	30
2nd Bus Cyc	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
3rd Bus Cyc	Addr	555	AAA	555	AAA				
	Data	80	80	80	80				
4th Bus Cyc	Addr	555	AAA	555	AAA				
	Data	AA	AA	AA	AA				
5th Bus Cyc	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
6th Bus Cyc	Addr	555	AAA	Sector	Sector				
	Data	10	10	30	30				

Notes:
1. Device ID: 2270H/70H for Top Boot Sector device.
   22F1H/F1H for Bottom Boot Sector device.
2. For sector protect verify result, XX00H/00H means sector is not protected, XX01H/01H means sector has been protected.
3. Sector Protect command is valid during Vhv at RESET# pin, Vih at A1 pin and Vil at A0, A6 pins. The last Bus cyc is for protect verify.
4. It is not allowed to adopt any other code which is not in the above command definition table.

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in program mode (not program fail) or erase mode (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

		Address	Data (Hex)	Representation
Manufacturer ID	Word	X00	00C2	
	Byte	X00	C2	
Device ID	Word	X01	2270/22F1	Top/Bottom Boot Sector
	Byte	X02	70/F1	Top/Bottom Boot Sector
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected
	Byte	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 3, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29SL400C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

With the internal write state controller, the device requires the user to write the program command and data only. The typical chip program time at room temperature of the MX29SL400C T/B is 4.8 seconds. (Word-Mode)

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware rests or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Toggling	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1(<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	1	0	0	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	0	1	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 10ms interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29SL400C T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/ "AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

TABLE 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Address (Word Mode)	Data
Query-unique ASCII string "QRY"	20	10	0051
	22	11	0052
	24	12	0059
Primary vendor command set and control interface ID code	26	13	0002
	28	14	0000
Address for primary algorithm extended query table	2A	15	0040
	2C	16	0000
Alternate vendor command set and control interface ID code (none)	2E	17	0000
	30	18	0000
Address for secondary algorithm extended query table (none)	32	19	0000
	34	1A	0000

TABLE 4-2. CFI Mode: System Interface Data Values
(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Address (Word Mode)	Data
VCC supply, minimum (1.65V)	36	1B	0016
VCC supply, maximum (2.2V)	38	1C	0022
VPP supply, minimum (none)	3A	1D	0000
VPP supply, maximum (none)	3C	1E	0000
Typical timeout for single word/byte write (2^N us)	3E	1F	0004
Typical timeout for Minimum size buffer write (2^N us)	40	20	0000
Typical timeout for individual block erase (2^N ms)	42	21	000A
Typical timeout for full chip erase (2^N ms)	44	22	0000
Maximum timeout for single word/byte write times (2^N X Typ)	46	23	0005
Maximum timeout for buffer write times (2^N X Typ)	48	24	0000
Maximum timeout for individual block erase times (2^N X Typ)	4A	25	0004
Maximum timeout for full chip erase times (not supported)	4C	26	0000

TABLE 4-3. CFI Mode: Device Geometry Data Values
(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Address (Word Mode)	Data
Device size (2^N bytes)	4E	27	0013
Flash device interface code (refer to the CFI publication 100)	50	28	0002
	52	29	0000
Maximum number of bytes in multi-byte write (not supported)	54	2A	0000
	56	2B	0000
Number of erase block regions	58	2C	0004
Index for Erase Bank Area 1 (refer to the CFI publication 100)	5A	2D	0000
	5C	2E	0000
	5E	2F	0040
	60	30	0000
Index for Erase Bank Area 2	62	31	0001
	64	32	0000
	66	33	0020
	68	34	0000
Index for Erase Bank Area 3	6A	35	0000
	6C	36	0000
	6E	37	0080
	70	38	0000
Index for Erase Bank Area 4	72	39	0006
	74	3A	0000
	76	3B	0000
	78	3C	0001

TABLE 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values
(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Address (Word Mode)	Data
Query - Primary extended table, unique ASCII string, PRI	80	40	0050
	82	41	0052
	84	42	0049
Major version number, ASCII	86	43	0031
Minor version number, ASCII	88	44	0030
Unlock recognizes address (0= recognize, 1= don't recognize)	8A	45	0000
Erase suspend (2= to both read and program)	8C	46	0002
Sector protect (N= # of sectors/group)	8E	47	0001
Temporary sector unprotected (1=supported)	90	48	0001
Sector protect/unprotected scheme	92	49	0004
Simultaneous R/W operation (0=not supported)	94	4A	0000
Burst mode (0=not supported)	96	4B	0000
Page mode (0=not supported)	98	4C	0000

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . -0.5V to +3.0 V
RESET#, A9 and OE# . . . . . -0.3V to +11.5 V
The other pins. . . . . -0.3V to Vcc +0.5 V
Output Short Circuit Current (less than one second) . . . . . 200 mA

OPERATING TEMPERATURE AND VOLTAGE

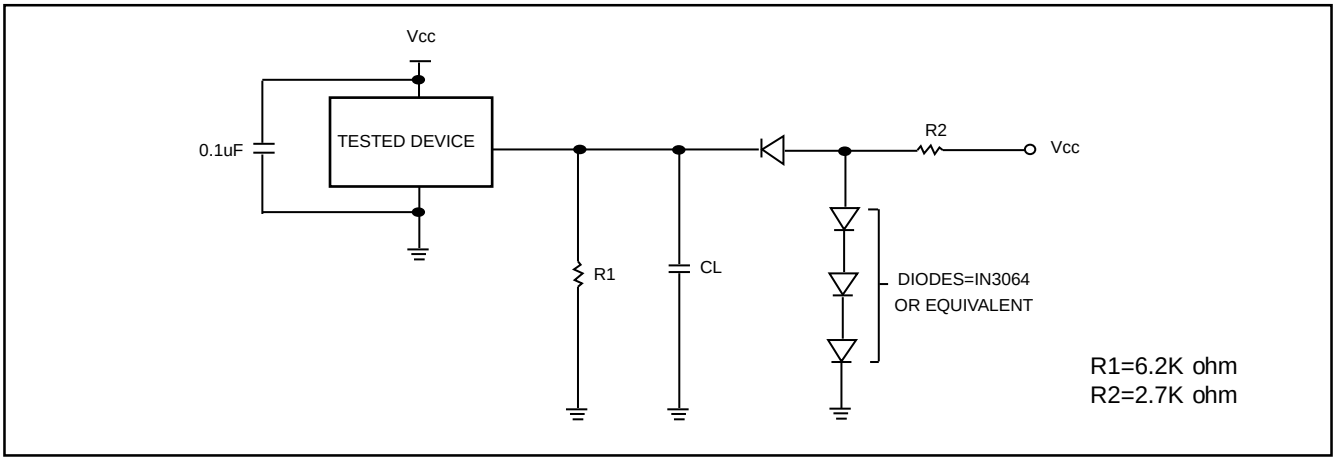
Commercial (C) Grade
Surrounding Temperature (T_A). . . . . 0° C to +70° C
Industrial (I) Grade
Surrounding Temperature (T_A). . . . . -40° C to +85° C
V_{CC} Supply Voltages
V_{CC} range. . . . . +1.65V to 2.2V

DC CHARACTERISTICS

Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			±1.0uA	
Iilk9	A9, OE#, RESET# Input Leak			35uA	A9, OE#, RESET#=11V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current(10MHz)			12mA	CE#=Vil, OE#=Vih
Icr2	Read Current(5MHz)			6mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	25mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		1uA	5uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		1uA	5uA	Vcc=Vccmax, RESET# enable, other pin disable
Isbs	Sleep Mode Current		1uA	5uA	
Vil	Input Low Voltage	-0.5V		0.2 x Vcc	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/ Auto Select/Temporary Unprotect	10V	10.5V	11V	
Vol	Output Low Voltage			0.25V	Iol=2mA, Vcc=Vcc min
				0.1V	Iol=100uA, Vcc=Vcc min
Voh1	Ouput High Voltage (TTL)	0.85xVcc			IOH1=-2mA
Voh2	Ouput High Voltage (CMOS)	Vcc-0.4V			IOH2=-100uA

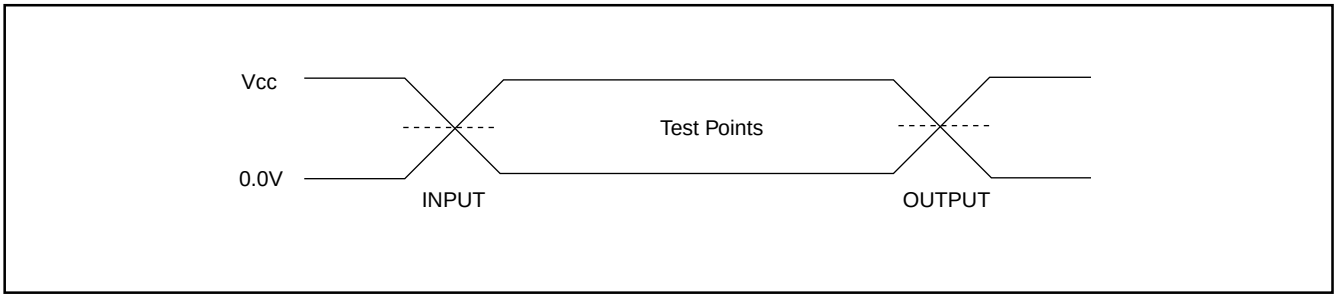
Notes:
When address is not changed and remain stable for Taa + 30nS, the device automatically enter Auto sleep Mode.

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF
Rise/Fall Times : 5ns
Input/Output reference levels :Vcc/2

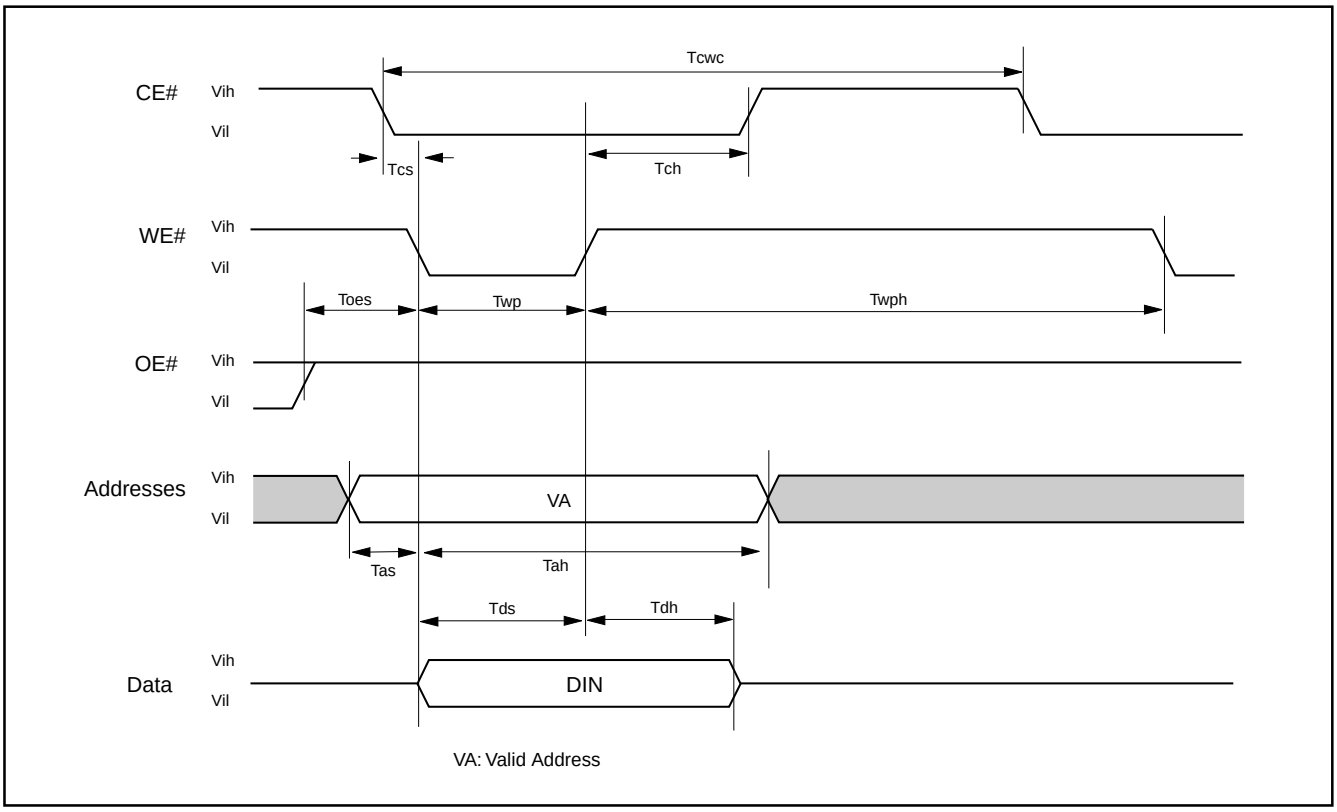
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

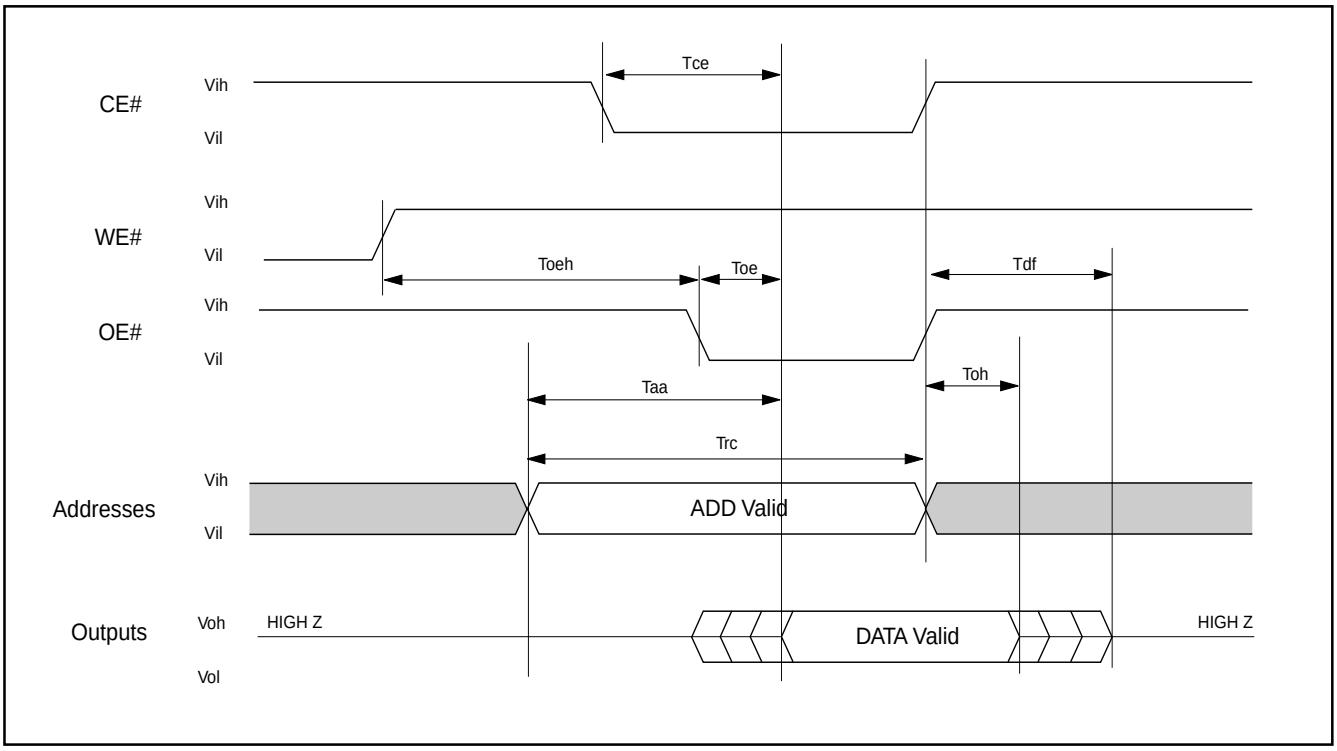
Symbol	Description		Min	Typ	Max	Unit
Taa	Valid data output after address				90	ns
Tce	Valid data output after CE# low				90	ns
Toe	Valid data output after OE# low				35	ns
Tdf	Data output floating after OE# high				30	ns
Toh	Data hold time after address rising		0			ns
Trc	Read period time		90			ns
Twc	Write period time		90			ns
Tcwc	Command write period time		90			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45			ns
Tds	Data setup time		45			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		50			us
Tcs	CE# Setup time		0			ns
Tch	CE# hold time		0			ns
Toes	OE# setup time		0			ns
Toeh	OE# hold time	Read	0			ns
Toeh		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		45			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		45			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation	Byte		12		us
Twhwh1	Program operation	Word		18		us
Twhwh2	Sector erase operation			1.3		sec
Tbal	Sector add load time				50	us

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

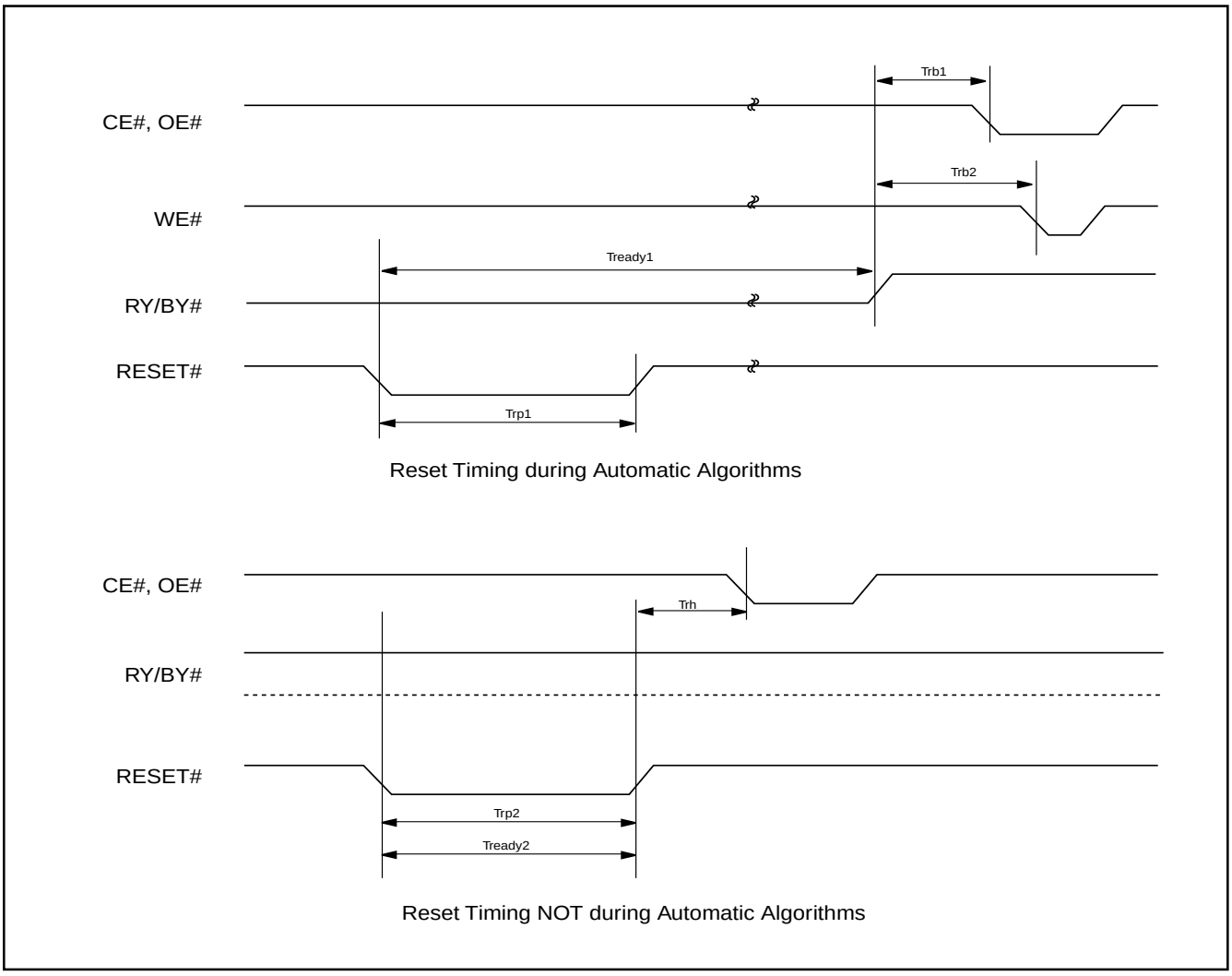
Figure 2. READ TIMING WAVEFORMS



AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	200	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

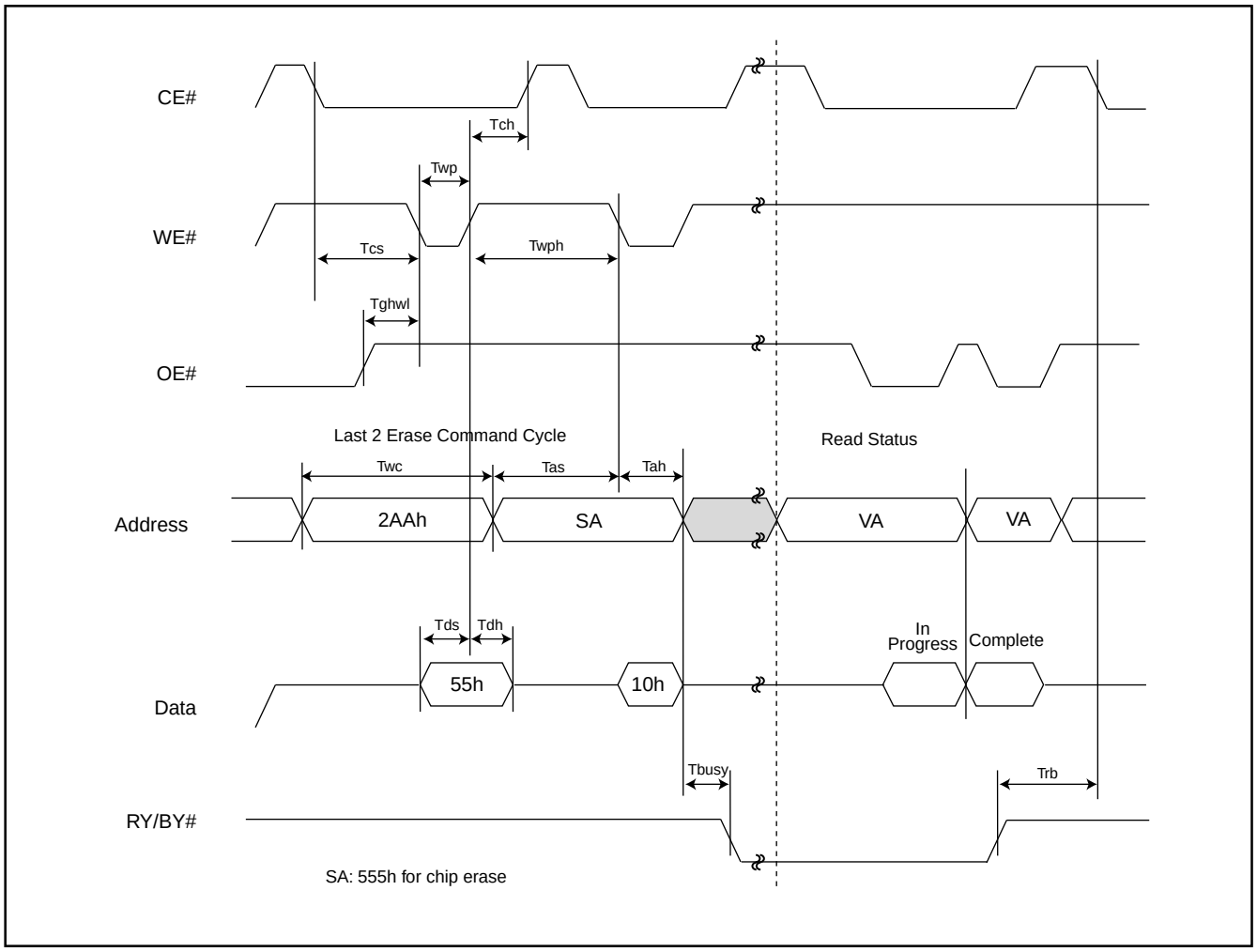


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

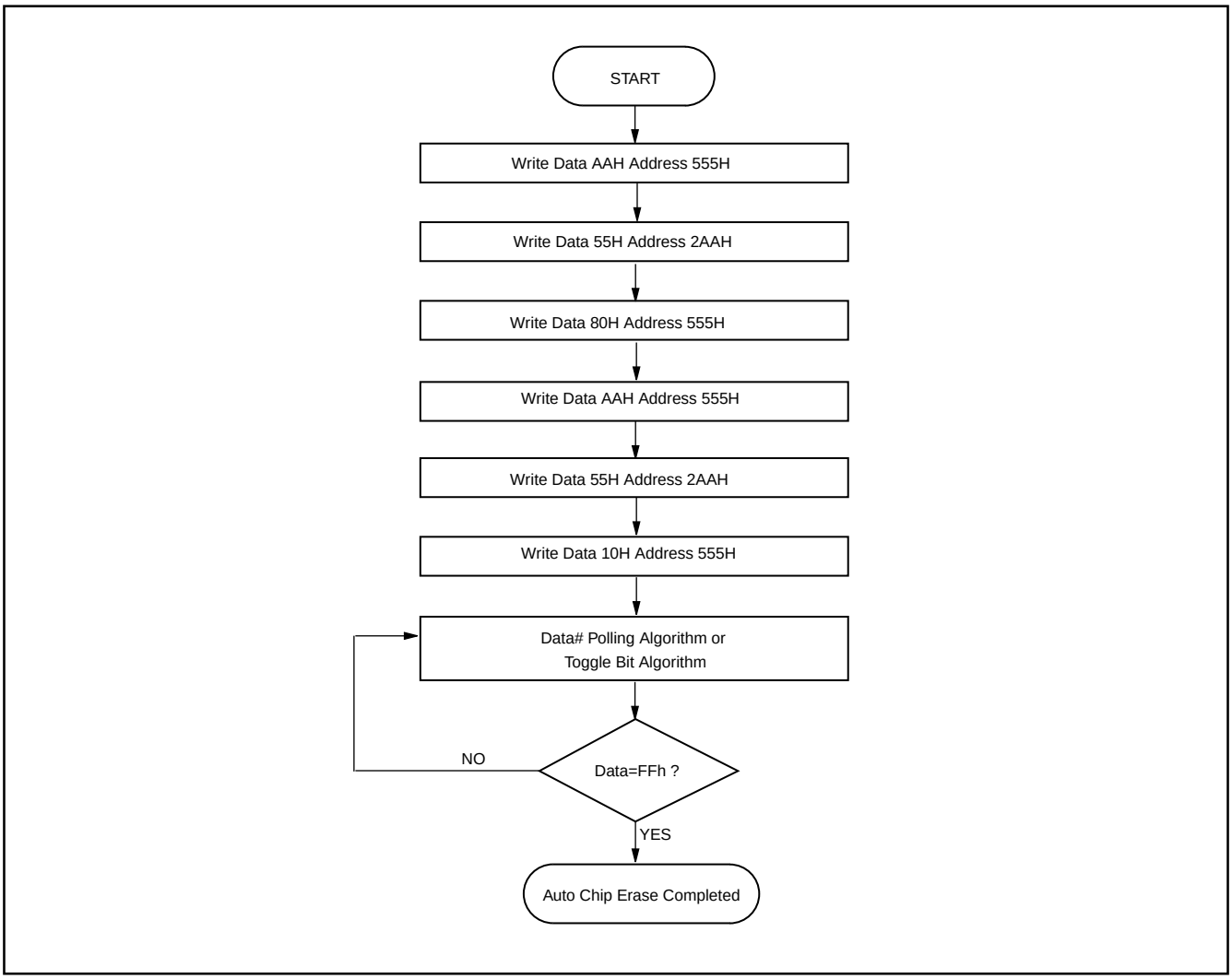


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

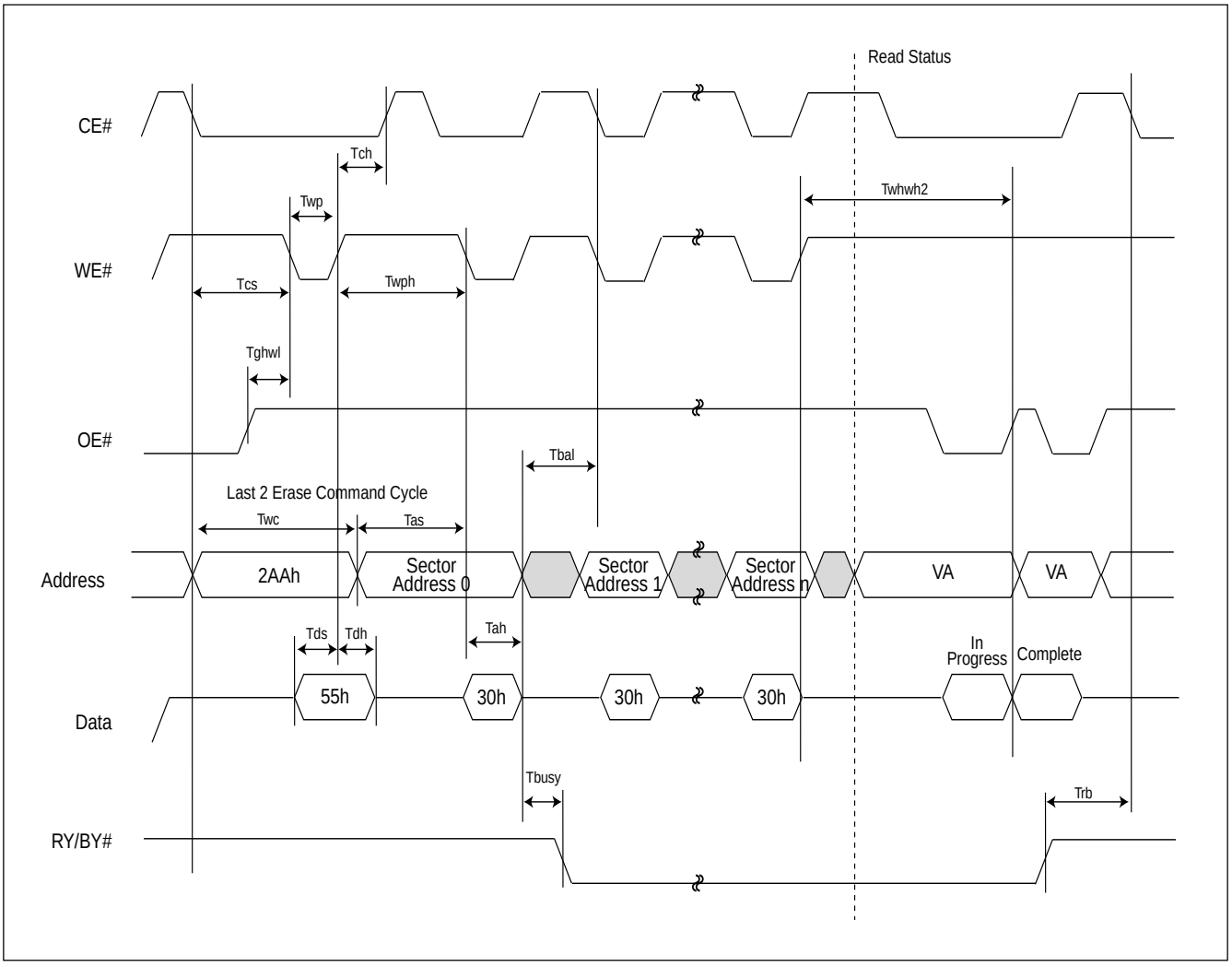


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

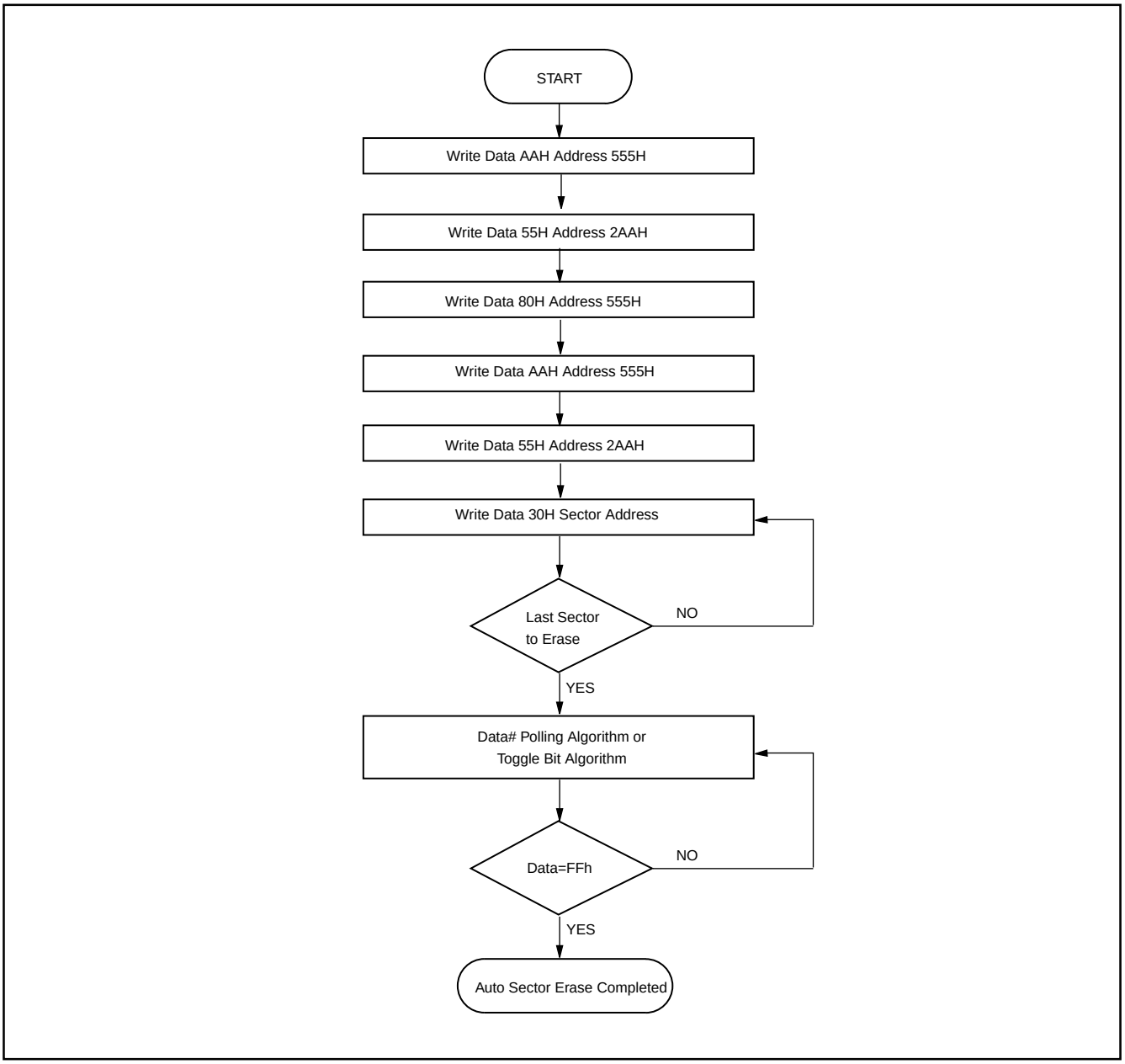


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

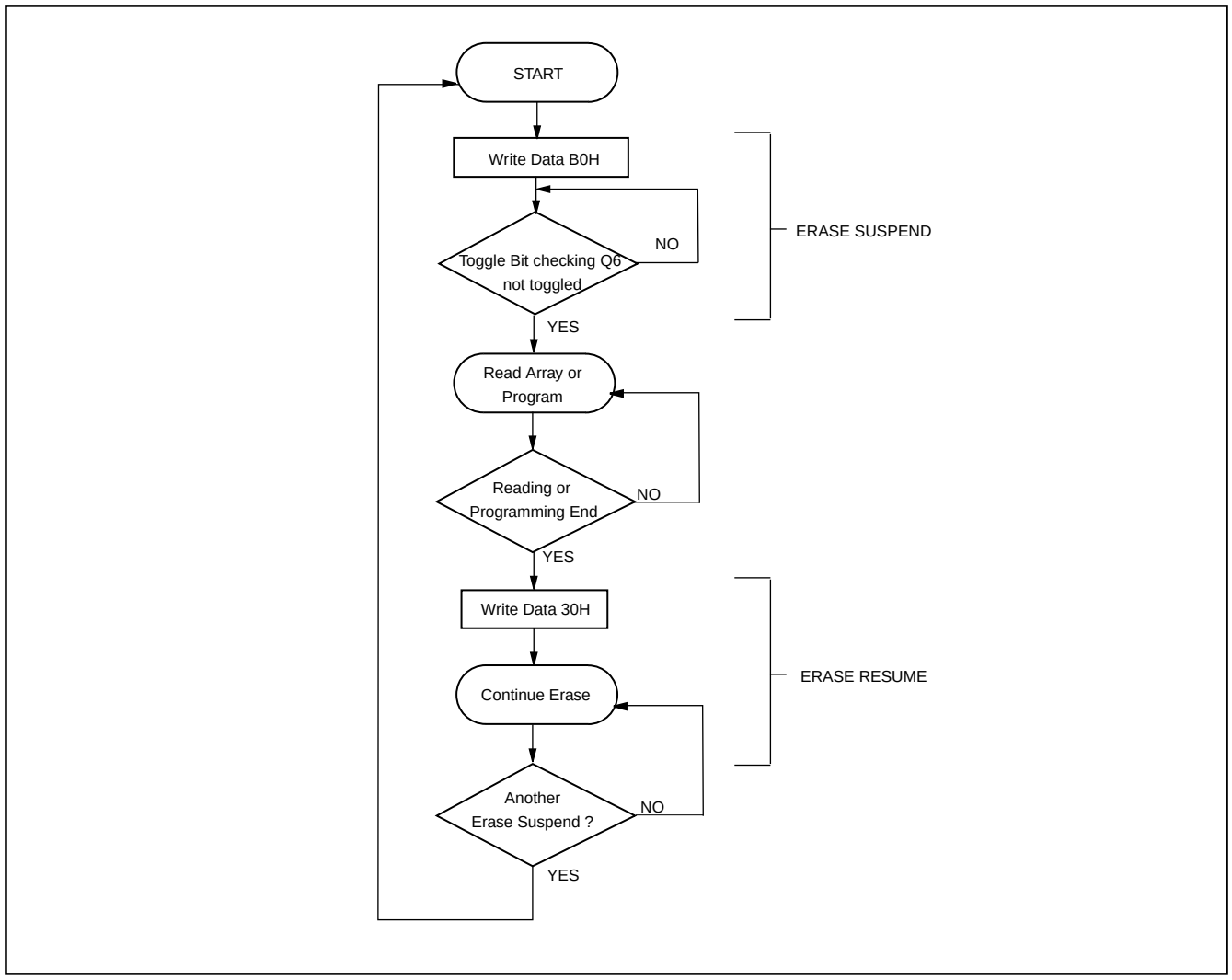


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

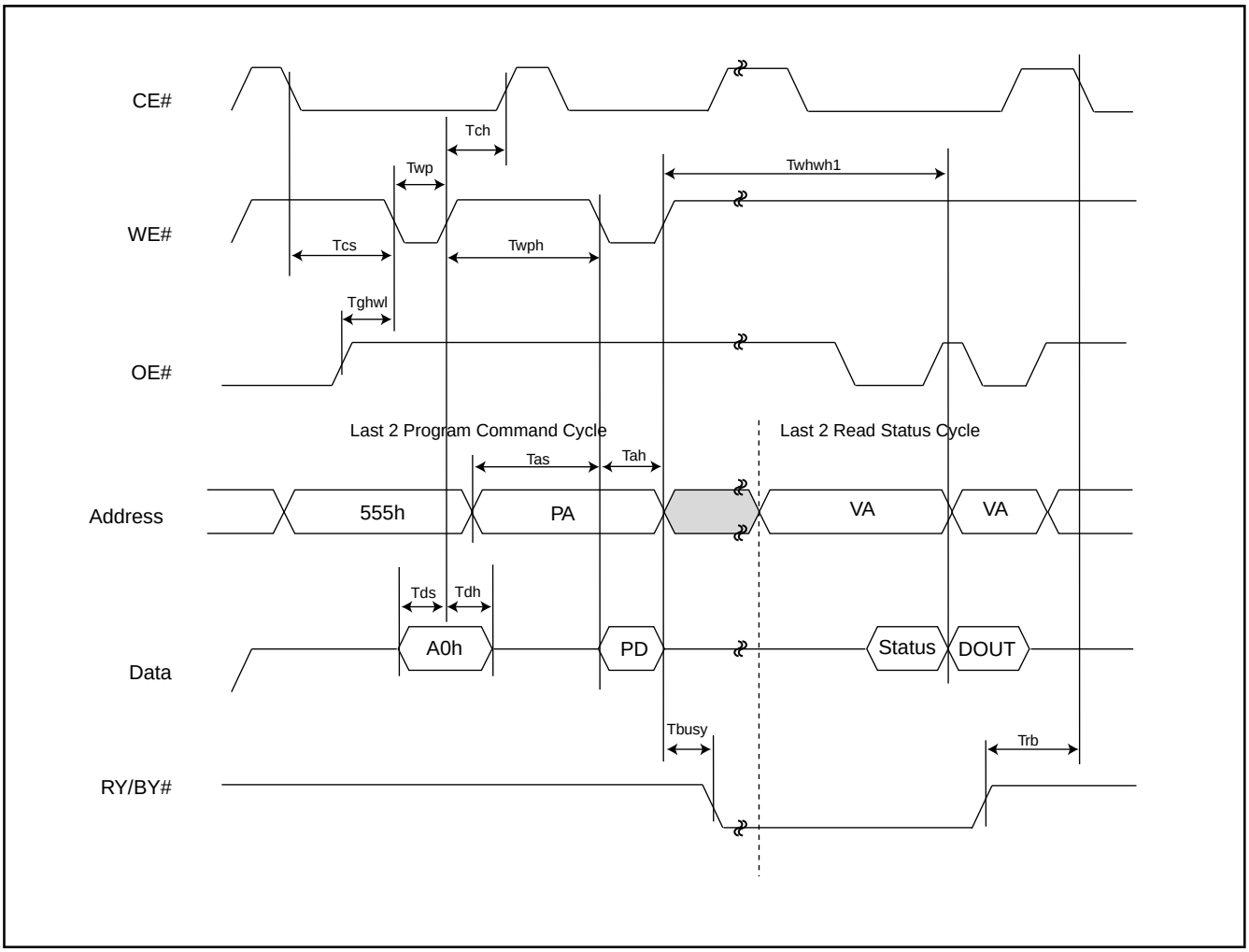


Figure 10. CE# CONTROLLED WRITE TIMING WAVEFORM

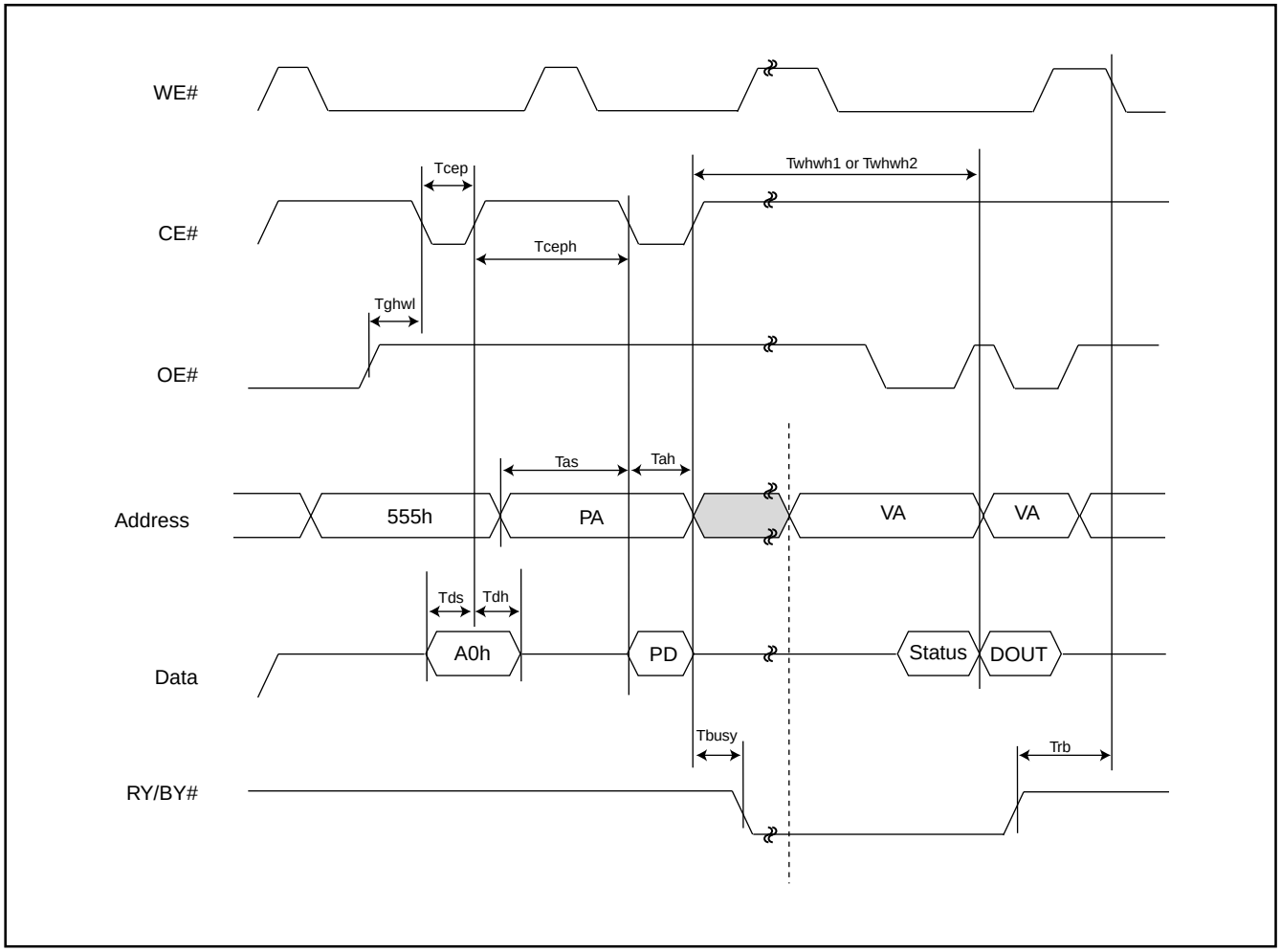
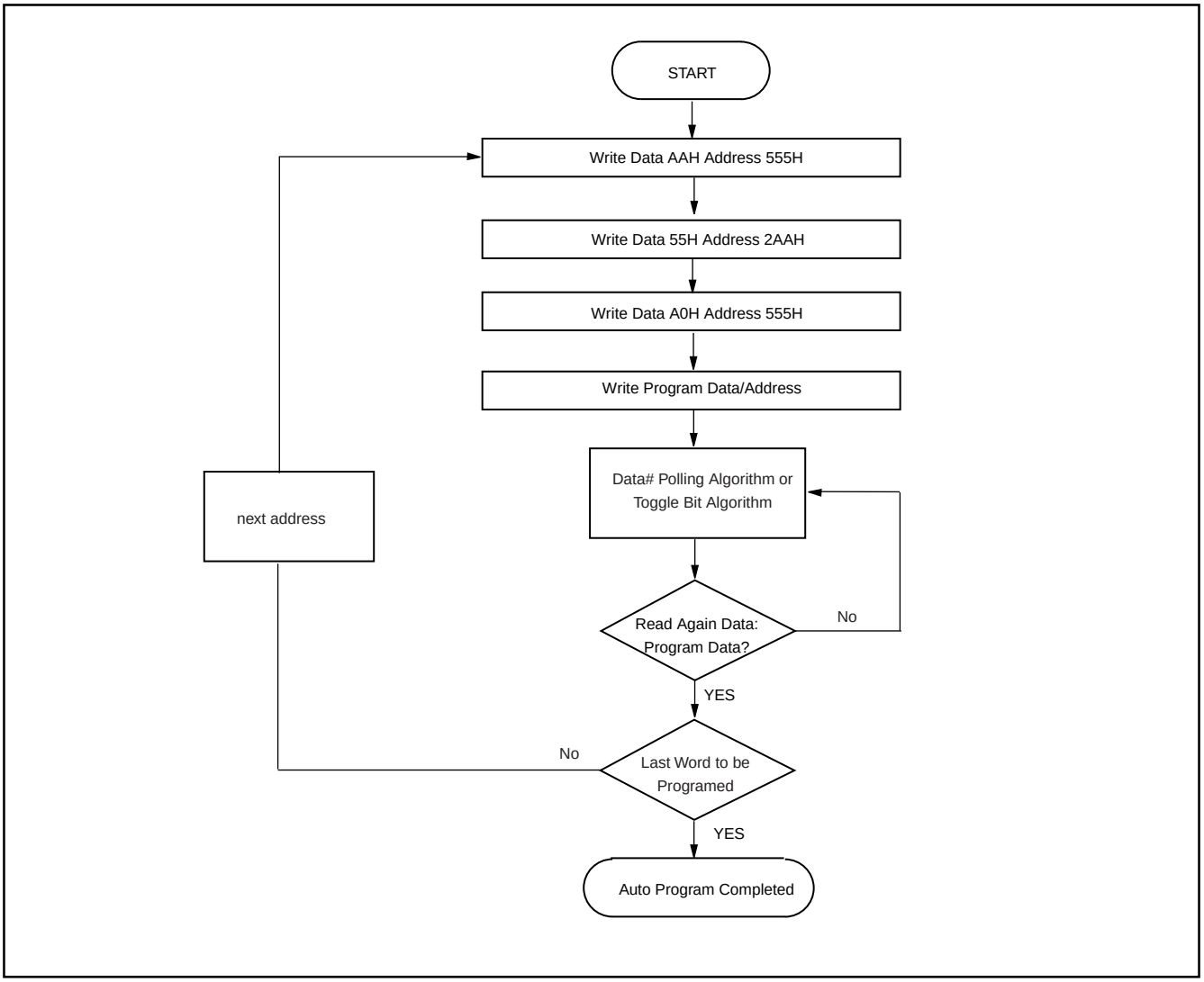


Figure 11. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR PROTECT/CHIP UNPROTECT

Figure 12. SECTOR PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)

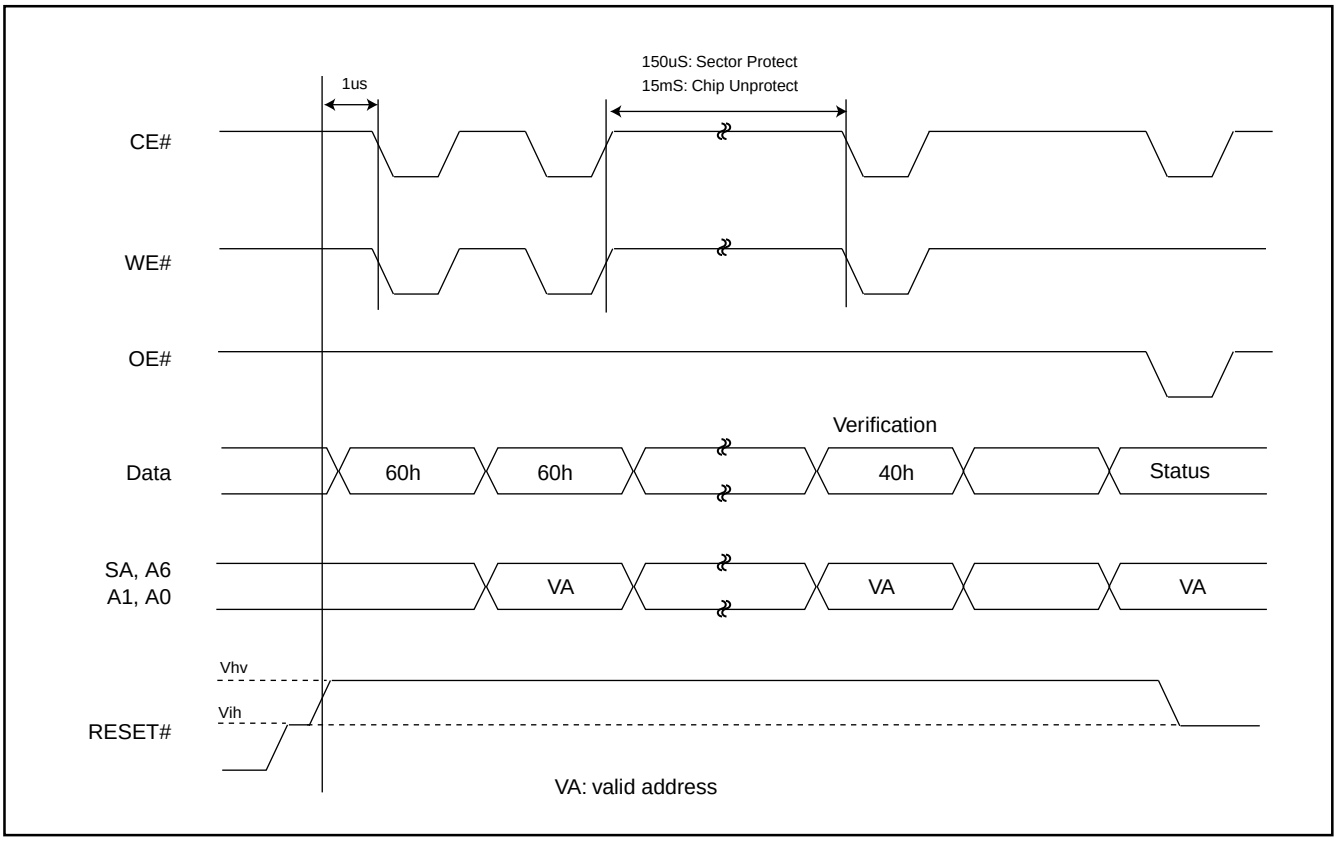


Figure 13-1. IN-SYSTEM SECTOR PROTECT WITH RESET#=Vhv

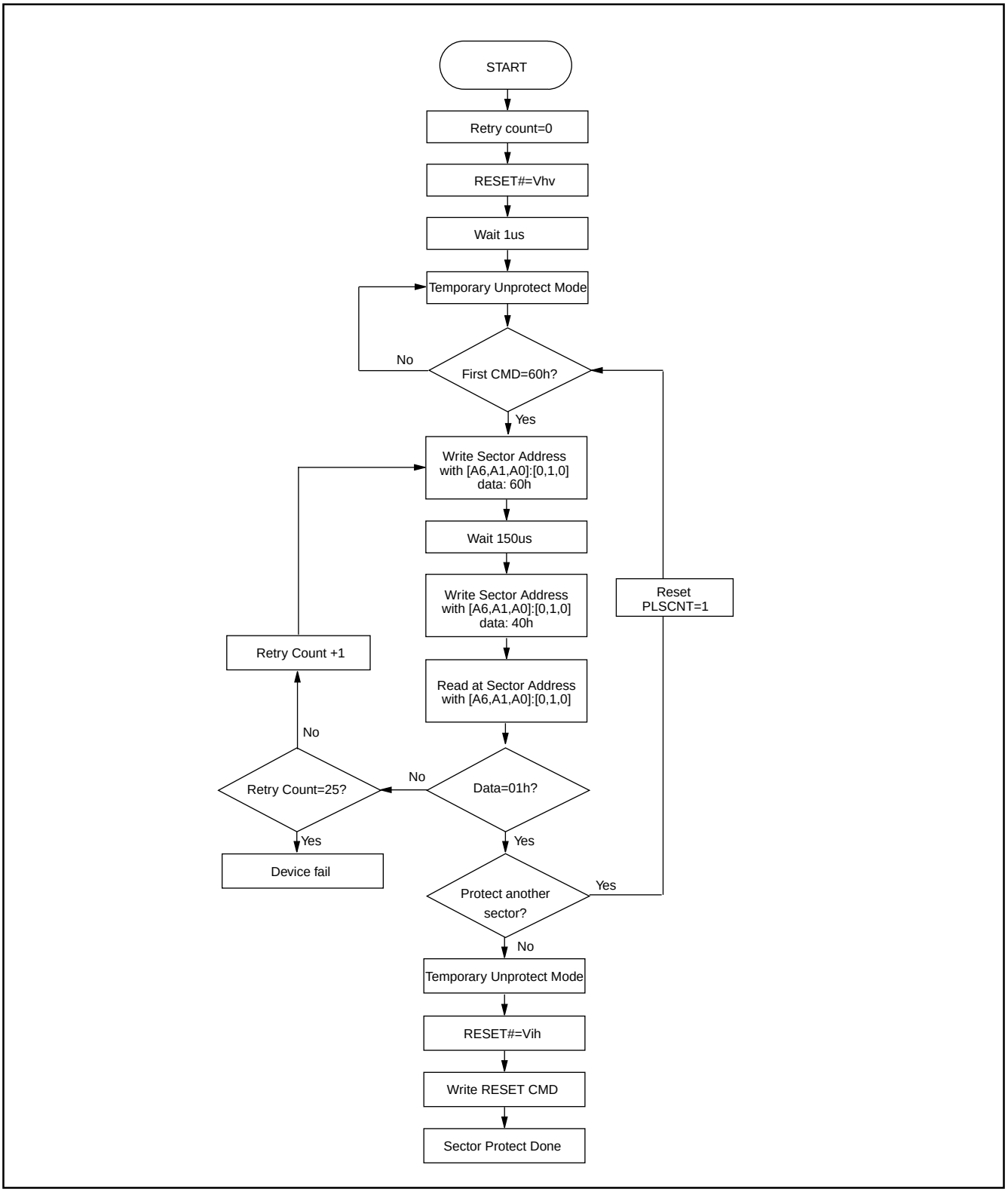


Figure 13-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

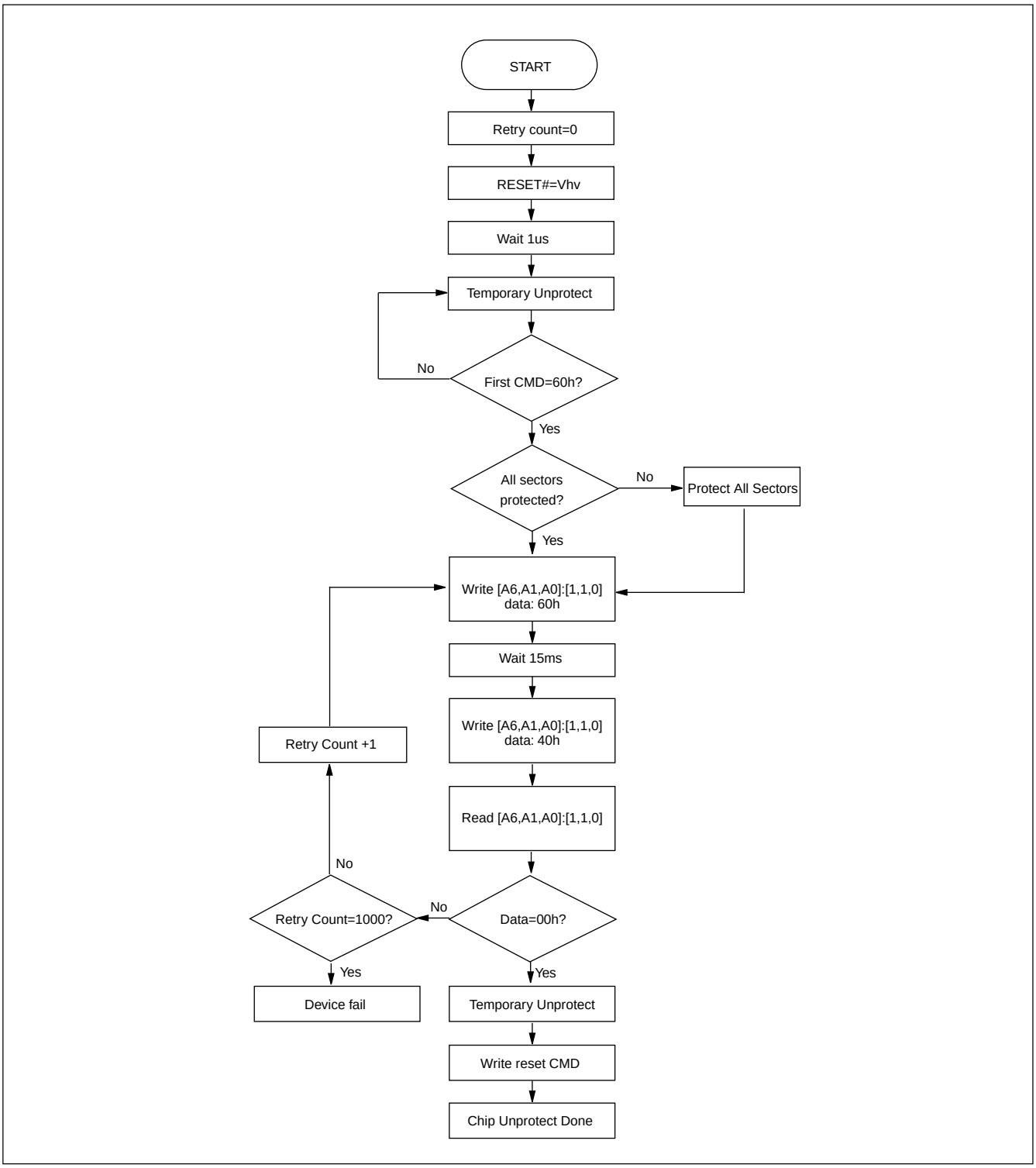
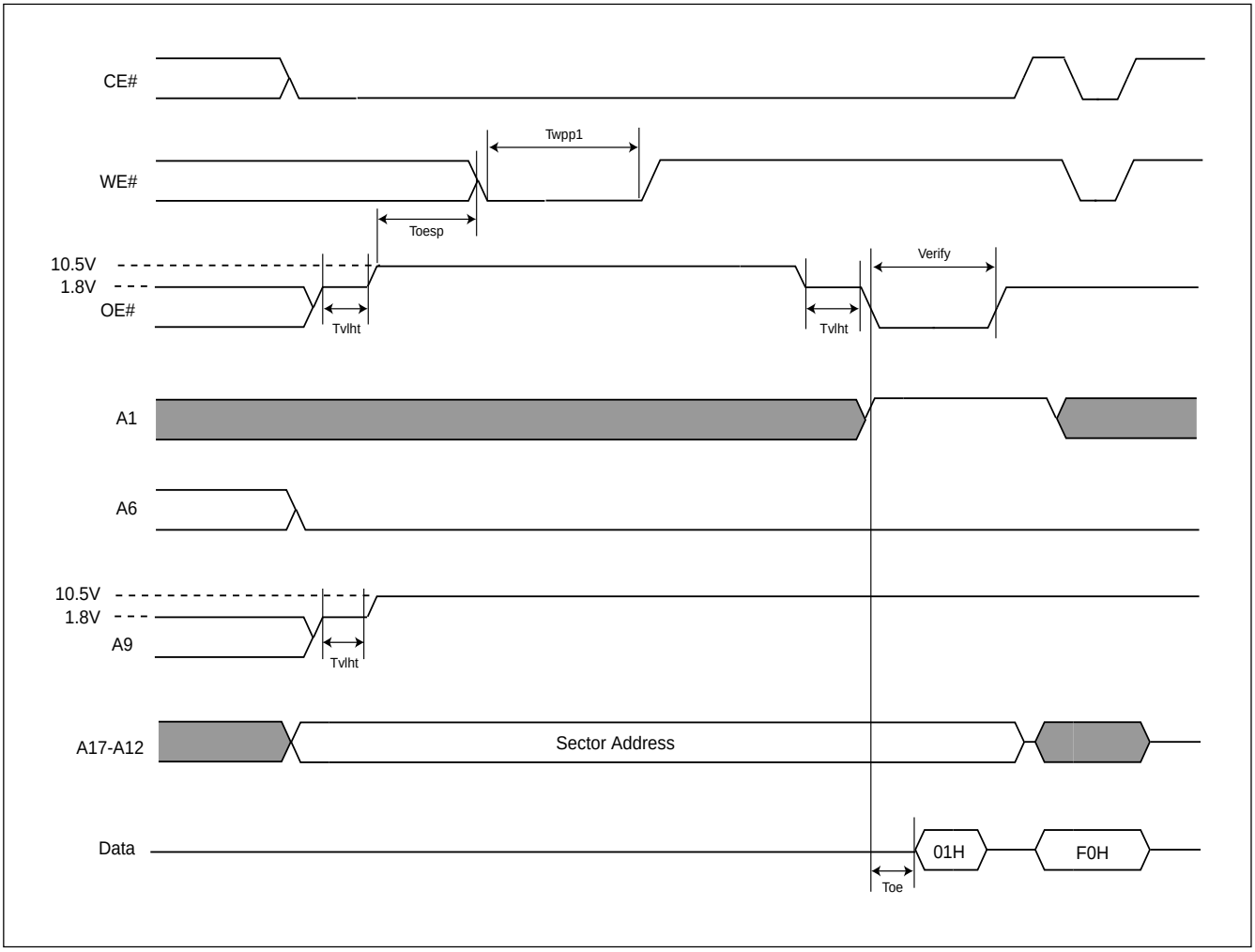


Figure 14. SECTOR PROTECT TIMING WAVEFORM (A9, OE# Control)



Notes: Tvlht (Voltage transition time)=4us min.
Twpp1 (Write pulse width for sector protect)=100ns min, 10us(Typ.)
Twpp2 (Write pulse width for chip unprotected)=100ns min, 12ms(Typ.)
Toesp (OE# setup time to WE# active)=4us min.

Figure 15. SECTOR PROTECTION ALGORITHM (A9, OE# Control)

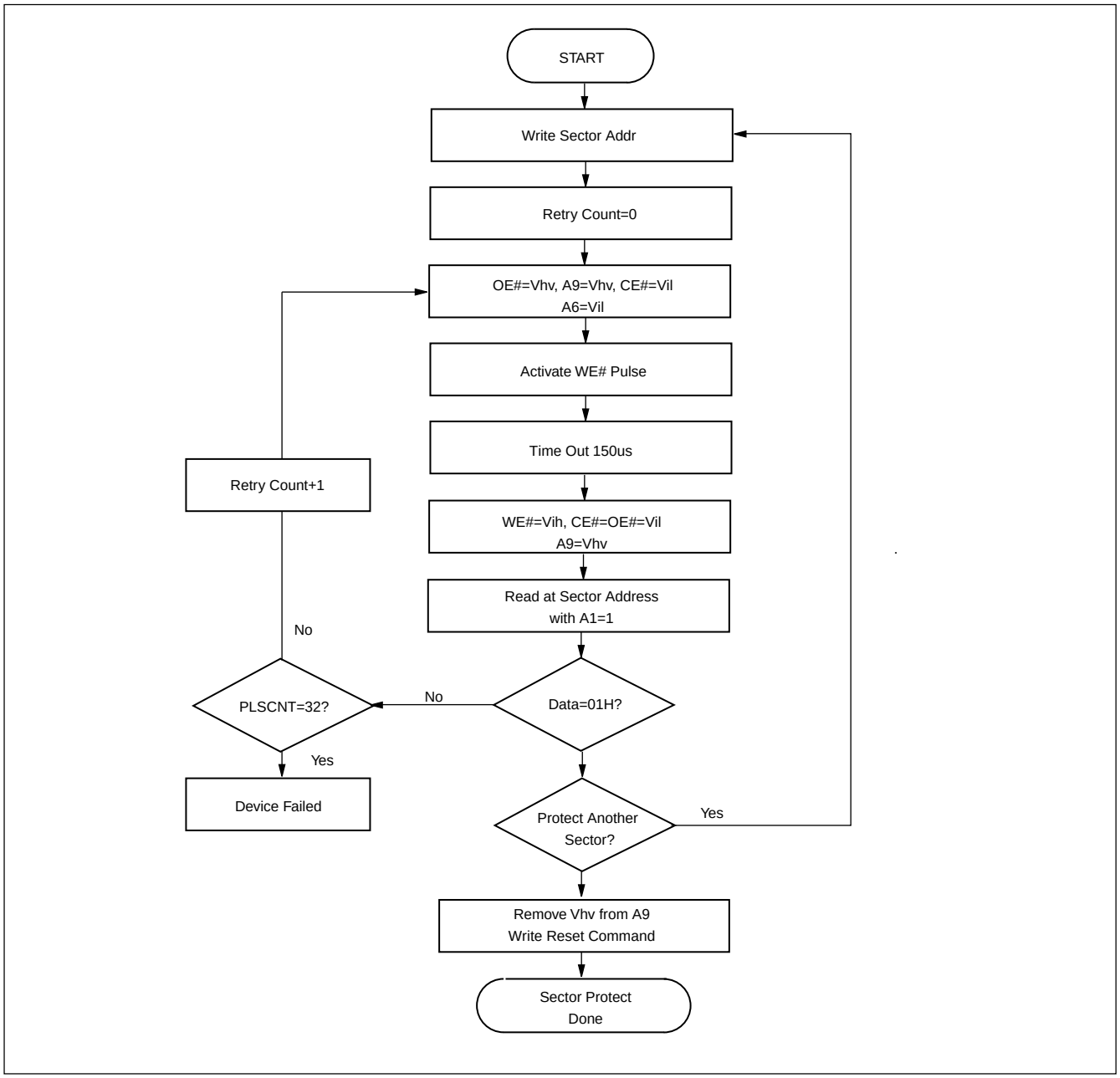
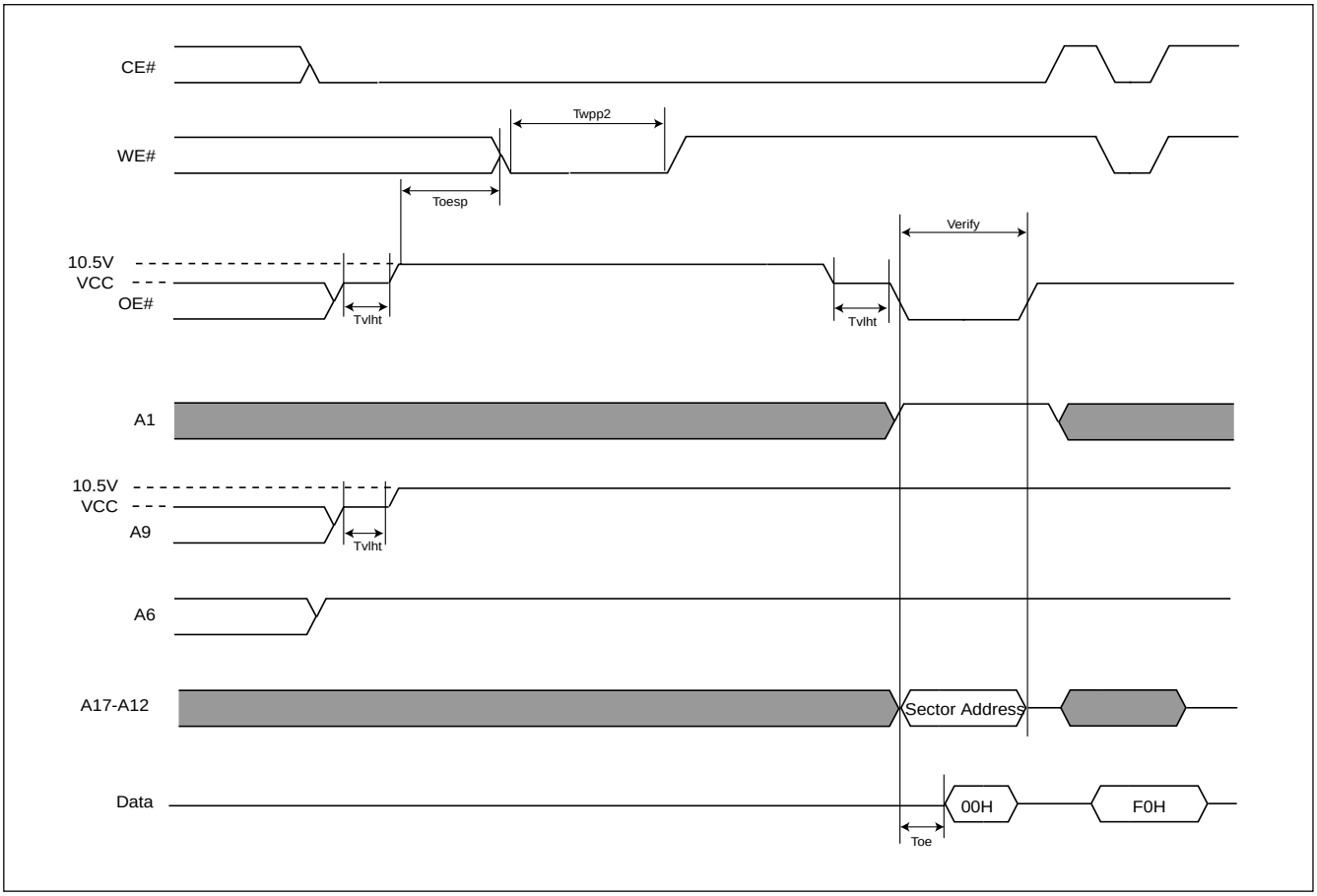


Figure 16. TIMING WAVEFORM FOR CHIP UNPROTECTION (A9, OE# Control)



Notes: Tvlht (Voltage transition time)=4us min.
Twpp1 (Write pulse width for sector protect)=100ns min, 10us(Typ.)
Twpp2 (Write pulse width for chip unprotected)=100ns min, 12ms(Typ.)
Toesp (OE# setup time to WE# active)=4us min.

Figure 17. CHIP UNPROTECTION ALGORITHM (A9, OE# Control)

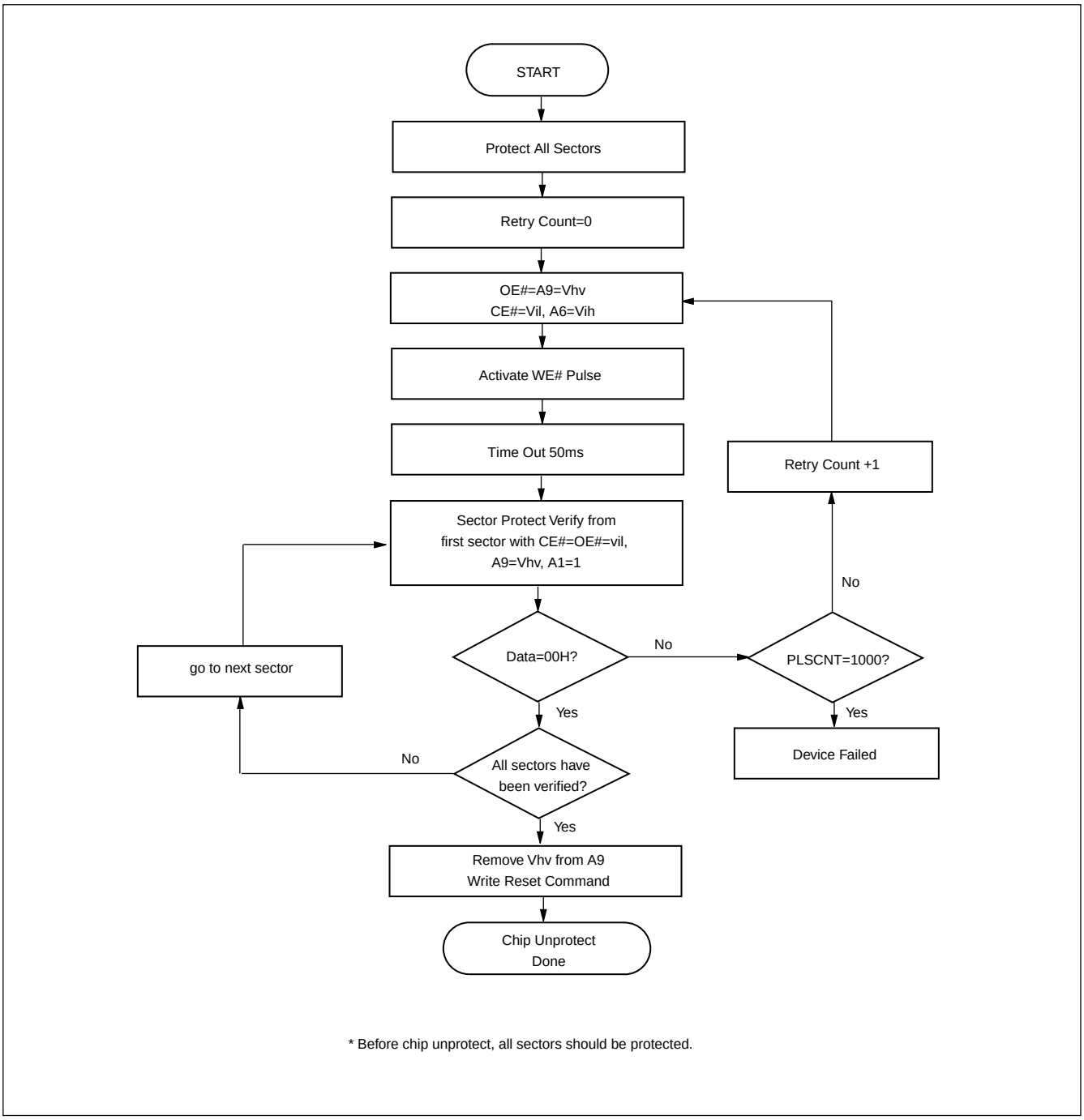


Table 5. TEMPORARY SECTOR UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 18. TEMPORARY SECTOR UNPROTECT WAVEFORMS

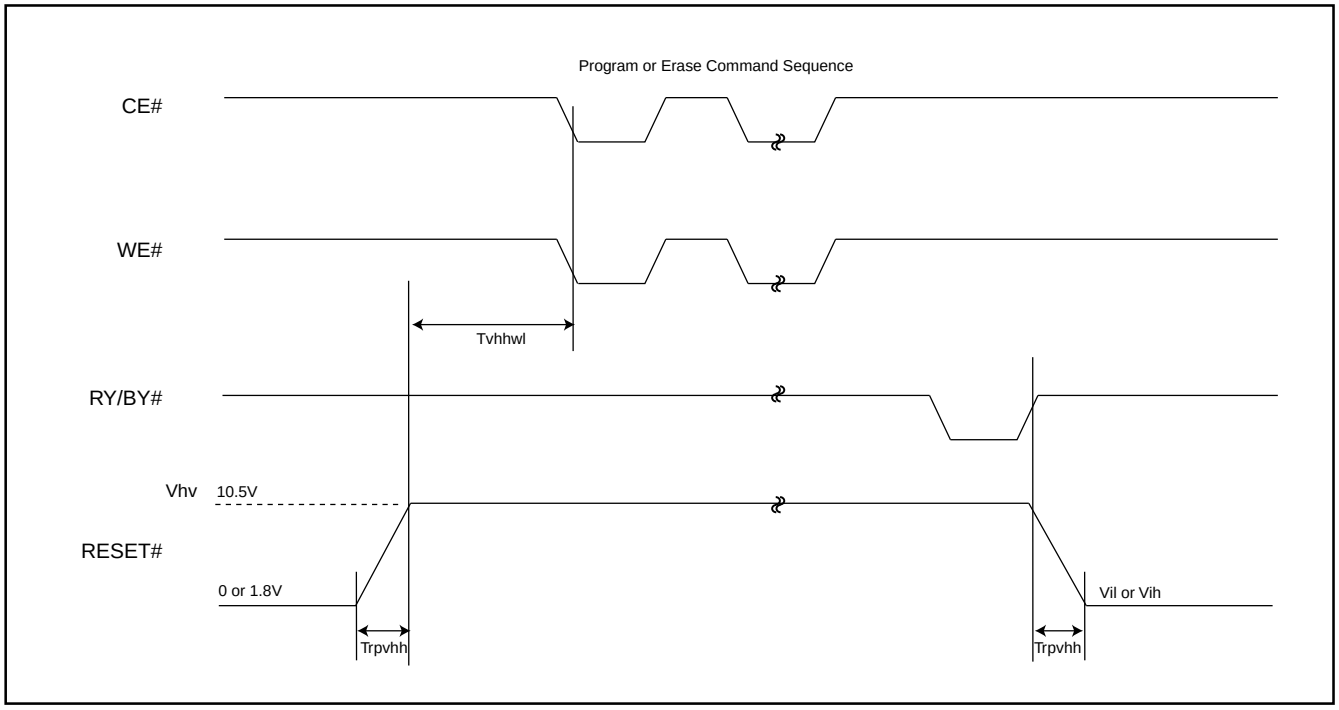
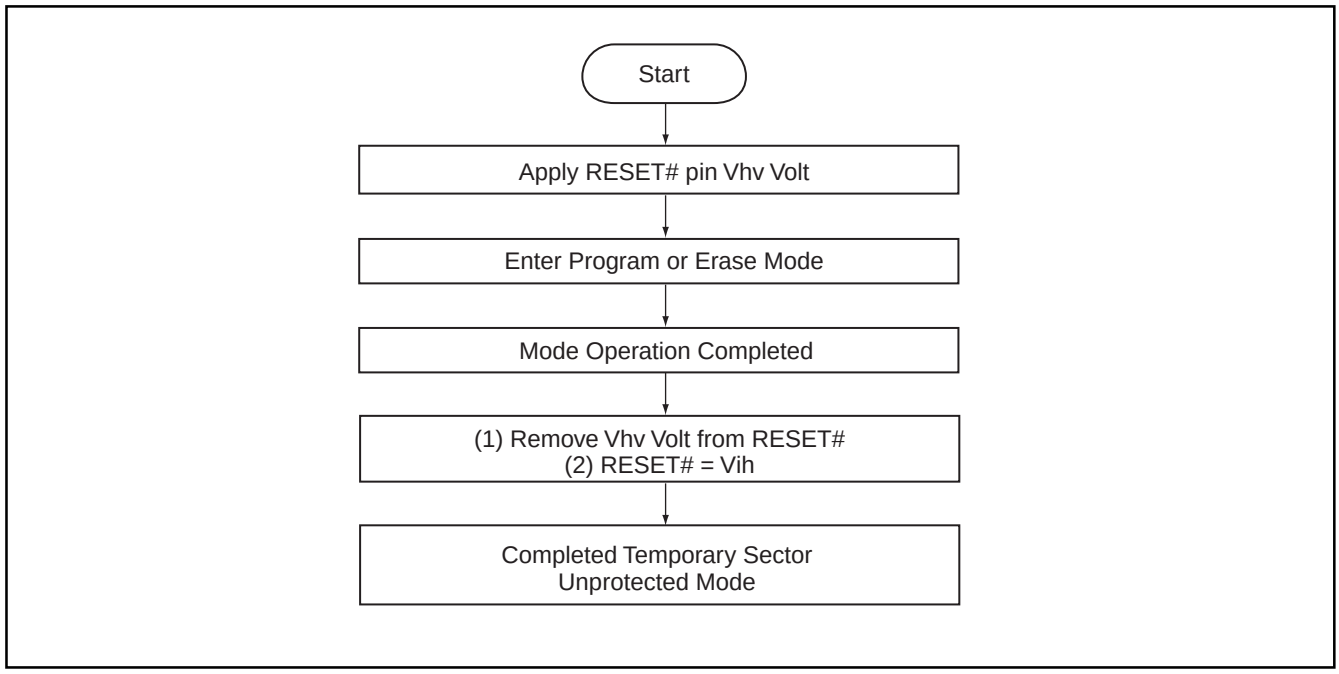
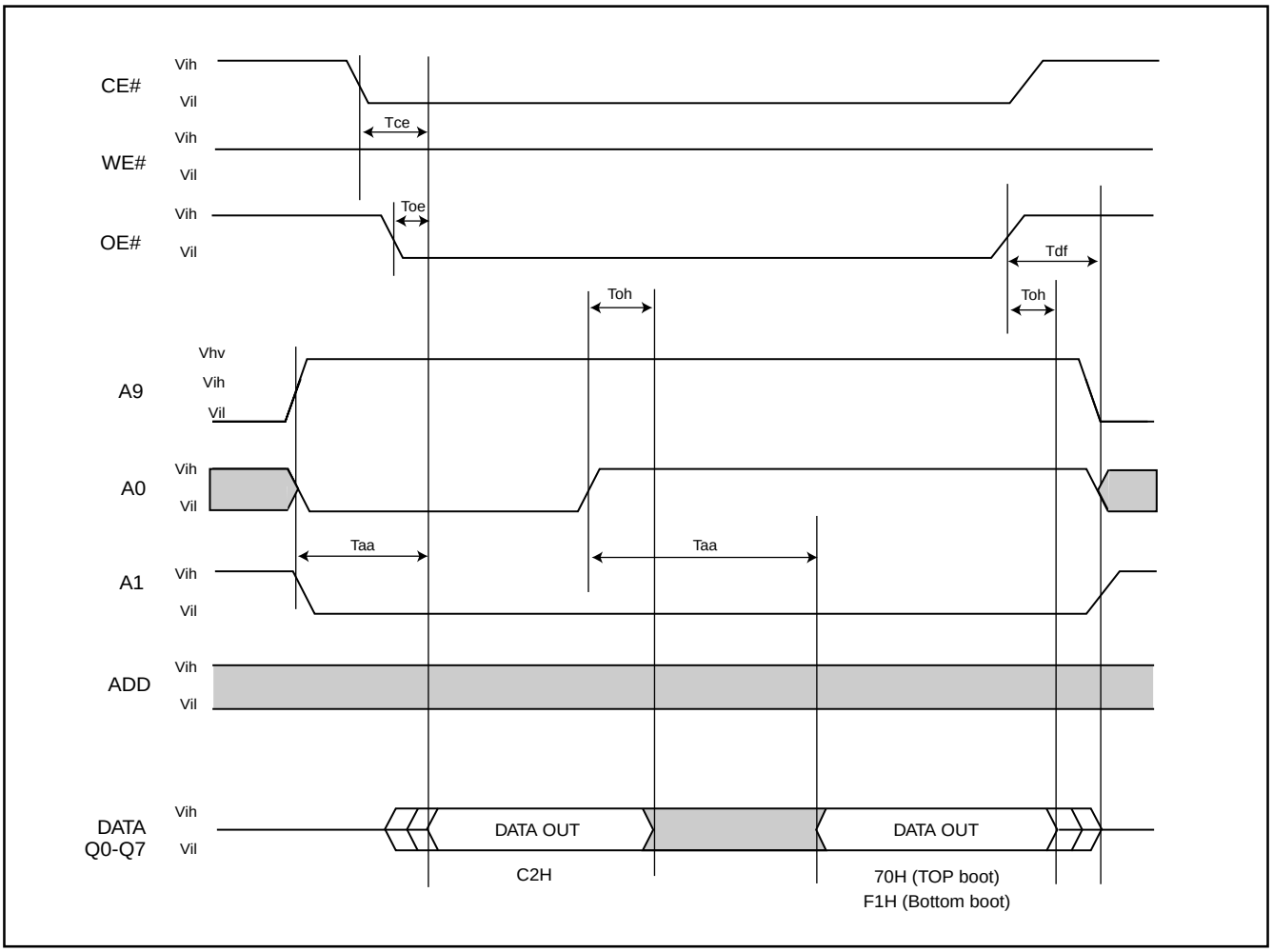


Figure 19. TEMPORARY SECTOR UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=10~11V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 20. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 21. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

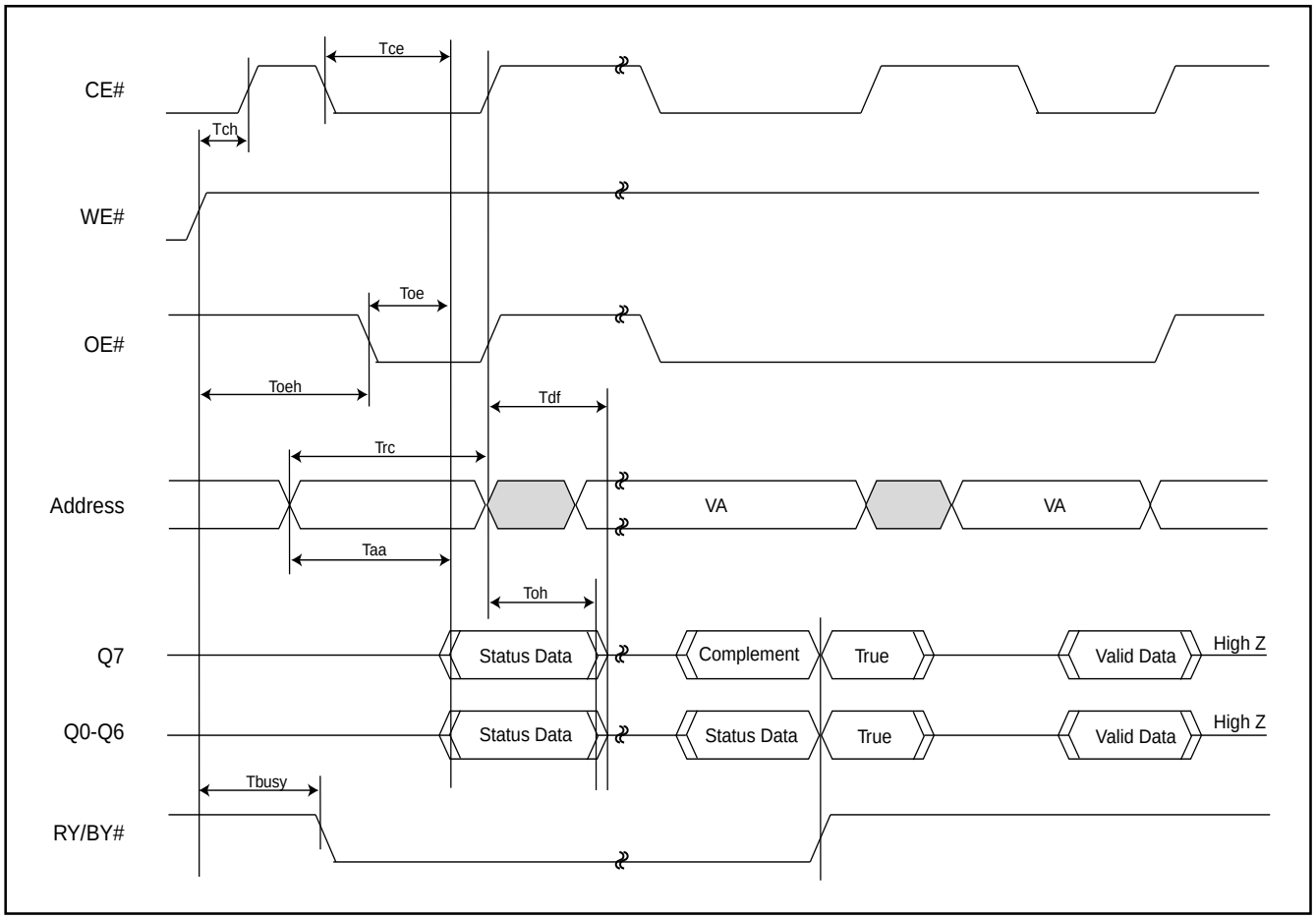
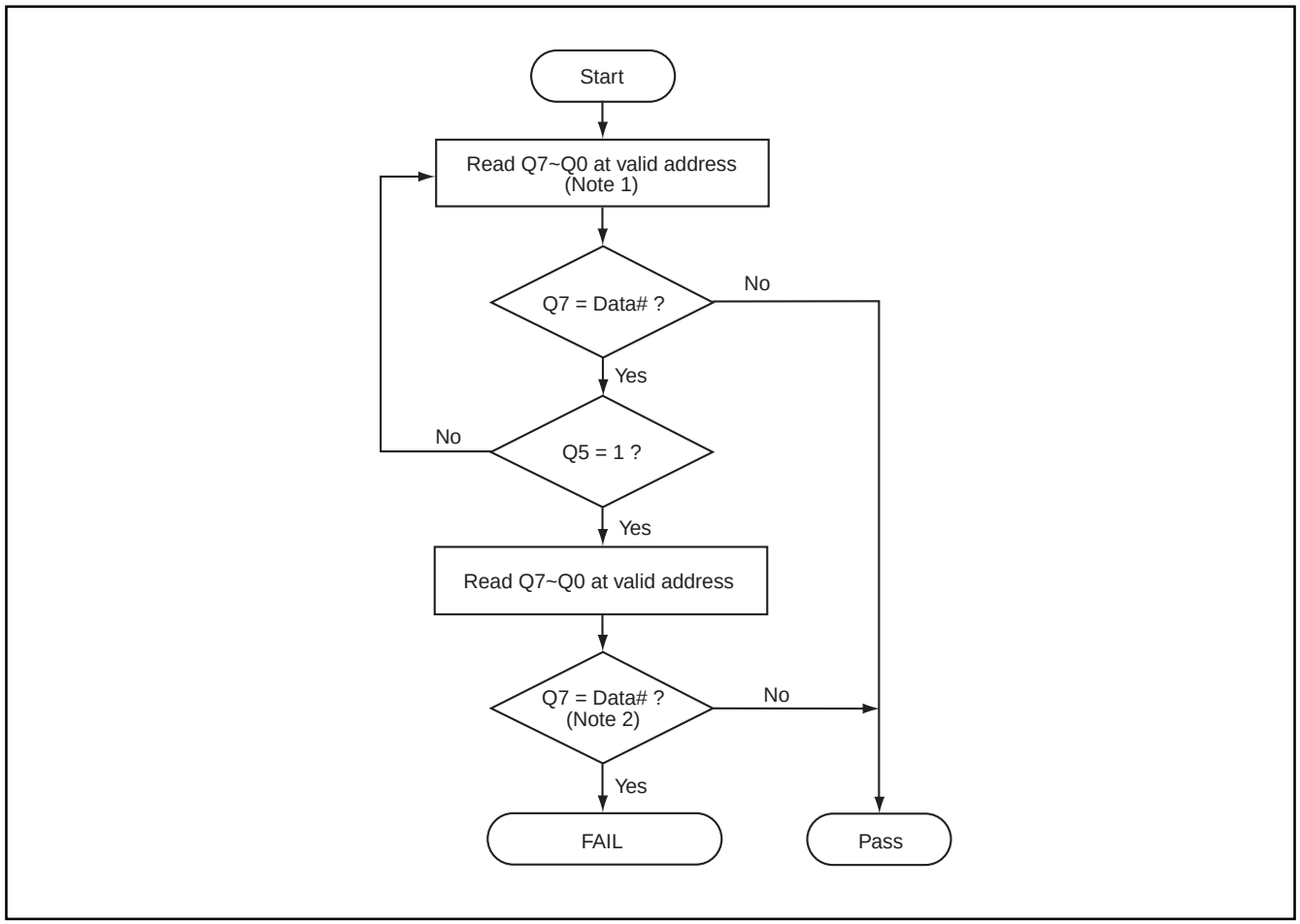
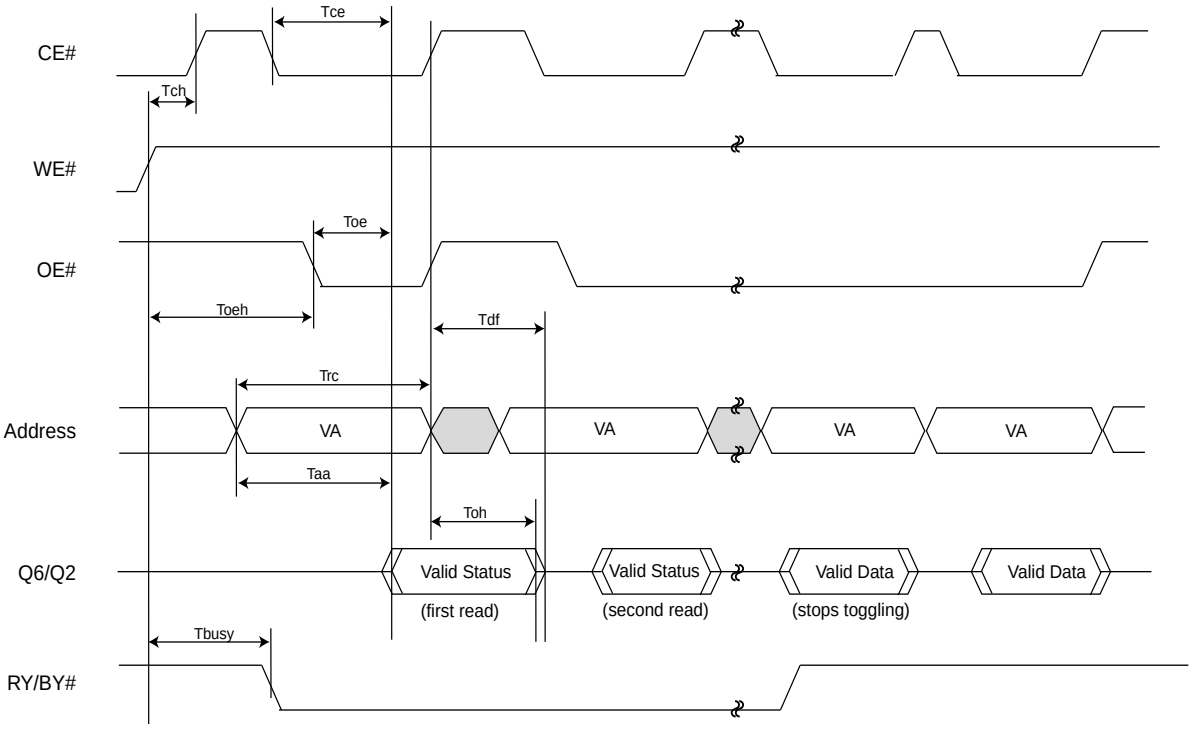


Figure 22. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5 ="1" because Q7 may change simultaneously with Q5.

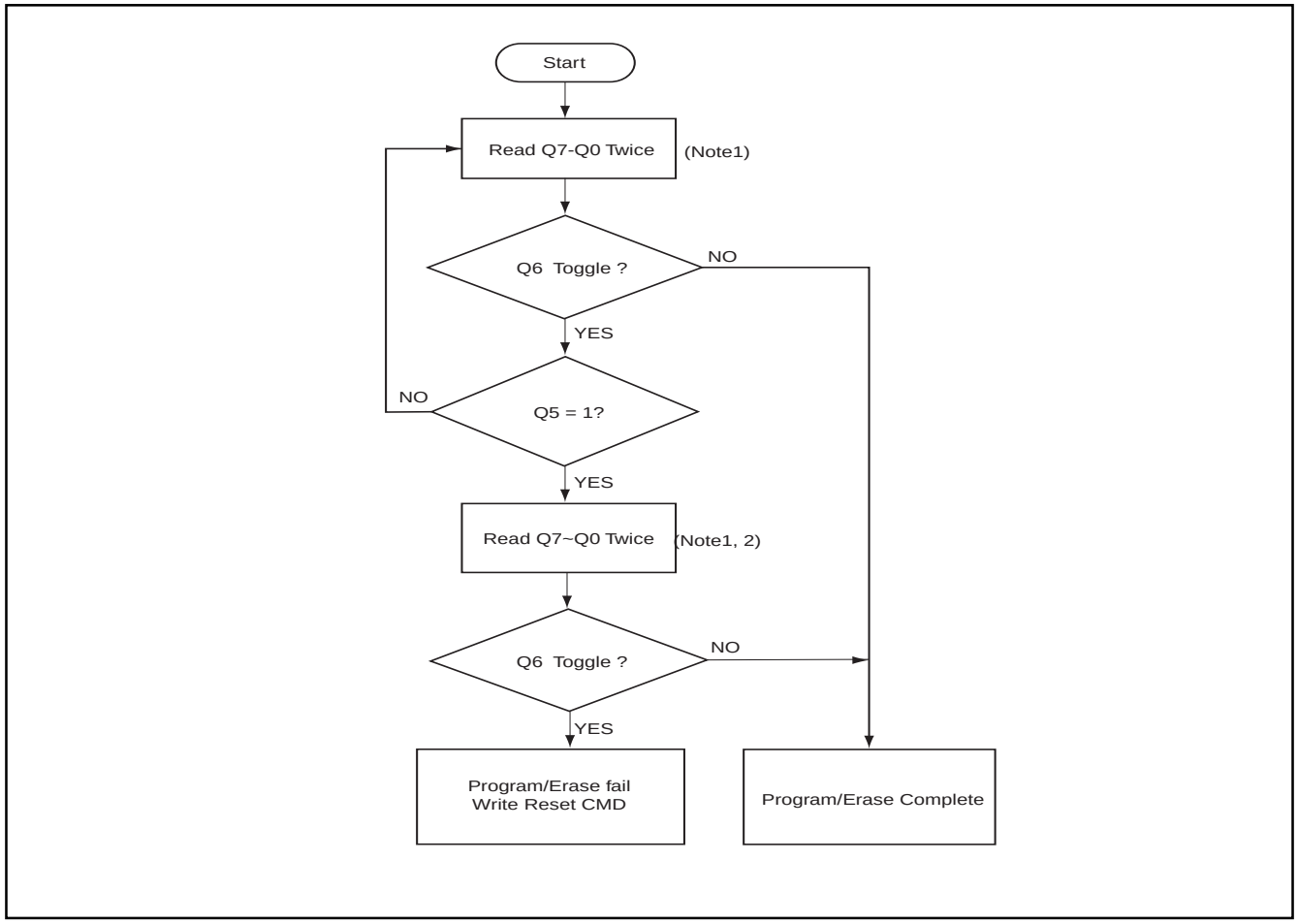
Figure 23. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Notes:

1. VA : Valid Address
2. CE# must be toggled when toggle bit toggling.

Figure 24. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

AC CHARACTERISTICS

WORD/BYTE CONFIGURATION (BYTE#)

Parameter	Description		Speed	Unit
			-90	
Telfl/Telfh	CE# to BYTE# Switching Low/High	MAX	5	ns
Tflqz	BYTE# from L to Output High-z	MAX	30	ns
Tfhqv	BYTE# from H to Output Active	MIN	90	ns

Figure 25. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)

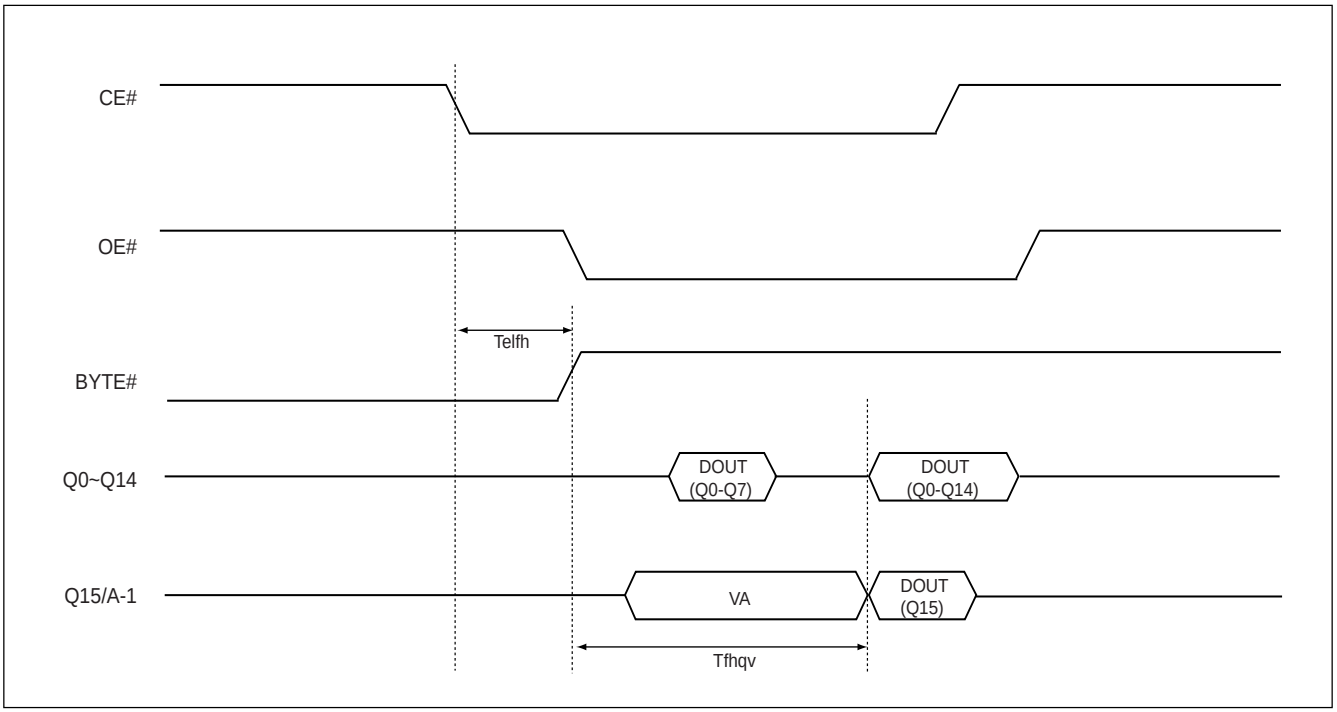


Figure 26. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from word mode to byte mode)

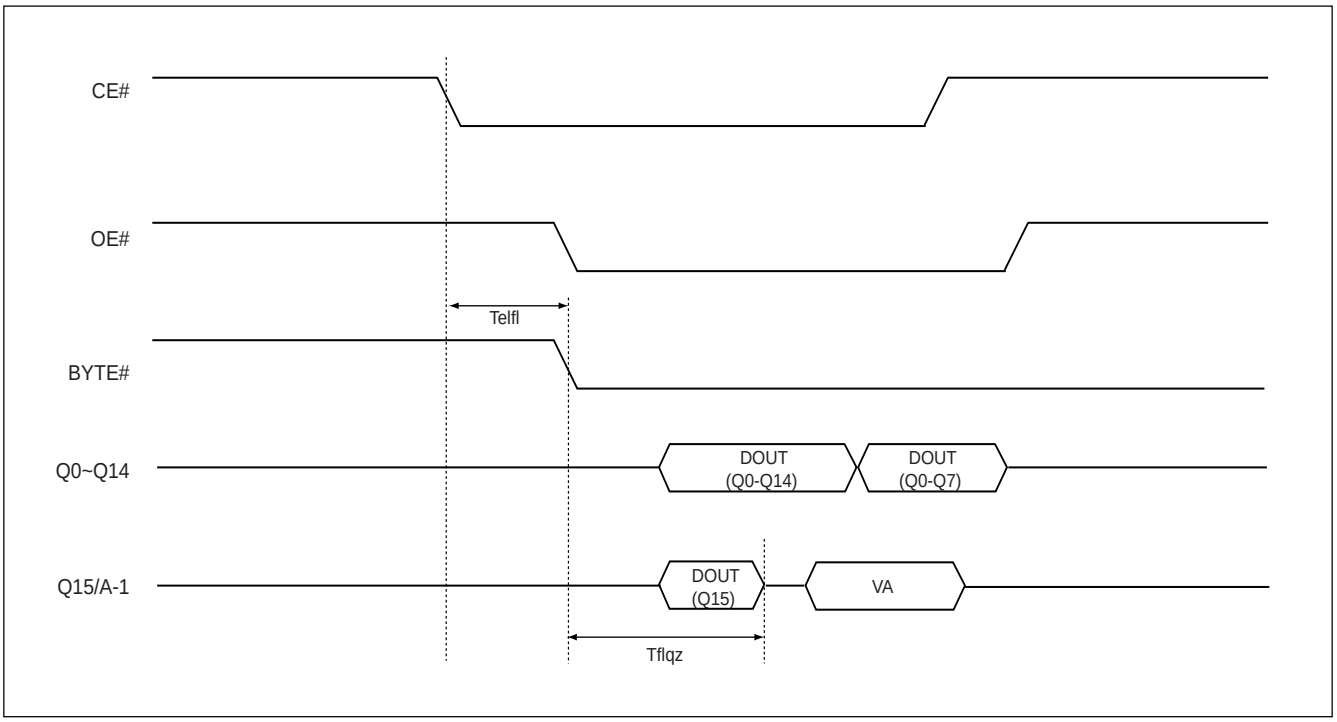
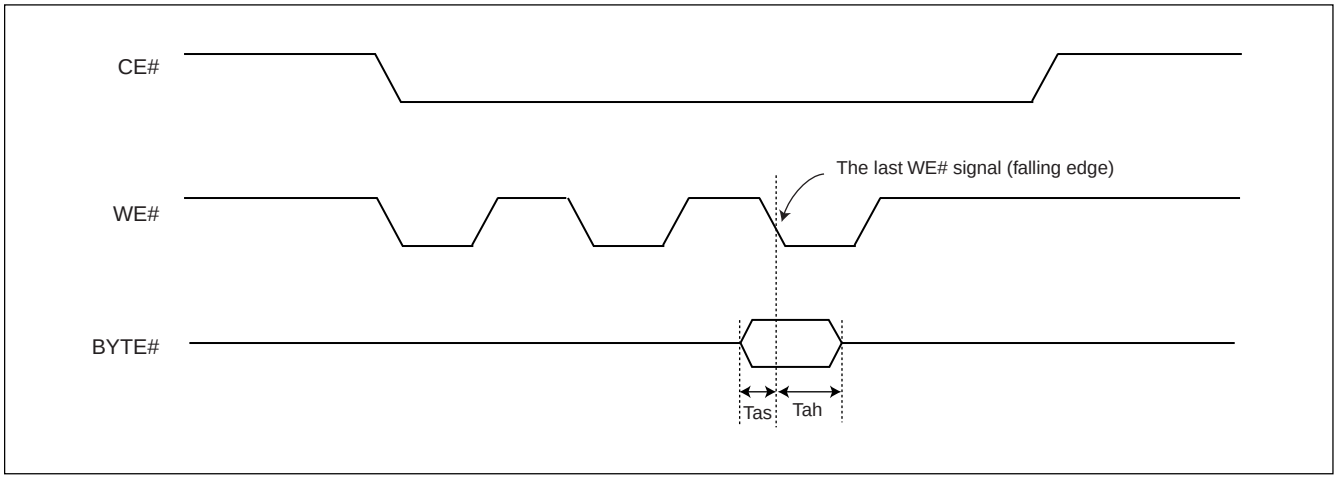


Figure 27. BYTE# TIMING WAVEFORM FOR PROGRAM OPERATIONS



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

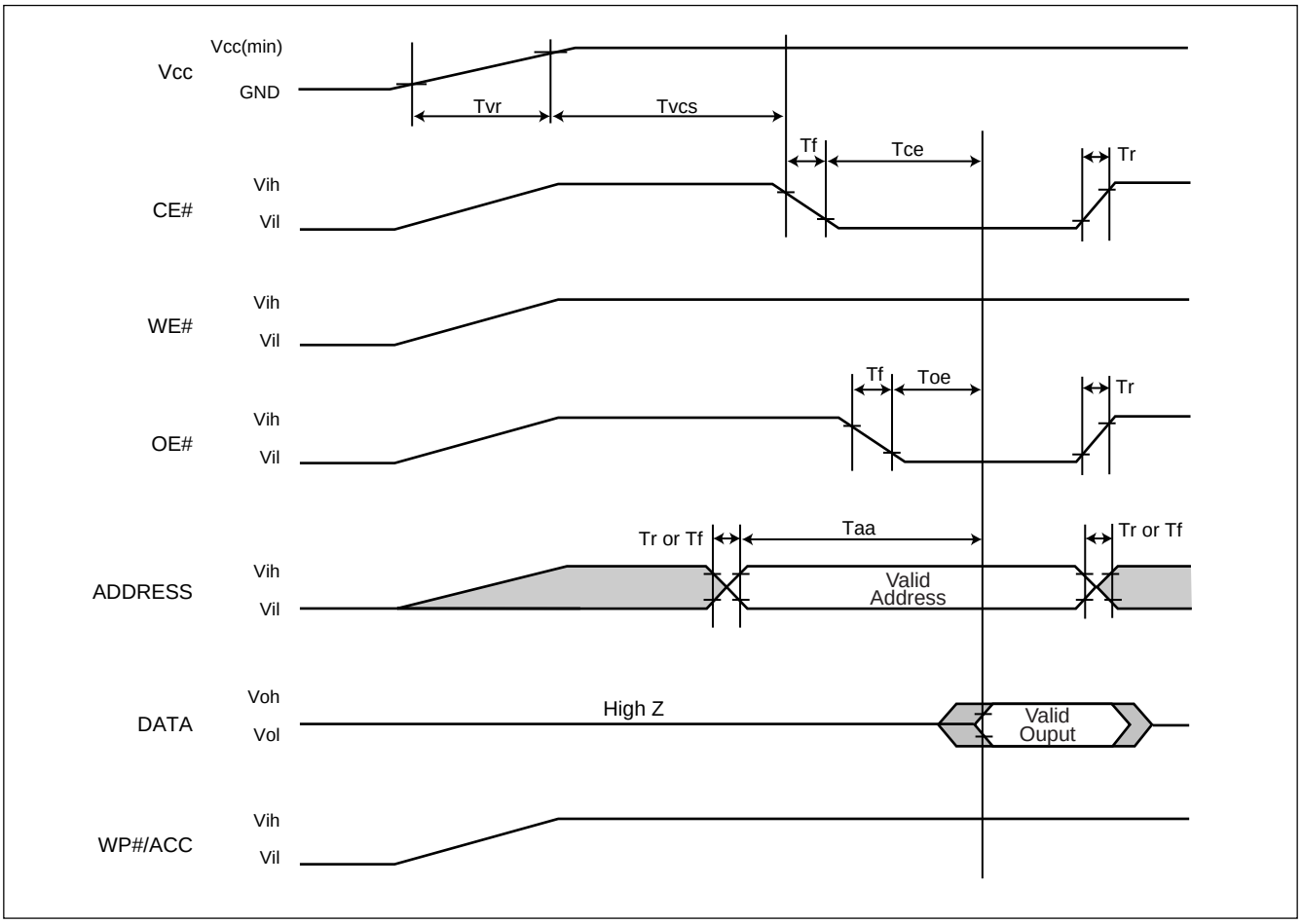


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		LIMITS MIN.	TYP.	MAX.	UNITS
Byte Programming Time			12	72	us
Word Programming Time			18	108	us
Sector Erase Time			1.3	15	sec
Chip Erase Time			9		sec
Chip Programming Time	Byte Mode		6.3		sec
	Word Mode		4.8		sec
Erase/Program Cycles		100,000			Cycles

Note: 1. Typical condition means 25° C, 1.8V.
2. Maximum condition means 90° C, 1.65V, 100K cycles.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage difference with GND on OE#, RESET#, A9	-1.0V	11V
Input Voltage difference with GND on all power pins, Address pins, CE# and WE#	-1.0V	2xVCC
Input Voltage difference with GND on all I/O pins	-1.0V	VCC + 1.0V
Vcc Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin per testing		

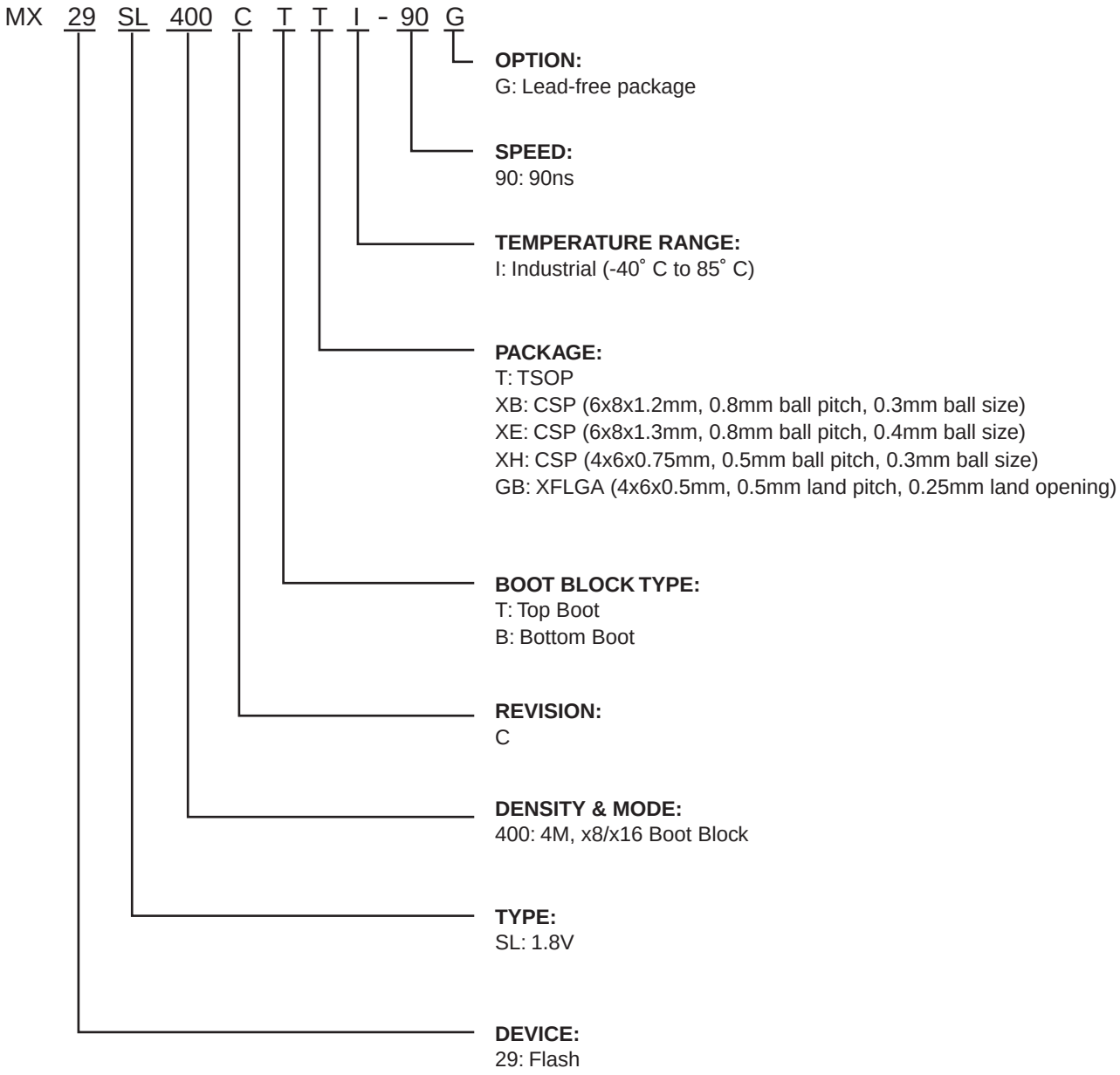
TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

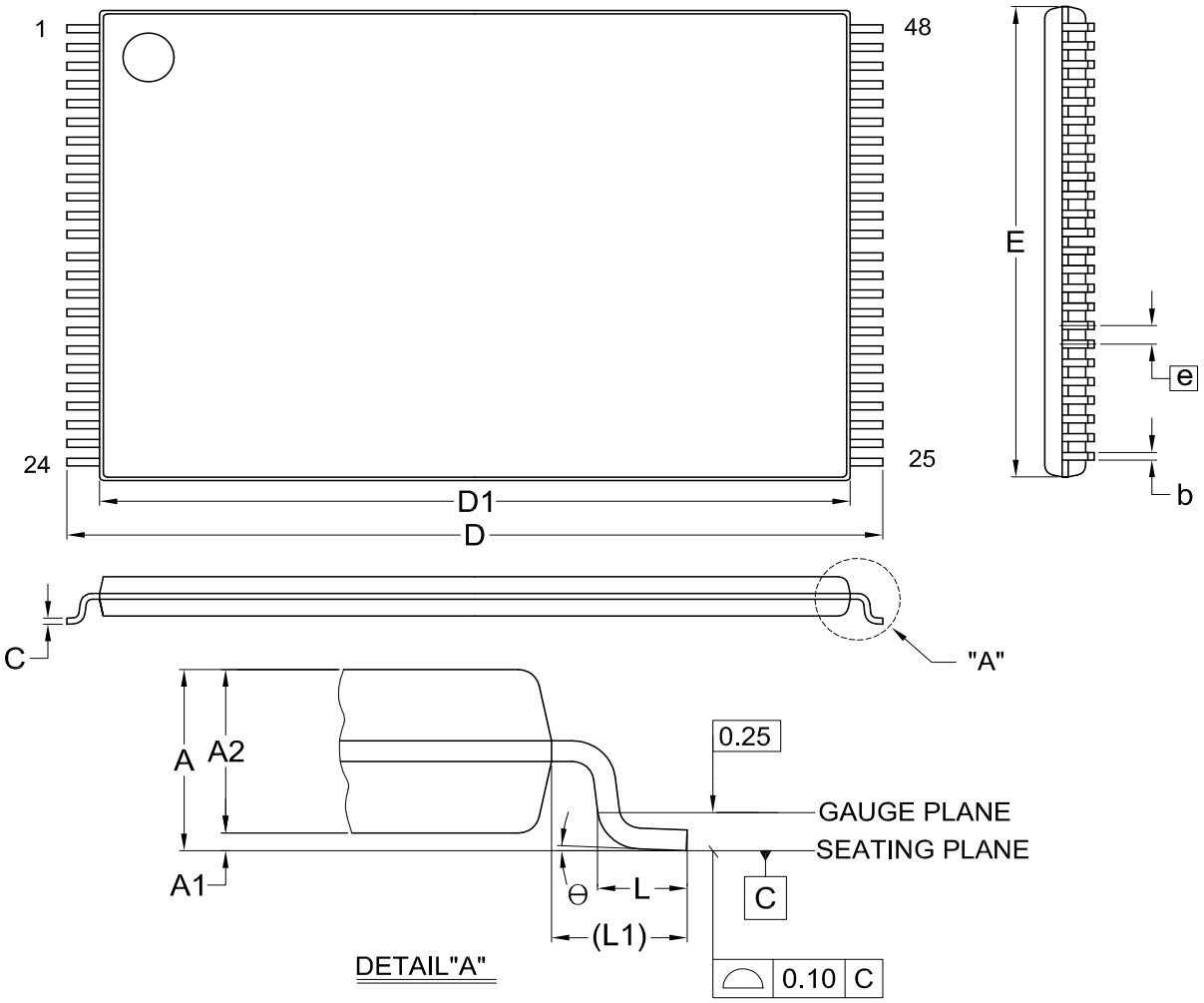
PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29SL400CTTI-90G	90	12	5	48-Pin TSOP (Normal Type)	Pb-free
MX29SL400CBTI-90G	90	12	5	48-Pin TSOP (Normal Type)	Pb-free
MX29SL400CTXBI-90G	90	12	5	48-ball CSP (6x8x1.2mm, Ball Size:0.3mm)	Pb-free
MX29SL400CBXBI-90G	90	12	5	48-ball CSP (6x8x1.2mm, Ball Size:0.3mm)	Pb-free
MX29SL400CTXEI-90G	90	12	5	48-ball CSP (6x8x1.3mm, Ball Size:0.4mm)	Pb-free
MX29SL400CBXEI-90G	90	12	5	48-ball CSP (6x8x1.3mm, Ball Size:0.4mm)	Pb-free
MX29SL400CTXHI-90G	90	12	5	48-ball CSP (4x6x0.75mm, Ball Pitch:0.5mm, Ball Size:0.3mm)	Pb-free
MX29SL400CBXHI-90G	90	12	5	48-ball CSP (4x6x0.75mm, Ball Pitch:0.5mm, Ball Size:0.3mm)	Pb-free
MX29SL400CTGBI-90G	90	12	5	48-ball XFLGA (4x6x0.5mm, Land Pitch:0.5mm, Land Opening:0.25mm)	Pb-free
MX29SL400CBGBI-90G	90	12	5	48-ball XFLGA (4x6x0.5mm, Land Pitch:0.5mm, Land Opening:0.25mm)	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM

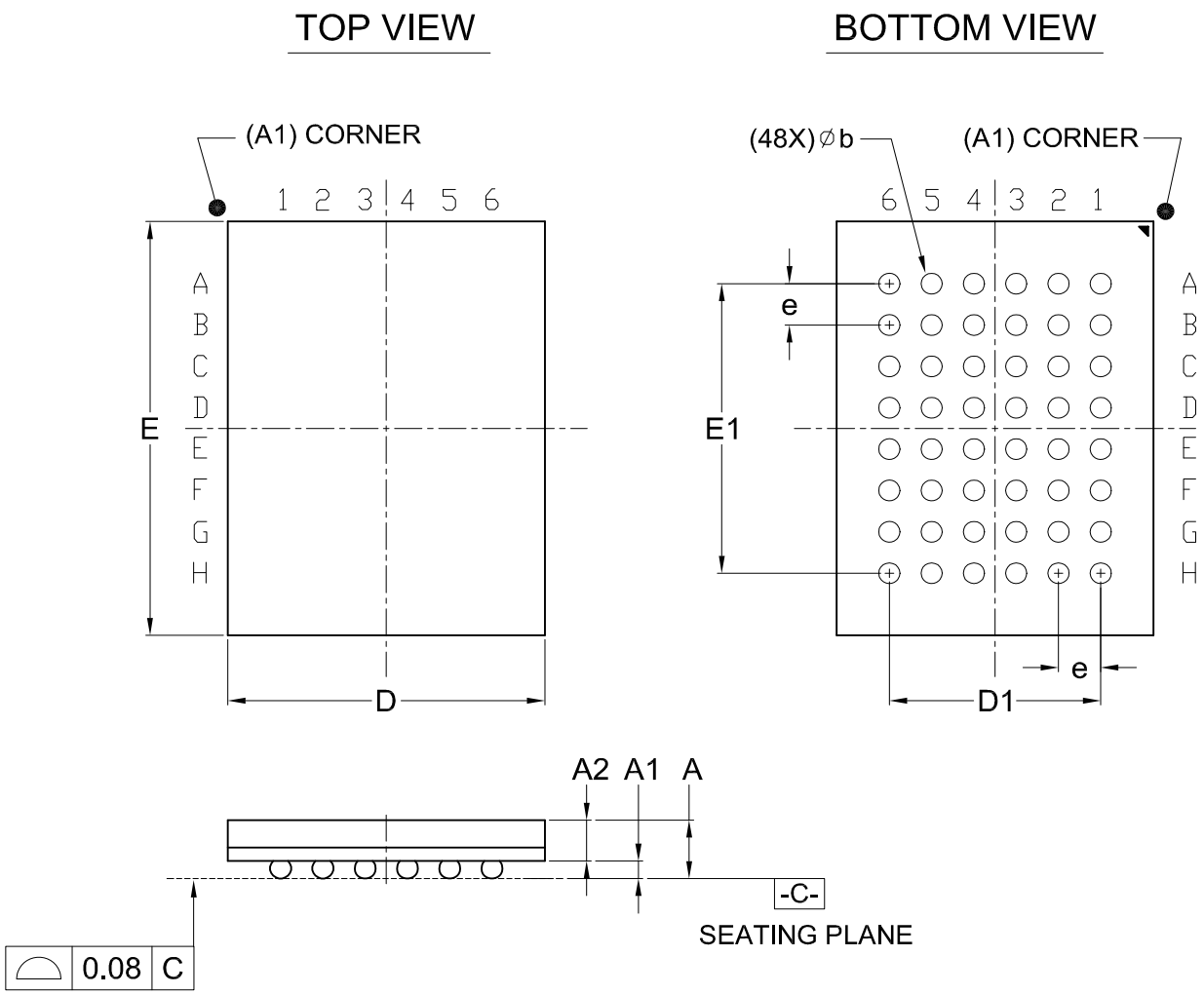


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

Title: **Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)**



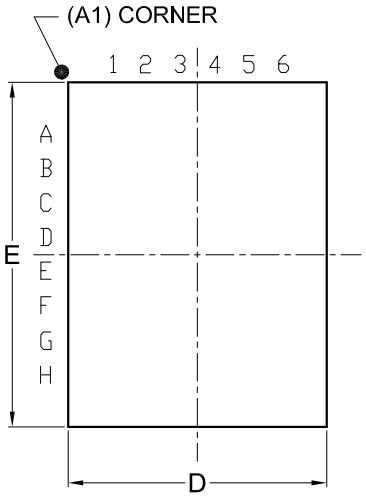
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.18	0.65	0.25	5.90		7.90		
	Nom.	---	0.23	---	0.30	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.28	---	0.35	6.10		8.10		
Inch	Min.	---	0.007	0.026	0.010	0.232		0.311		
	Nom.	---	0.009	---	0.012	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.011	---	0.014	0.240		0.319		

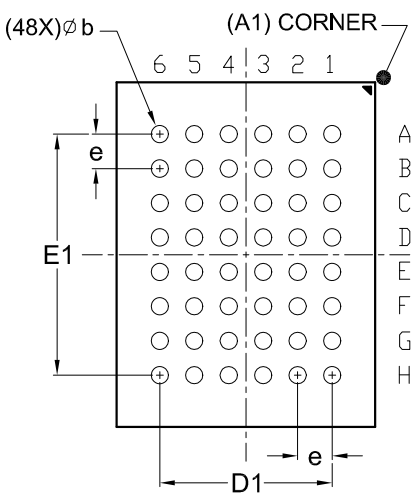
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4201	6	MO-210			03-29-'06

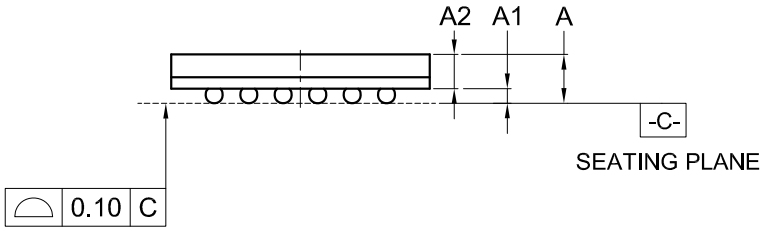
Title: **Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)**

TOP VIEW



BOTTOM VIEW



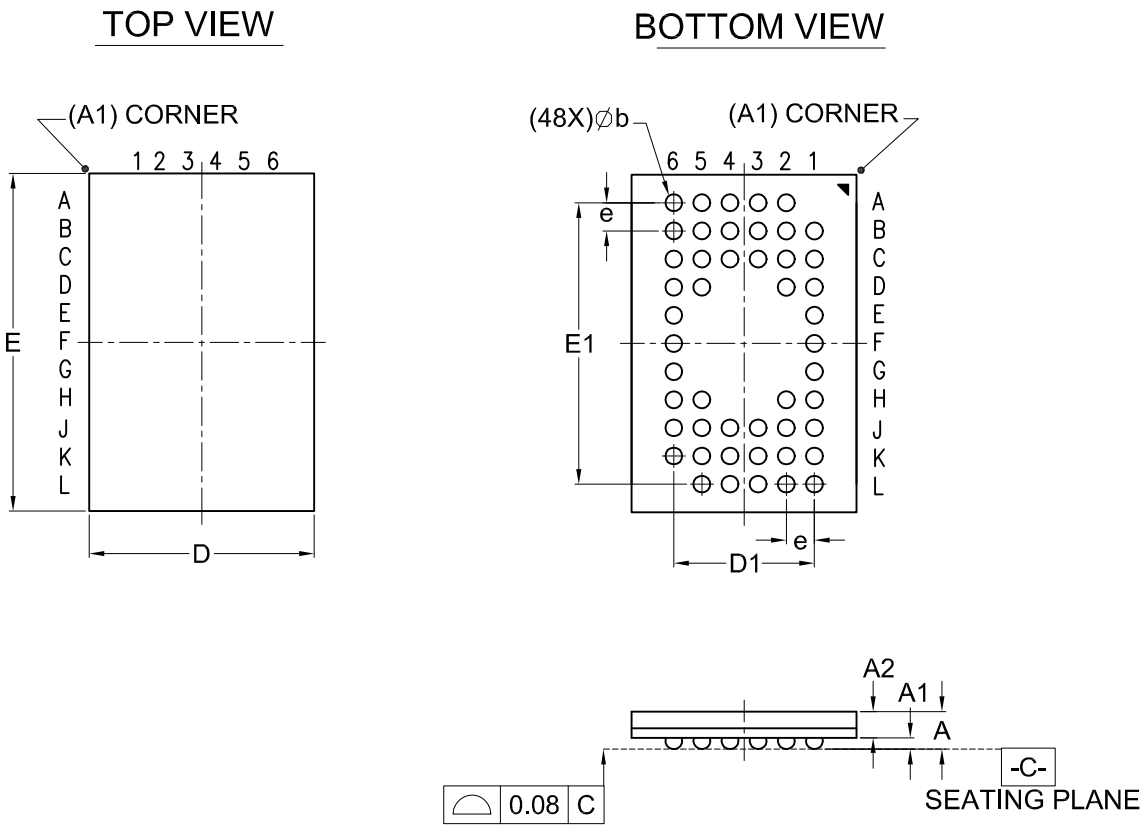


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	—	0.010	0.026	0.014	0.232		0.311		
	Nom.	—	0.012	—	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	—	0.018	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4202	4	MO-219			12-12-'03

Title: **Package Outline for CSP 48BALL(4X6X0.75MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)**

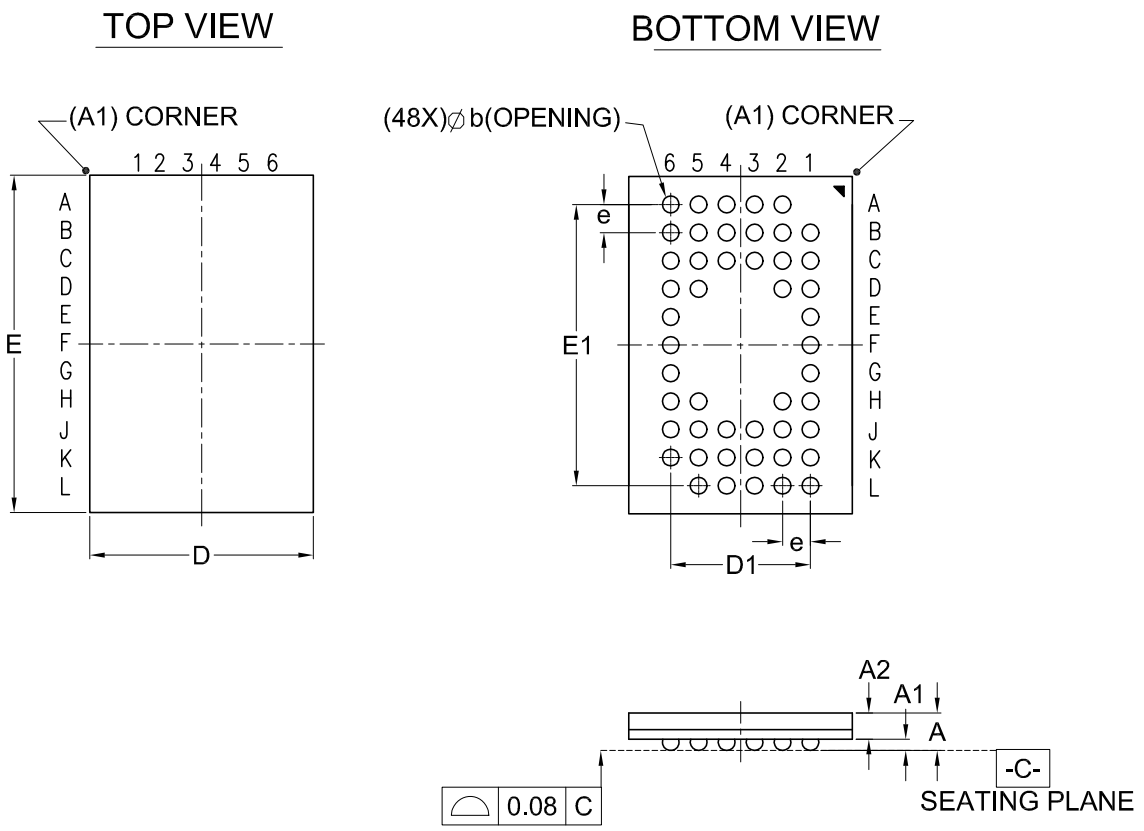


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.41	0.25	3.90		5.90		
	Nom.	---	0.21	---	0.30	4.00	2.50	6.00	5.00	0.50
	Max.	0.75	0.26	---	0.35	4.10		6.10		
Inch	Min.	---	0.006	0.016	0.010	0.154		0.232		
	Nom.	---	0.008	---	0.012	0.157	0.098	0.236	0.197	0.020
	Max.	0.030	0.010	---	0.014	0.161		0.240		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4250	1				02-14-'06

Title: **Package Outline for XFLGA 48L (4x6x0.5MM,LAND PITCH 0.5MM,LAND OPENING 0.25MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.02	0.33	0.20	3.90	—	5.90	—	—
	Nom.	---	0.05	---	0.25	4.00	2.50	6.00	5.00	0.50
	Max.	0.50	0.08	---	0.30	4.10	—	6.10	—	—
Inch	Min.	---	0.001	0.013	0.008	0.154	—	0.232	—	—
	Nom.	---	0.002	—	0.010	0.157	0.098	0.236	0.197	0.020
	Max.	0.020	0.003	—	0.012	0.161	—	0.240	—	—

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3501	0	MO-222			08-16-'06

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	Supplemented package dimension	P1~3,51,52	MAR/01/2007
0.02	Corrected wrong ordering information data	P51	JUN/20/2007
0.03	1. Revised "CFI Mode" statement	P16	JAN/16/2008
	2. Added note 4 into table 3. Command Definitions	P11	
0.04	1. Announced "phase-out" wording	P1,2	SEP/03/2008

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