MX29LV321D T/B

DATASHEET

Contents

FEATURES **5**
GENERAL DESCRIPTION **6**
PIN CONFIGURATION **7**
PIN DESCRIPTION **8**
BLOCK DIAGRAM **9**
BLOCK DIAGRAM DESCRIPTION **10**
BLOCK STRUCTURE **11**
Table 1-1. MX29LV321DT SECTOR GROUP ARCHITECTURE 11
Table 1-2. MX29LV321DB SECTOR GROUP ARCHITECTURE 13
BUS OPERATION **15**
Table 2-1. BUS OPERATION 15
Table 2-2. BUS OPERATION 16
FUNCTIONAL OPERATION DESCRIPTION **17**
READ OPERATION 17
WRITE OPERATION 17
DEVICE RESET 17
STANDBY MODE 17
OUTPUT DISABLE 17
HARDWARE WRITE PROTECT 18
ACCELERATED PROGRAMMING OPERATION 18
TEMPORARY SECTOR GROUP UNPROTECT OPERATION 18
SECTOR GROUP PROTECT OPERATION 18
CHIP UNPROTECT OPERATION 18
AUTOMATIC SELECT BUS OPERATIONS 19
SECTOR LOCK STATUS VERIFICATION 19
READ SILICON ID MANUFACTURER CODE 19
READ SILICON ID MX29LV321DT CODE 19
READ SILICON ID MX29LV321DB CODE 19
READ INDICATOR BIT (Q7) FOR SECURITY SECTOR 19
INHERENT DATA PROTECTION 20
COMMAND COMPLETION 20
LOW VCC WRITE INHIBIT 20
WRITE PULSE "GLITCH" PROTECTION 20
LOGICAL INHIBIT 20
POWER-UP SEQUENCE 20
POWER-UP WRITE INHIBIT 20
POWER SUPPLY DECOUPLING 20
COMMAND OPERATIONS **21**
TABLE 3. MX29LV321D T/B COMMAND DEFINITIONS 21

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY 22
SECTOR ERASE 23
CHIP ERASE 24
SECTOR ERASE SUSPEND 24
SECTOR ERASE RESUME 25
AUTOMATIC SELECT OPERATIONS 25
AUTOMATIC SELECT COMMAND SEQUENCE 25
READ MANUFACTURER ID OR DEVICE ID 26
SECURITY SECTOR LOCK STATUS 26
VERIFY SECTOR GROUP PROTECTION 26
SECURITY SECTOR FLASH MEMORY REGION 26
FACTORY LOCKED: SECURITY SECTOR PROGRAMMED AND PROTECTED AT THE FACTORY 26
CUSTOMER LOCKABLE: SECURITY SECTOR NOT PROGRAMMED OR PROTECTED AT THE FACTORY 27
ENTER AND EXIT SECURITY SECTOR 27
RESET OPERATION 28
COMMON FLASH MEMORY INTERFACE (CFI) MODE 29
QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE 29
Table 4-1. CFI mode: Identification Data Values 29
Table 4-2. CFI Mode: System Interface Data Values 29
Table 4-3. CFI Mode: Device Geometry Data Values 30
Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values 31
ELECTRICAL CHARACTERISTICS 32
ABSOLUTE MAXIMUM STRESS RATINGS 32
OPERATING TEMPERATURE AND VOLTAGE 32
DC CHARACTERISTICS 33
SWITCHING TEST CIRCUITS 34
SWITCHING TEST WAVEFORMS 34
AC CHARACTERISTICS 35
WRITE COMMAND OPERATION 36
Figure 1. COMMAND WRITE OPERATION 36
READ/RESET OPERATION 37
Figure 2. READ TIMING WAVEFORMS 37
Figure 3. RESET# TIMING WAVEFORM 38
ERASE/PROGRAM OPERATION 39
Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM 39
Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART 40
Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM 41
Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART 42
Figure 8. ERASE SUSPEND/RESUME FLOWCHART 43
Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORM 44
Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM 44

Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM 45
Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART 46
SECTOR GROUP PROTECT/CHIP UNPROTECT 47
Figure 13. Sector Group Protect/Chip Unprotect Waveform (RESET# Control) 47
Figure 14. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv 48
Figure 15. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv 49
Table 5. TEMPORARY SECTOR GROUP UNPROTECT 50
Figure 16. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS 50
Figure 17. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART 51
Figure 18. SILICON ID READ TIMING WAVEFORM 52
WRITE OPERATION STATUS 53
Figure 19. DATA# POLLING TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM) 53
Figure 20. DATA# POLLING ALGORITHM 54
Figure 21. TOGGLE BIT TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM) 55
Figure 22. TOGGLE BIT ALGORITHM 56
RECOMMENDED OPERATING CONDITIONS 57
ERASE AND PROGRAMMING PERFORMANCE 58
DATA RETENTION 58
LATCH-UP CHARACTERISTICS 58
TSOP PIN/BGA PACKAGE CAPACITANCE 58
ORDERING INFORMATION 59
PART NAME DESCRIPTION 60
PACKAGE INFORMATION 61
REVISION HISTORY 63

32M-BIT [2M x 16] 3V SUPPLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Word mode only
  - 2,097,152 x 16
- Sector Structure
  - 4K-Word x 8 and 32K-Word x 63
- Extra 64K-Byte sector for security
  - Features factory locked and identifiable, and customer lockable
- Twenty-Four Sector Groups
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector group unprotect function for code changing in previously protected sector groups
- Power Supply Operation
  - Vcc 2.7 to 3.6 volt for read, erase, and program operations
  - VI/O 1.65V to 3.6V for Input/Output
- Latch-up protected to 100mA from -1V to 1.5 x Vcc
- Low Vcc write inhibit : Vcc ≤ Vlko
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 90ns
  - Word program time: 11us/word (typical)
  - Fast erase time: 0.7s/sector, 35s/chip (typical)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 5uA (typical)
- 100,000 erase/program cycle (typical)
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Provides accelerated program capability

PACKAGE

- 48-Pin TSOP
- 48-Ball TFBGA
- **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

MX29LV321DT/B is a 32Mbit flash memory that can be organized as 2,097,152 words. These devices operate over a voltage range of 2.7V to 3.6V typically using a 3V power supply input. The memory array is divided into 64 equal 64 Kilo byte blocks. However, depending on the device being used as a Top-Boot or Bottom-Boot device, the top or the bottom first block is further subdivided into 8 equal 4Kword blocks. The outermost two sectors at the top or at the bottom are respectively the boot blocks for this device. This flash memory also provides an additional factory lockable or customer lockable 32Kword sector to provide security feature.

The MX29LV321DT/B is offered in a 48-pin TSOP and a 48-ball TFBGA JEDEC standard package. These packages are offered lead-free versions that are compliant to the RoHS specifications. The software algorithm used for this device also adheres to the JEDEC standard for single power supply devices. These flash parts can be programmed in system or on commercially available EPROM/Flash programmers.

Separate OE# and CE# (Output Enable and Chip Enable) signals are provided to simplify system design. When used with high speed processors, the 90ns read access time of this flash memory permits operation with minimal time lost due to system timing delays.

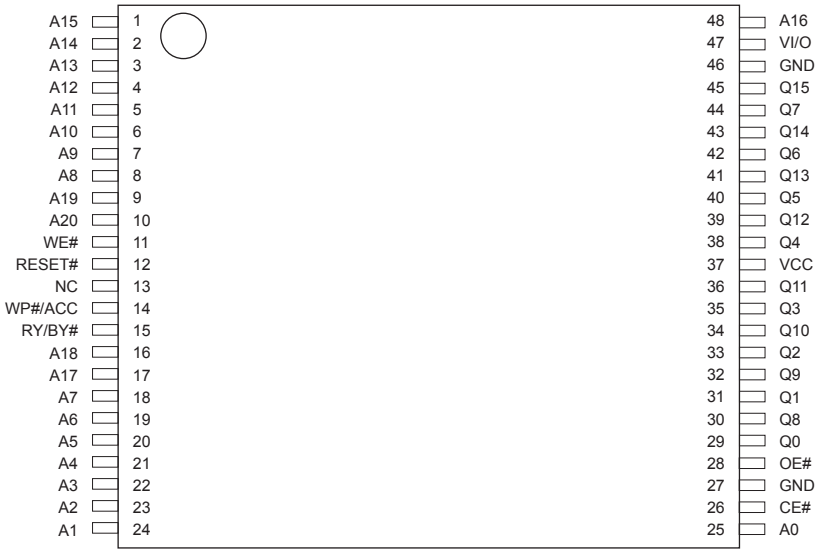
The automatic write algorithm provided on Macronix flash memories perform an automatic erase prior to write. The user only needs to provide a write command to the command register. The on-chip state machine automatically controls the program and erase functions including all necessary internal timings. Since erase and write operations take much longer time than read operations, erase/write can be interrupted to perform read operations in other sectors of the device. For this, Erase Suspend operation along with Erase Resume operation are provided. Data# polling or Toggle bits are used to indicate the end of the erase/write operation.

These devices are manufactured at the Macronix fabrication facility using the time tested and proven MXIC's advanced technology. This proprietary non-epi process provides a very high degree of latch-up protection for stresses up to 100 milliamperes on address and data pins from -1V to 1.5xVCC.

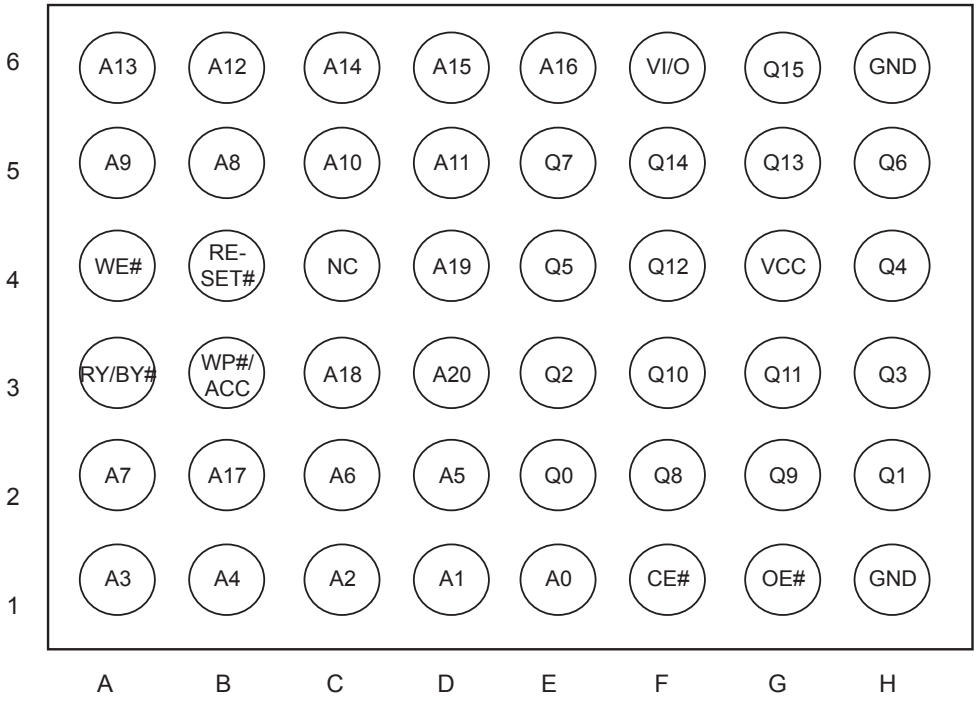
With low power consumption and enhanced hardware and software features, this flash memory retains data reliably for at least 20 years. Erase and programming functions have been tested to meet a typical specification of 100,000 cycles of operation.

PIN CONFIGURATION

48 TSOP



48-Ball TFBGA (6mm x 8mm, Top View, Balls Facing Down)

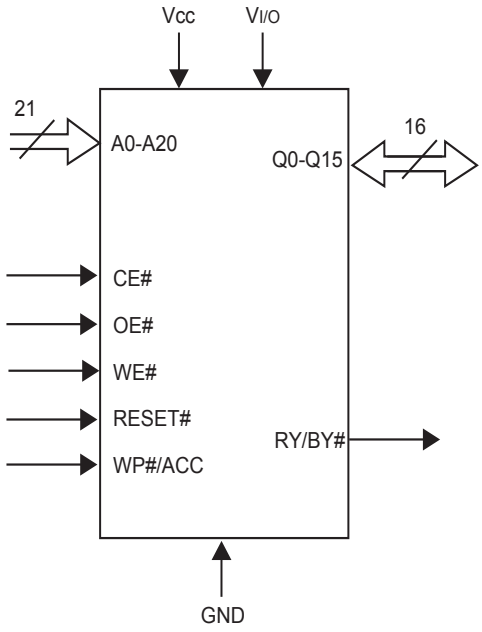


PIN DESCRIPTION

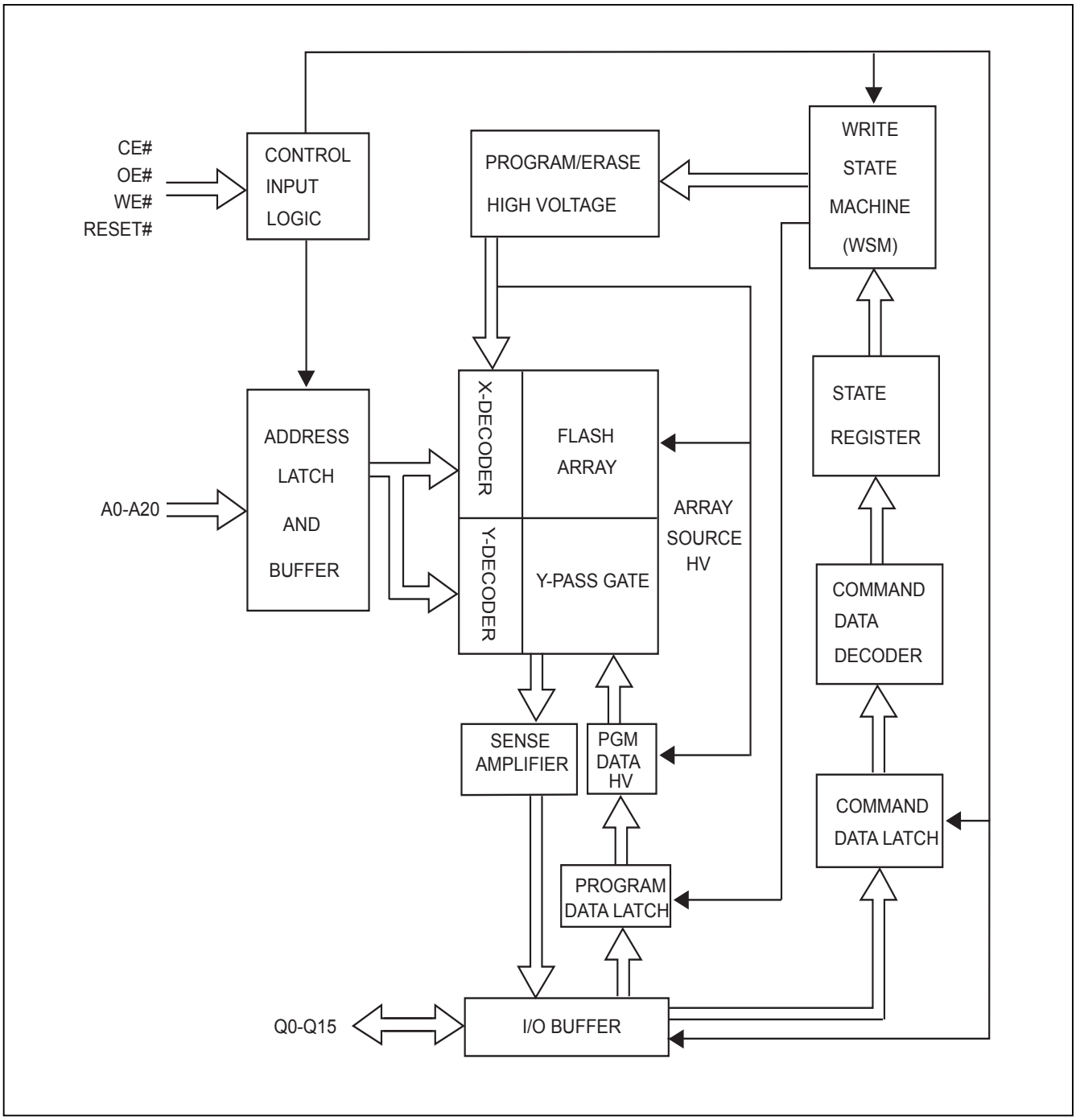
SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15	Q15(Data Input/Output, word mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply
VI/O	Power Supply for Input/Output
WP#/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

Note: If customers do not need WP#/ACC feature, please connect WP#/ACC pin to VCC or let it floating. The WP#/ACC has an internal pull-up when unconnected WP#/ACC is at Vih.

LOGIC SYMBOL



BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

The block diagram on Page 9 illustrates a simplified architecture of MX29LV321D T/B. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array..

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A20). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", and "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the y-pass gates. Sense amplifiers are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15 pads. During read operation, the I/O buffer receives data from sense amplifiers and drives the output pads accordingly. In the last cycle of program command, the I/O buffer transmits the data on Q0-Q15 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, "FLASH ARRAY", and "PGM DATA HV" block. The logic control module comprises of the "WRITE STATE MACHINE (WSM)", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15 is latched in the command data latch and is decoded by the command data decoder. The state register receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

BLOCK STRUCTURE

The main flash memory array can be organized as 2M Words. The details of the address ranges and the corresponding sector addresses are shown in Table 1-1 & 1-2. Table 1-1 shows the sector group architecture for the Top Boot part, whereas Table 1-2 shows the sector group architecture for the Bottom Boot part. The specific security sector addresses are shown at the bottom off each of these tables.

Table 1-1. MX29LV321DT SECTOR GROUP ARCHITECTURE

Sector Group	Sector Size Word Mode (Kwords)	Sector	Sector Address A20-A12	Address Range Word Mode (x16)
1	32	SA0	000000xxx	000000h-07FFFh
1	32	SA1	000001xxx	008000h-0FFFFh
1	32	SA2	000010xxx	010000h-17FFFh
1	32	SA3	000011xxx	018000h-01FFFFh
2	32	SA4	000100xxx	020000h-027FFFh
2	32	SA5	000101xxx	028000h-02FFFFh
2	32	SA6	000110xxx	030000h-037FFFh
2	32	SA7	000111xxx	038000h-03FFFFh
3	32	SA8	001000xxx	040000h-047FFFh
3	32	SA9	001001xxx	048000h-04FFFFh
3	32	SA10	001010xxx	050000h-057FFFh
3	32	SA11	001011xxx	058000h-05FFFFh
4	32	SA12	001100xxx	060000h-067FFFh
4	32	SA13	001101xxx	068000h-06FFFFh
4	32	SA14	001110xxx	070000h-077FFFh
4	32	SA15	001111xxx	078000h-07FFFFh
5	32	SA16	010000xxx	080000h-087FFFh
5	32	SA17	010001xxx	088000h-08FFFFh
5	32	SA18	010010xxx	090000h-097FFFh
5	32	SA19	010011xxx	098000h-09FFFFh
6	32	SA20	010100xxx	0A0000h-0A7FFFh
6	32	SA21	010101xxx	0A8000h-0AFFFFh
6	32	SA22	010110xxx	0B0000h-0B7FFFh
6	32	SA23	010111xxx	0B8000h-0BFFFFh
7	32	SA24	011000xxx	0C0000h-0C7FFFh
7	32	SA25	011001xxx	0C8000h-0CFFFFh
7	32	SA26	011010xxx	0D0000h-0D7FFFh
7	32	SA27	011011xxx	0D8000h-0DFFFFh
8	32	SA28	011100xxx	0E0000h-0E7FFFh
8	32	SA29	011101xxx	0E8000h-0EFFFFh
8	32	SA30	011110xxx	0F0000h-0F7FFFh
8	32	SA31	011111xxx	0F8000h-0FFFFFh
9	32	SA32	100000xxx	100000h-107FFFh
9	32	SA33	100001xxx	108000h-10FFFFh
9	32	SA34	100010xxx	110000h-117FFFh
9	32	SA35	100011xxx	118000h-11FFFFh

Sector Group	Sector Size Word Mode (Kwords)	Sector	Sector Address A20-A12	Address Range Word Mode (x16)
10	32	SA36	100100xxx	120000h-127FFFh
10	32	SA37	100101xxx	128000h-12FFFFh
10	32	SA38	100110xxx	130000h-137FFFh
10	32	SA39	100111xxx	138000h-13FFFFh
11	32	SA40	101000xxx	140000h-147FFFh
11	32	SA41	101001xxx	148000h-14FFFFh
11	32	SA42	101010xxx	150000h-157FFFh
11	32	SA43	101011xxx	158000h-15FFFFh
12	32	SA44	101100xxx	160000h-167FFFh
12	32	SA45	101101xxx	168000h-16FFFFh
12	32	SA46	101110xxx	170000h-177FFFh
12	32	SA47	101111xxx	178000h-17FFFFh
13	32	SA48	110000xxx	180000h-187FFFh
13	32	SA49	110001xxx	188000h-18FFFFh
13	32	SA50	110010xxx	190000h-197FFFh
13	32	SA51	110011xxx	198000h-19FFFFh
14	32	SA52	110100xxx	1A0000h-1A7FFFh
14	32	SA53	110101xxx	1A8000h-1AFFFFh
14	32	SA54	110110xxx	1B0000h-1B7FFFh
14	32	SA55	110111xxx	1B8000h-1BFFFFh
15	32	SA56	111000xxx	1C0000h-1C7FFFh
15	32	SA57	111001xxx	1C8000h-1CFFFFh
15	32	SA58	111010xxx	1D0000h-1D7FFFh
15	32	SA59	111011xxx	1D8000h-1DFFFFh
16	32	SA60	111100xxx	1E0000h-1E7FFFh
16	32	SA61	111101xxx	1E8000h-1EFFFFh
16	32	SA62	111110xxx	1F0000h-1F7FFFh
17	4	SA63	111111000	1F8000h-1F8FFFh
18	4	SA64	111111001	1F9000h-1F9FFFh
19	4	SA65	111111010	1FA000h-1FAFFFh
20	4	SA66	111111011	1FB000h-1FBFFFh
21	4	SA67	111111100	1FC000h-1FCFFFh
22	4	SA68	111111101	1FD000h-1FDFFFh
23	4	SA69	111111110	1FE000h-1FEFFFh
24	4	SA70	111111111	1FF000h-1FFFFFh

Top Boot Security Sector Addresses

Sector Size Word Mode (Kwords)	Sector Address A20~A12	Address Range Word Mode (x16)
32	111111xxx	1F8000h-1FFFFFh

Table 1-2. MX29LV321DB SECTOR GROUP ARCHITECTURE

Sector Group	Sector Size Word Mode (Kwords)	Sector	Sector Address A20-A12	Address Range Word Mode (x16)
1	4	SA0	000000000	000000h-000FFFh
2	4	SA1	000000001	001000h-001FFFh
3	4	SA2	000000010	002000h-002FFFh
4	4	SA3	000000011	003000h-003FFFh
5	4	SA4	000000100	004000h-004FFFh
6	4	SA5	000000101	005000h-005FFFh
7	4	SA6	000000110	006000h-006FFFh
8	4	SA7	000000111	007000h-007FFFh
9	32	SA8	000001xxx	008000h-00FFFFh
9	32	SA9	000010xxx	010000h-017FFFh
9	32	SA10	000011xxx	018000h-01FFFFh
10	32	SA11	000100xxx	020000h-027FFFh
10	32	SA12	000101xxx	028000h-02FFFFh
10	32	SA13	000110xxx	030000h-037FFFh
10	32	SA14	000111xxx	038000h-03FFFFh
11	32	SA15	001000xxx	040000h-047FFFh
11	32	SA16	001001xxx	048000h-04FFFFh
11	32	SA17	001010xxx	050000h-057FFFh
11	32	SA18	001011xxx	058000h-05FFFFh
12	32	SA19	001100xxx	060000h-067FFFh
12	32	SA20	001101xxx	068000h-06FFFFh
12	32	SA21	001110xxx	070000h-077FFFh
12	32	SA22	001111xxx	078000h-07FFFFh
13	32	SA23	010000xxx	080000h-087FFFh
13	32	SA24	010001xxx	088000h-08FFFFh
13	32	SA25	010010xxx	090000h-097FFFh
13	32	SA26	010011xxx	098000h-09FFFFh
14	32	SA27	010100xxx	0A0000h-0A7FFFh
14	32	SA28	010101xxx	0A8000h-0AFFFFh
14	32	SA29	010110xxx	0B0000h-0B7FFFh
14	32	SA30	010111xxx	0B8000h-0BFFFFh
15	32	SA31	011000xxx	0C0000h-0C7FFFh
15	32	SA32	011001xxx	0C8000h-0CFFFFh
15	32	SA33	011010xxx	0D0000h-0D7FFFh
15	32	SA34	011011xxx	0D8000h-0DFFFFh
16	32	SA35	011100xxx	0E0000h-0E7FFFh
16	32	SA36	011101xxx	0E8000h-0EFFFFh
16	32	SA37	011110xxx	0F0000h-0F7FFFh
16	32	SA38	011111xxx	0F8000h-0FFFFFh
17	32	SA39	100000xxx	100000h-107FFFh
17	32	SA40	100001xxx	108000h-10FFFFh
17	32	SA41	100010xxx	110000h-117FFFh
17	32	SA42	100011xxx	118000h-11FFFFh

Sector Group	Sector Size Word Mode (Kwords)	Sector	Sector Address A20-A12	Address Range Word Mode (x16)
18	32	SA43	100100xxx	120000h-127FFFh
18	32	SA44	100101xxx	128000h-12FFFFh
18	32	SA45	100110xxx	130000h-137FFFh
18	32	SA46	100111xxx	138000h-13FFFFh
19	32	SA47	101000xxx	140000h-147FFFh
19	32	SA48	101001xxx	148000h-14FFFFh
19	32	SA49	101010xxx	150000h-157FFFh
19	32	SA50	101011xxx	158000h-15FFFFh
20	32	SA51	101100xxx	160000h-167FFFh
20	32	SA52	101101xxx	168000h-16FFFFh
20	32	SA53	101110xxx	170000h-177FFFh
20	32	SA54	101111xxx	178000h-17FFFFh
21	32	SA55	110000xxx	180000h-187FFFh
21	32	SA56	110001xxx	188000h-18FFFFh
21	32	SA57	110010xxx	190000h-197FFFh
21	32	SA58	110011xxx	198000h-19FFFFh
22	32	SA59	110100xxx	1A0000h-1A7FFFh
22	32	SA60	110101xxx	1A8000h-1AFFFFh
22	32	SA61	110110xxx	1B0000h-1B7FFFh
22	32	SA62	110111xxx	1B8000h-1BFFFFh
23	32	SA63	111000xxx	1C0000h-1C7FFFh
23	32	SA64	111001xxx	1C8000h-1CFFFFh
23	32	SA65	111010xxx	1D0000h-1D7FFFh
23	32	SA66	111011xxx	1D8000h-1DFFFFh
24	32	SA67	111100xxx	1E0000h-1E7FFFh
24	32	SA68	111101xxx	1E8000h-1EFFFFh
24	32	SA69	111110xxx	1F0000h-1F7FFFh
24	32	SA70	111111xxx	1F8000h-1FFFFFh

Bottom Boot Security Sector Addresses

Sector Size Word Mode (Kwords)	Sector Address A20~A12	Address Range Word Mode (x16)
32	000000xxx	00000h-07FFFh

BUS OPERATION

Table 2-1. BUS OPERATION

Mode Select	RESET#	CE#	WE#	OE#	Address	Data (I/O) Q0~Q15	WP#/ACC
Device Reset	L	X	X	X	X	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc ± 0.3V	X	X	X	HighZ	H
Output Disable	H	L	H	H	X	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	L/H
Write(Note1)	H	L	L	H	AIN	DIN	Note3
Accelerate Program	H	L	L	H	AIN	DIN	Vhv
Temporary Sector-Group Unprotect	Vhv	X	X	X	AIN	DIN	Note3
Sector-Group Protect (Note2)	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	L/H
Chip Unprotect (Note2)	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	Note3

Notes:
1. All sectors will be unprotected if WP#/ACC=Vhv.
2. The two outmost boot sectors are protected if WP#/ACC=Vil.
3. When WP#/ACC = Vih, the protection conditions of the two outmost boot sectors depend on previous protection conditions."Sector/Sector Block Protection and Unprotection" describes the protect and unprotect method.
4. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.

Table 2-2. BUS OPERATION

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0~Q7	Q8~Q15
	CE#	WE#	OE#										
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)	x
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2h	x
Read Silicon ID MX29LV321DT	L	H	L	x	x	V_{hv}	x	L	x	L	H	A7h	22h
Read Silicon ID MX29LV321DB	L	H	L	x	x	V_{hv}	x	L	x	L	H	A8h	22h
Read Indicator Bit (Q7) For Security Sector	L	H	L	x	x	V_{hv}	x	L	x	H	H	99h or 19h (Note2)	x

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: 99h. Factory unlocked code: 19h.
3. AM: MSB of address.

FUNCTIONAL OPERATION DESCRIPTION

READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toa timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in Figure 1 on Page 32. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Word Data (I/O) pins will drive data.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW, the outermost two boot sectors are protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these two outermost sectors revert to their previously protected/unprotected status.

ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program word locations directly. Typically, this mode provides a 30% reduction in overall programming times. During accelerated programming, the current drawn from the WP#/ACC pin is no more than Icp1.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

The system can apply Vhv to the RESET# pin to place the device in Temporary Unprotect mode. In this mode, previously protected sectors can be programmed/erased just as though they were unprotected. The device returns to normal operation once Vhv is removed from the RESET# pin and previously protected sectors will once again be protected.

SECTOR GROUP PROTECT OPERATION

The MX29LV321D T/B provides user programmable protection against program/erase operations for selected sectors. Most sectors cannot protected individually. Instead, they are bound in groups of four or less called Sector-Groups. Protection is available for individual Sector-Groups, which includes all member sectors. Boot sectors are the exception to this rule as they are assigned unique Sector-Group addresses and can be protected individually without protecting any adjacent sectors or Sector-Groups. The three sectors adjacent to the boot sectors form a non-standard Sector-Group. Please refer to Table 1-1 and Table 1-2 which show all Sector-Group assignments.

During the protection operation, the sector address of any sector within a Sector-Group may be used to specify the Sector-Group being protected.

There are two methods available to protect Sector-Groups. The first and preferred method is activated by applying Vhv on the RESET# pin and following the timing in Figure 13 and the algorithm shown in Figure 14. This is a command operation that can be performed either on an external programmer or in-circuit by the system controller. The second method is strictly a bus operation and is entered by asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for more details on this method.

CHIP UNPROTECT OPERATION

The Chip Unprotect operation unprotects all sectors within the device. It is standard procedure and highly recommended to protect all Sector-Groups prior using the Chip Unprotect operation. This will prevent possible damage to the Sector-Group protection logic. All Sector Groups are unprotected when shipped from the factory, so this operation is only necessary if the user has previously protected any Sector-Groups and wishes to unprotect them now.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

CHIP UNPROTECT OPERATION (cont'd)

MX29LV321D T/B provides two methods for unprotecting the entire chip. The first and preferred method is entered by applying Vhv on RESET# pin and following the timing diagram in Figure 13 and using the algorithm shown in Figure 15.

The second method is entered by asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for more details on this method.

AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see "AUTOMATIC SELECT COMMAND SEQUENCE" in the "COMMAND OPERATIONS" section for details of equivalent command operations that do not require the use of Vhv.

SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A20 to A12, address pins A6 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q0 to Q7.

READ SILICON ID MX29LV321DT CODE

To verify the Silicon ID MX29LV321DT Code, the system performs a READ OPERATION with A9 raised to Vhv, address pins A6 & A1 held LOW, and address pin A0 held HIGH. The MX29LV321DT code of A7h should be present on data bits Q0 to Q7, Q15 to Q8 will output the value 22h.

READ SILICON ID MX29LV321DB CODE

To verify the Silicon ID MX29LV321DB Code, the system performs a READ OPERATION with A9 raised to Vhv, address pins A6 & A1 held LOW, and address pin A0 held HIGH. The MX29LV321DT code of A8h should be present on data bits Q0 to Q7, Q15 to Q8 will output the code 22h.

READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9raised to Vhv, address pin A6 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h will be present on data bits Q0 to Q7. Otherwise, the factory unlocked code of 19h will be present.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. If any command sequence is interrupted or given an invalid command, the device immediately returns to Read mode.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than Vlko. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than Vlko and write cycles are ignored until Vcc is greater than Vlko. The system must provide proper signals on control pins after Vcc rises above Vlko to avoid unintentional program or erase operations.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, the MX29LV321D T/B is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

COMMAND OPERATIONS

TABLE 3. MX29LV321D T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select				Enter Security Sector Region Enable
				Manifacture ID	Device ID	Sector Factory	Sector Protect Verify	
1st Bus Cycle	Addr	Addr	XXX	555	555	555	555	555
	Data	Data	F0	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	2AA	2AA	2AA	2AA
	Data			55	55	55	55	55
3rd Bus Cycle	Addr			555	555	555	555	555
	Data			90	90	90	90	88
4th Bus Cycle	Addr			X00	X01	X03	(Sector)X02	
	Data			C2h	ID	99/19	00/01	
5th Bus Cycle	Addr							
	Data							
6th Bus Cycle	Addr							
	Data							

Command		Exit Security Sector	Program	Chip Erase	Sector Erase	CFI Read	Erase Suspend	Erase Resume
1st Bus Cycle	Addr	555	555	555	555	55	XXX	XXX
	Data	AA	AA	AA	AA	98	B0	30
2nd Bus Cycle	Addr	2AA	2AA	2AA	2AA			
	Data	55	55	55	55			
3rd Bus Cycle	Addr	555	555	555	555			
	Data	90	A0	80	80			
4th Bus Cycle	Addr	XXX	Addr	555	555			
	Data	00	Data	AA	AA			
5th Bus Cycle	Addr			2AA	2AA			
	Data			55	55			
6th Bus Cycle	Addr			555	Sector			
	Data			10	30			

Notes:
1. ID 22A7h(Top), 22A8h(Bottom).
2. It is not allowed to adopt any other code which is not in the above command definition table.

COMMAND OPERATIONS (cont'd)

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The MX29LV321D T/B provides the user the ability to program the memory array in Word mode. As long as the users enters the correct cycle defined in the Table 3 (including 2 unlock cycles and the A0h program command), any word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7*1	Q6*1	Q5	RY/BY# *2
In progress	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: When an attempt is made to program a protected sector, the program operation will abort thus preventing any data changes in the protected sector. Q7 will output complement data and Q6 will toggle briefly (1us or less) before aborting and returning the device to Read mode.

*2: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors.

COMMAND OPERATIONS (cont'd)

SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3 (note 1)	Q2	RY/BY# (note 2)
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceeded time limit	0	Toggling	1	1	Toggling	0

Note :
1. The Q3 status bit is the time-out indicator. When Q3=0, the time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
2. RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector(s), the program operation will abort thus preventing any data changes in the protected sector(s). Q7 will output its complement data and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode). When a sector has been completely erased, Q2 stops toggling at the sector even when the device is still in erase operation for remaining selected sectors. At that circumstance, Q2 will still toggle when device is read at any other sector that remains to be erased.

COMMAND OPERATIONS (cont'd)

CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#*1
In progress	0	Toggling	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

*1: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

SECTOR ERASE SUSPEND

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until Tready1 time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector(s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

COMMAND OPERATIONS (cont'd)

SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 4ms interval between Ease Resume and the next Erase Suspend command. If the user enters an infinite suspend-resume loop, or suspend-resume exceeds 1024 times, erase times will increase dramatically.

AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Erase-Suspended Read mode, or CFI mode, the user can issue the Automatic Select command shown in Table 3 (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector-Group protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active).

Another way to enter Automatic Select mode is to use one of the bus operations shown in Table 2-2. BUS OPERATION. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address (Hex)	Data (Hex)	Representation
Manufacturer ID	X00	C2	
Device ID	X01	22A7/22A8	Top/Bottom Boot Sector
Secured Silicon	X03	99/19	Factory locked/unlocked
Sector Protect Verify	(Sector address) X 02	00/01	Unprotected/protected

After entering automatic select mode, no other commands are allowed except the reset command.

COMMAND OPERATIONS (cont'd)

READ MANUFACTURER ID OR DEVICE ID

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JEDEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

The Device ID is a unique hexadecimal number assigned by the manufacturer for each one of the flash devices made by that manufacturer.

The above two ID types are stored in a 16-bit register on the flash device -- eight bits for each ID. This register is normally read by the user or by the programming machine to identify the manufacturer and the specific device.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins. Performing a read operation with A1 LOW and A0 HIGH will cause the device to output the Device ID.

SECURITY SECTOR LOCK STATUS

After entering Automatic Select mode, the customer can check the lock status of the Security Sector by performing a read operations with A0 and A1 held HIGH. If the code 99h is read from data pins Q7 to Q0, the sector has been locked at the factory. If the code 19h is read, the sector has not been locked at the factory.

VERIFY SECTOR GROUP PROTECTION

After entering Automatic Select mode, performing a read operation with A1 held HIGH and A0 held LOW and the address of the sector to be checked applied to A20 to A12, data bit Q0 will indicate the protected status of the addressed sector. If Q0 is HIGH, the sector is protected. Conversely, if Q0 is LOW, the sector is unprotected.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra memory space of 32KWords in length. The Security Sector can be locked by the factory prior to shipping, or it can be locked by the customer later.

FACTORY LOCKED: SECURITY SECTOR PROGRAMMED AND PROTECTED AT THE FACTORY

In a factory locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 8-word ESN in the security region. In bottom boot devices, the ESN occupies addresses 00000h to 00007h in word mode. In top boot devices, the EXN occupies addresses 1F800h to 1F8007h in word mode.

COMMAND OPERATIONS (cont'd)

CUSTOMER LOCKABLE: SECURITY SECTOR NOT PROGRAMMED OR PROTECTED AT THE FACTORY

When the security feature is not required, the Security Sector can provide an extra sector of memory, which can be read, programmed, and erased with the same endurance limitations specified for normal sectors.

Two methods are available for protecting the Security Sector. Note that once the Security Sector is protected, there is NO way to unprotect it and its contents can no longer be altered.

The first protection method requires writing the three-cycle Enter Security Region command followed by the use of the Sector-Group protect algorithm as illustrated in Figure 14 with the following exception: the RESET# pin may be at either Vih or Vhv. Unlike normal Sector-Groups, which do require Vhv on the RESET# pin, the Security Sector may be permanently locked in-circuit without the use of high voltage.

The second protection method also uses the three-cycle Enter Security Region command, but uses bus operations that applies Vhv to the A9 and OE# pins with A6, CE#, and WE# held LOW and the SA address applied to A20 to A12. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for more details on using this method.

After the Security Sector is locked and verified, the system must write an Exit Security Sector Region command, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

ENTER AND EXIT SECURITY SECTOR

The device allows the user to access the extra 64K-Byte sector identified as the Security Sector, which may contain a random, 128-bits electronic serial number (ESN), or it may contain user data.

To access the Security Sector, the user must issue a three-cycle "Enter Security Sector" command sequence. To exit the Security Sector and return to normal operation, the user issues the four-cycle "Exit Security Sector" command. Before issuing the "Exit Security Sector" command, please ensure the entering of security sector region.

COMMAND OPERATIONS (cont'd)

RESET OPERATION

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

COMMON FLASH MEMORY INTERFACE (CFI) MODE

QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE

MX29LV321D T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, word configuration, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command, 98H, to address 55H(word mode) any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode. The CFI unused area is Macronix's reserved.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code	17	0000
	18	0000
Address for alternate algorithm extended query table	19	0000
	1A	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word write, 2^n us	1F	0004
Typical timeout for maximum-size buffer write, 2^n us	20	0000
Typical timeout per individual block erase, 2^n ms	21	000A
Typical timeout for full chip erase, 2^n ms	22	0000
Maximum timeout for word write, 2^n times typical	23	0005
Maximum timeout for buffer write, 2^n times typical	24	0000
Maximum timeout per individual block erase, 2^n times typical	25	0004
Maximum timeout for chip erase, 2^n times typical	26	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Data (h)
Device size = 2^n in number of bytes	27	0016
Flash device interface description (01=asynchronous x16)	28	0001
	29	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	0000
	2B	0000
Number of erase regions within device	2C	0002
Index for Erase Bank Area 1 [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256-bytes	2D	0007
	2E	0000
	2F	0020
	30	0000
Index for Erase Bank Area 2	31	003E
	32	0000
	33	0000
	34	0001
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0031
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0000
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0004
Temporary sector unprotect (1=supported)	48	0001
Sector protect/Chip unprotect scheme	49	0004
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported)	4C	0000
Minimum ACC (acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	00A5
Maximum ACC (acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	00B5
Top/Bottom boot block indicator 02h=bottom boot device 03h=top boot device	4F	0002/ 0003

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0V
	VI/O	-0.5V to +4.0V
	RESET#, A9 and OE#	-0.5V to +10.5V
	The other pins	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

Note:
1. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

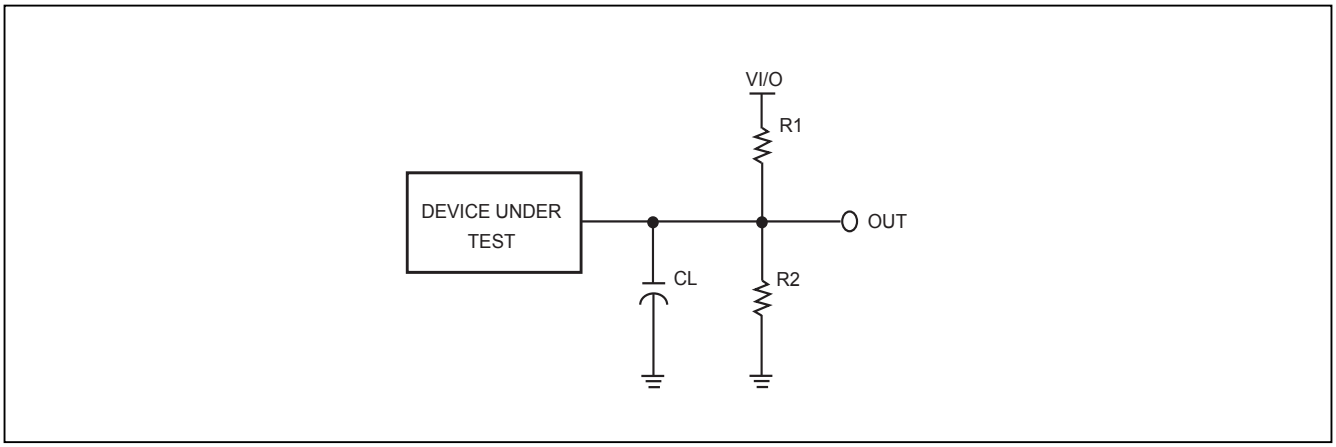
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	VCC range	+2.7V to 3.6V
	VI/O range	+1.65V to 3.6V

DC CHARACTERISTICS

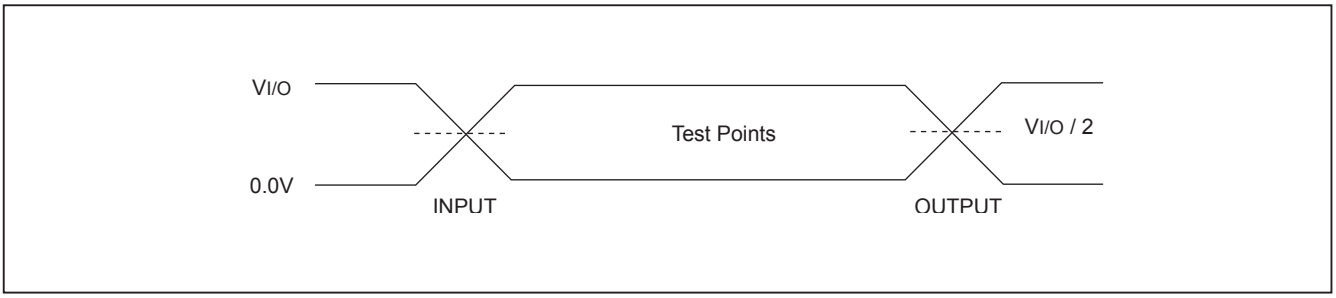
Symbol	Description	Min.	Typ.	Max.	Remark
Iilk	Input Leak			± 1.0uA	
Iilk9	A9 Leak			35uA(0~70°C)/ 45uA(-40~85°C)	A9=10.5V
Iolk	Output Leak			± 1.0uA	
Icr1	Read Current (5MHz)		10mA	16mA	CE#=Vil, OE#=Vih
Icr2	Read Current (1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		5uA	15uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		5uA	15uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		5uA	15uA	
Icp1	Accelerated Pgm Current, WP#/Acc pin		5mA	10mA	CE#=Vil, OE#=Vih,
Icp2	Accelerated Pgm Current, Vcc pin		15mA	30mA	CE#=Vil, OE#=Vih,
Vil	Input Low Voltage	-0.1V		0.3 x VI/O	
Vih	Input High Voltage	0.7 x VI/O		VI/O+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/Accelerated Program/Auto Select/Temporary Unprotect	9.5V		10.5V	
Vol	Output Low Voltage			0.15 x VI/O	Iol=100uA
Voh	Output High Voltage	0.85 x VI/O			Ioh=-100uA
Vlko	Low Vcc Lock-out Voltage	2.3V		2.5V	

SWITCHING TEST CIRCUITS



Test Condition
Output Load Capacitance,CL : 30pF(90ns)
R1=R2=25KΩ
Rise/Fall Times : 5ns
In/Out reference levels :VI/O / 2

SWITCHING TEST WAVEFORMS



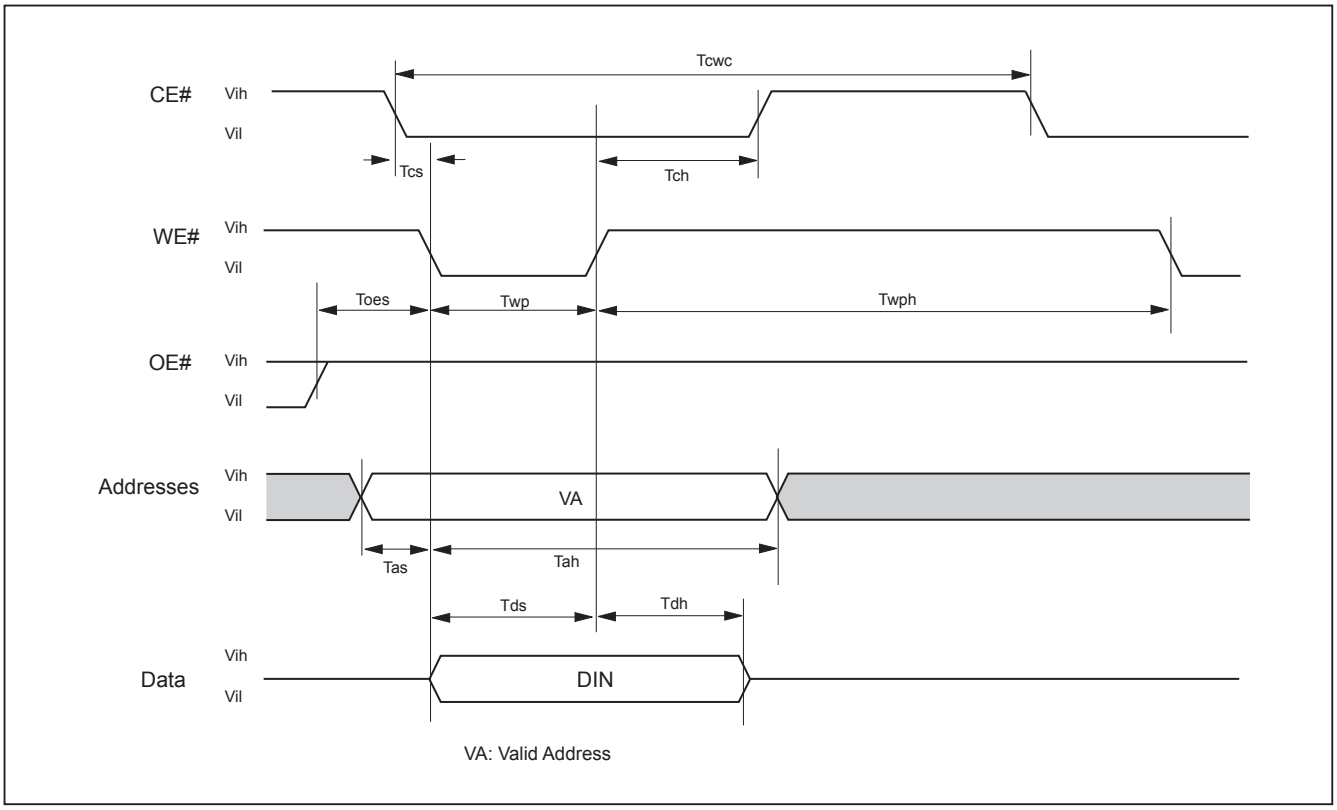
AC CHARACTERISTICS

Symbol	Description		Min.	Typ.	Max.	Unit
Taa	Valid data output after address				90	ns
Tce	Valid data output after CE# low				90	ns
Toe	Valid data output after OE# low				40	ns
Tdf	Data output floating after OE# high				30	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			ns
Trc	Read period time		90			ns
Tsrw	Latency Between Read and Write Operation (*Note 1)		45			ns
Twc	Write period time		90			ns
Tcwc	Command write period time		90			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45			ns
Tds	Data setup time		45			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		200			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		45			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		35			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation			11	360	us
Twhwh1	Acc program operation (Word/Byte)			7	210	us
Twhwh2	Sector erase operation			0.7		sec
Tbal	Sector add hold time				50	us

* Note 1: Sampled only, not 100% tested.

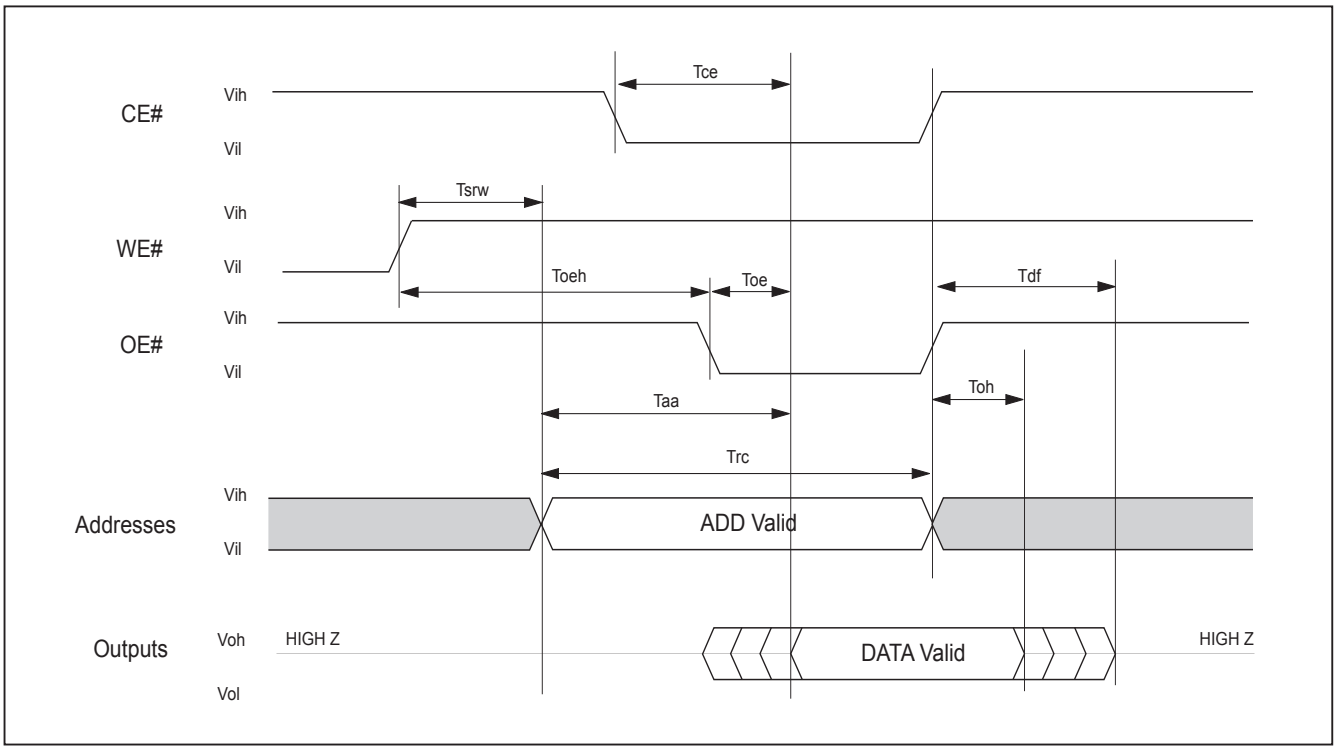
WRITE COMMAND OPERATION

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

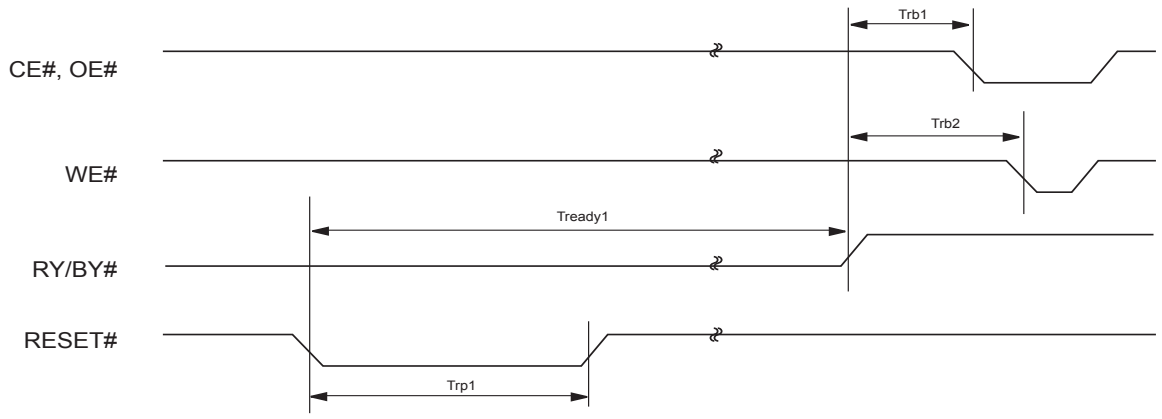
Figure 2. READ TIMING WAVEFORMS



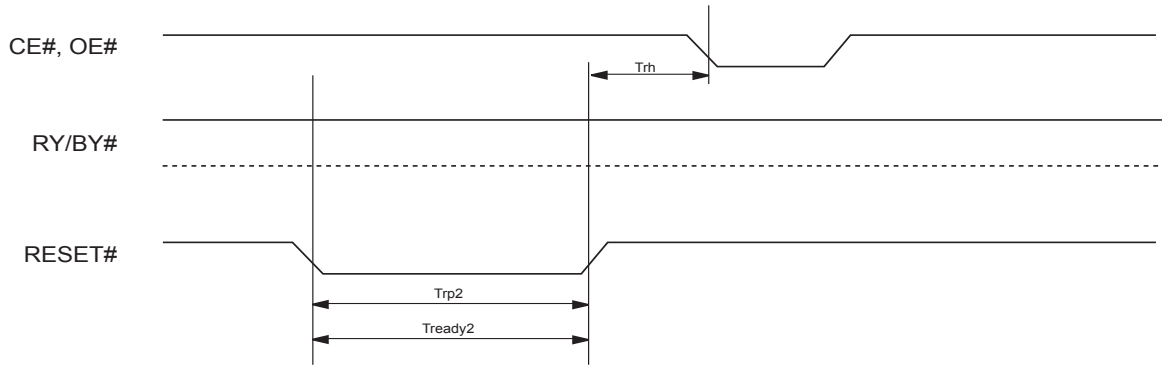
AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	70	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



Reset Timing during Automatic Algorithms



Reset Timing NOT during Automatic Algorithms

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

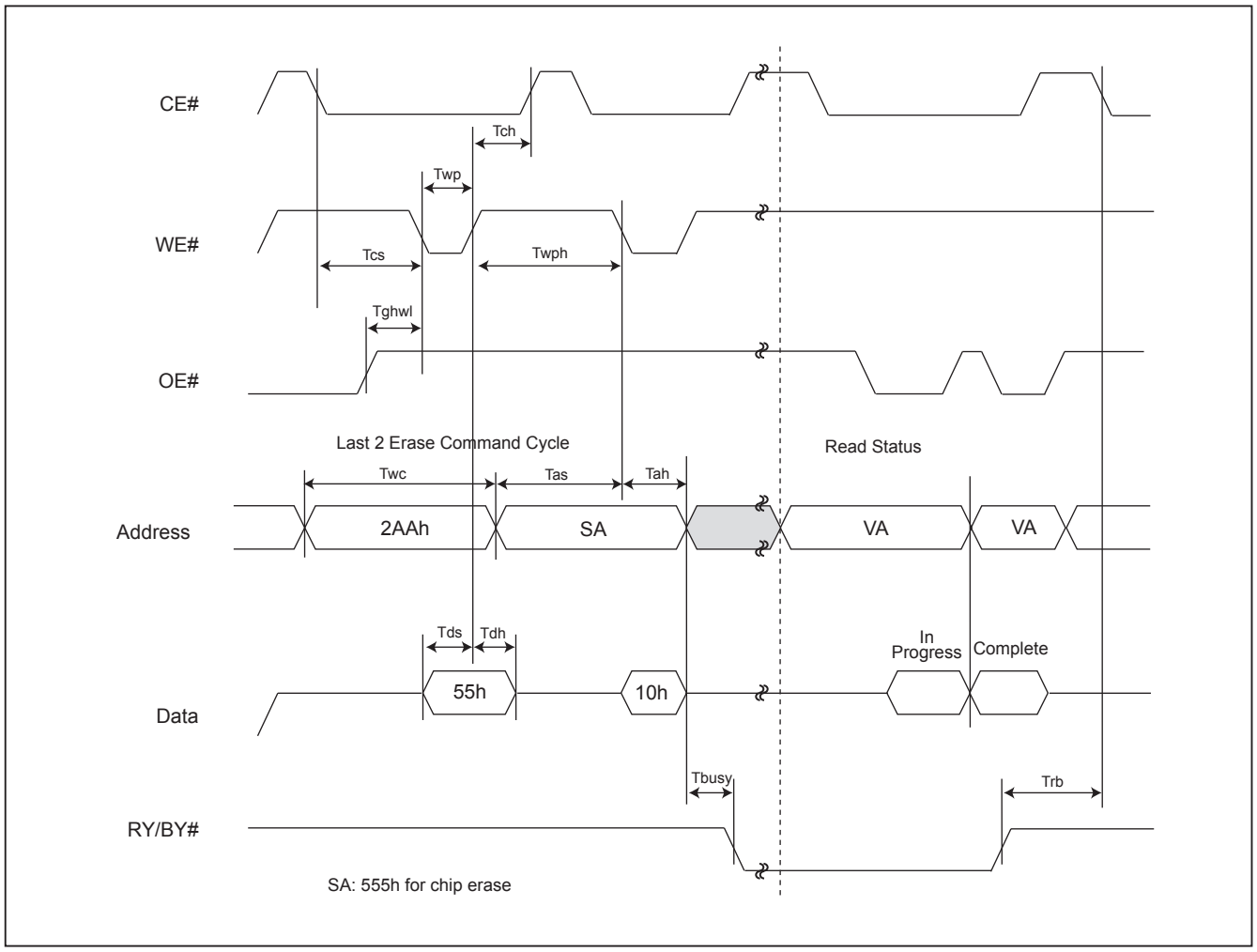


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

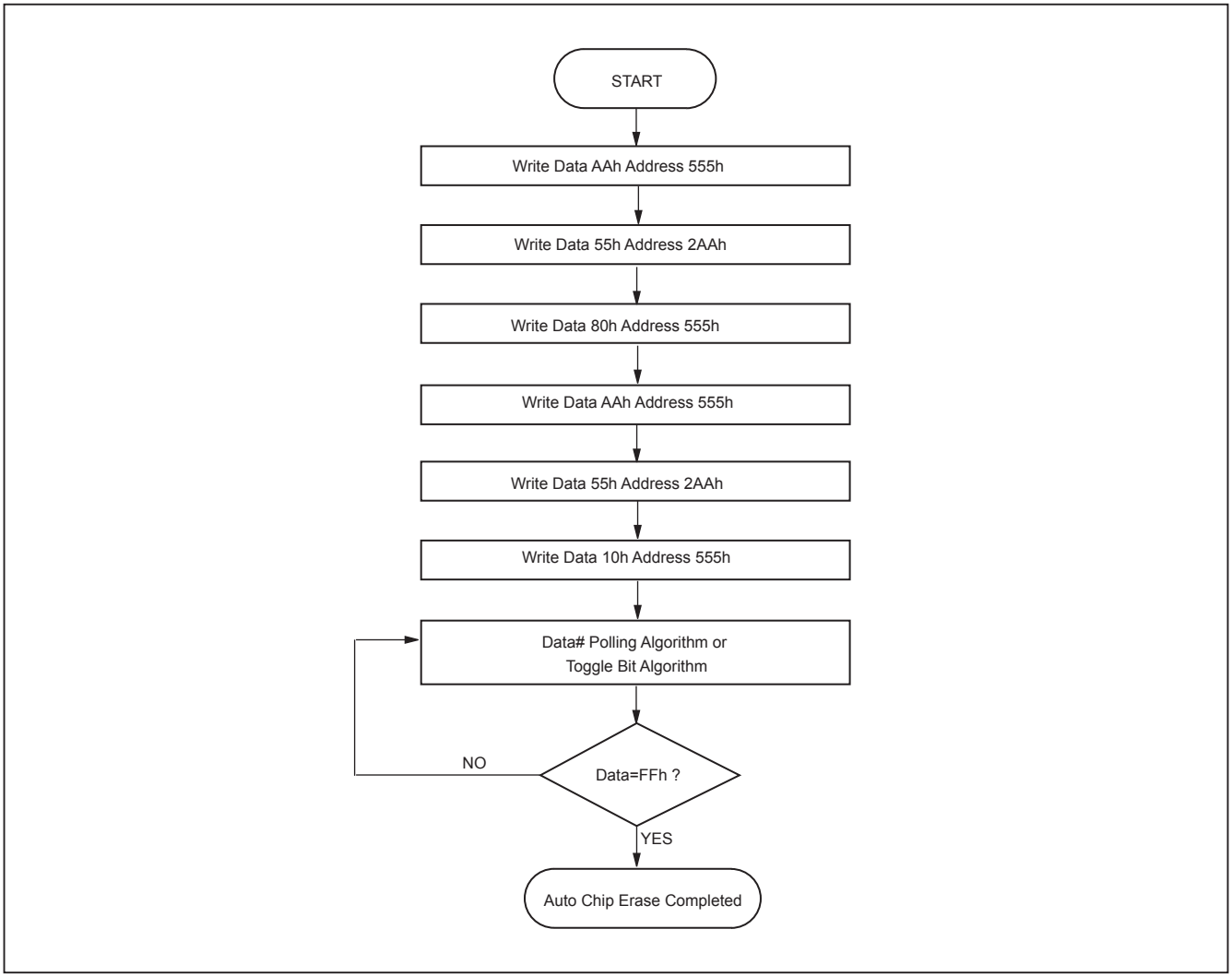


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

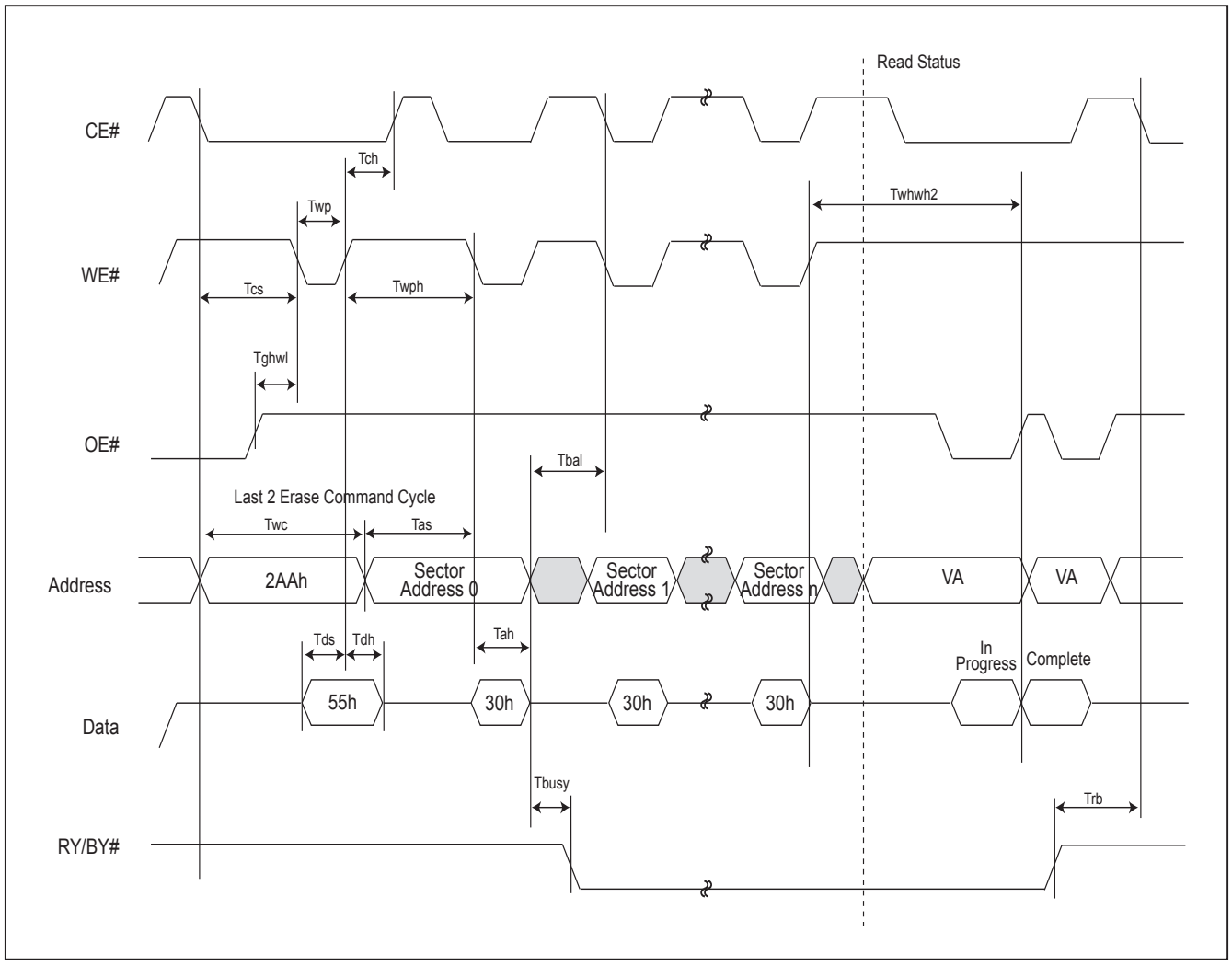


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

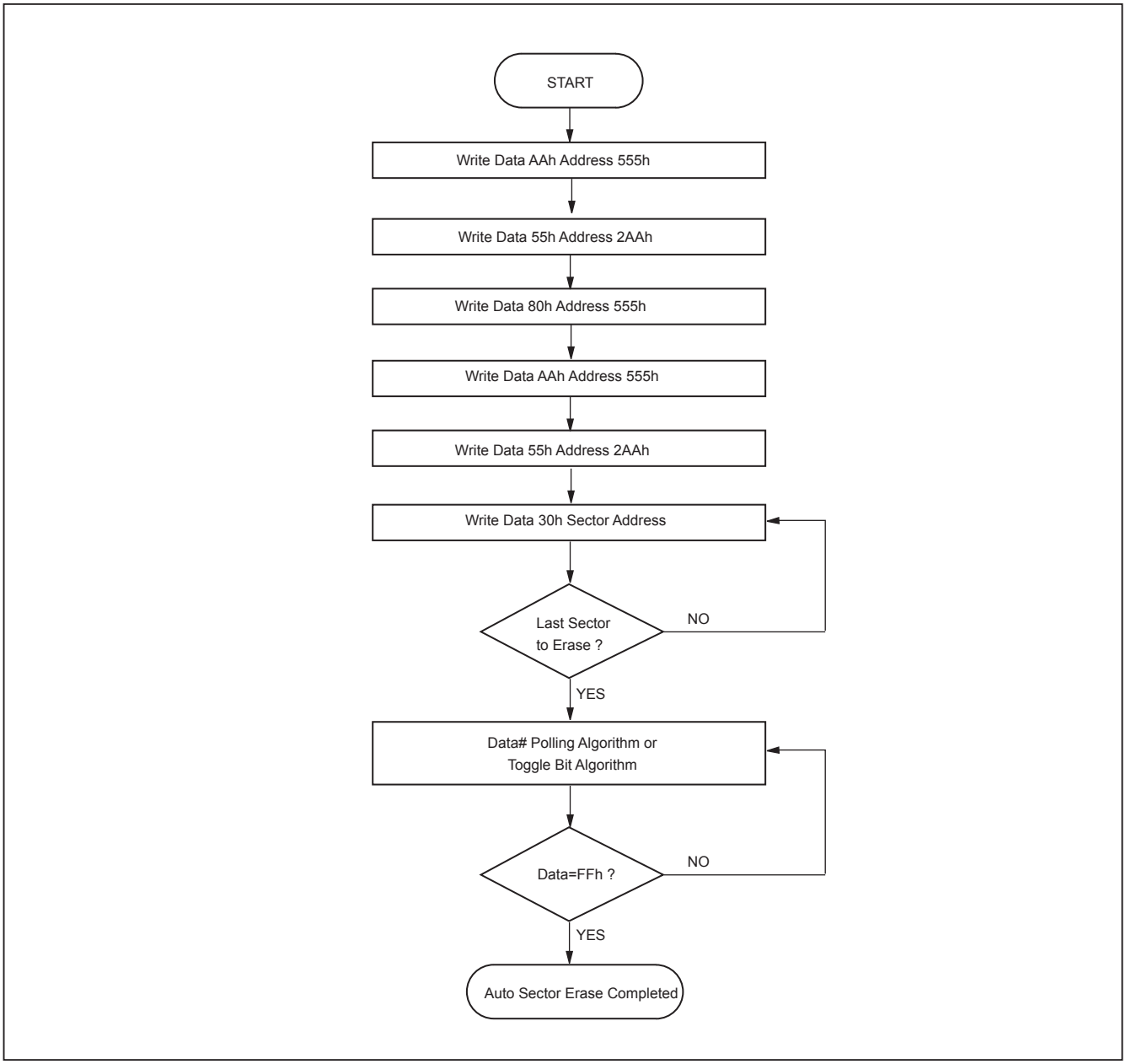


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

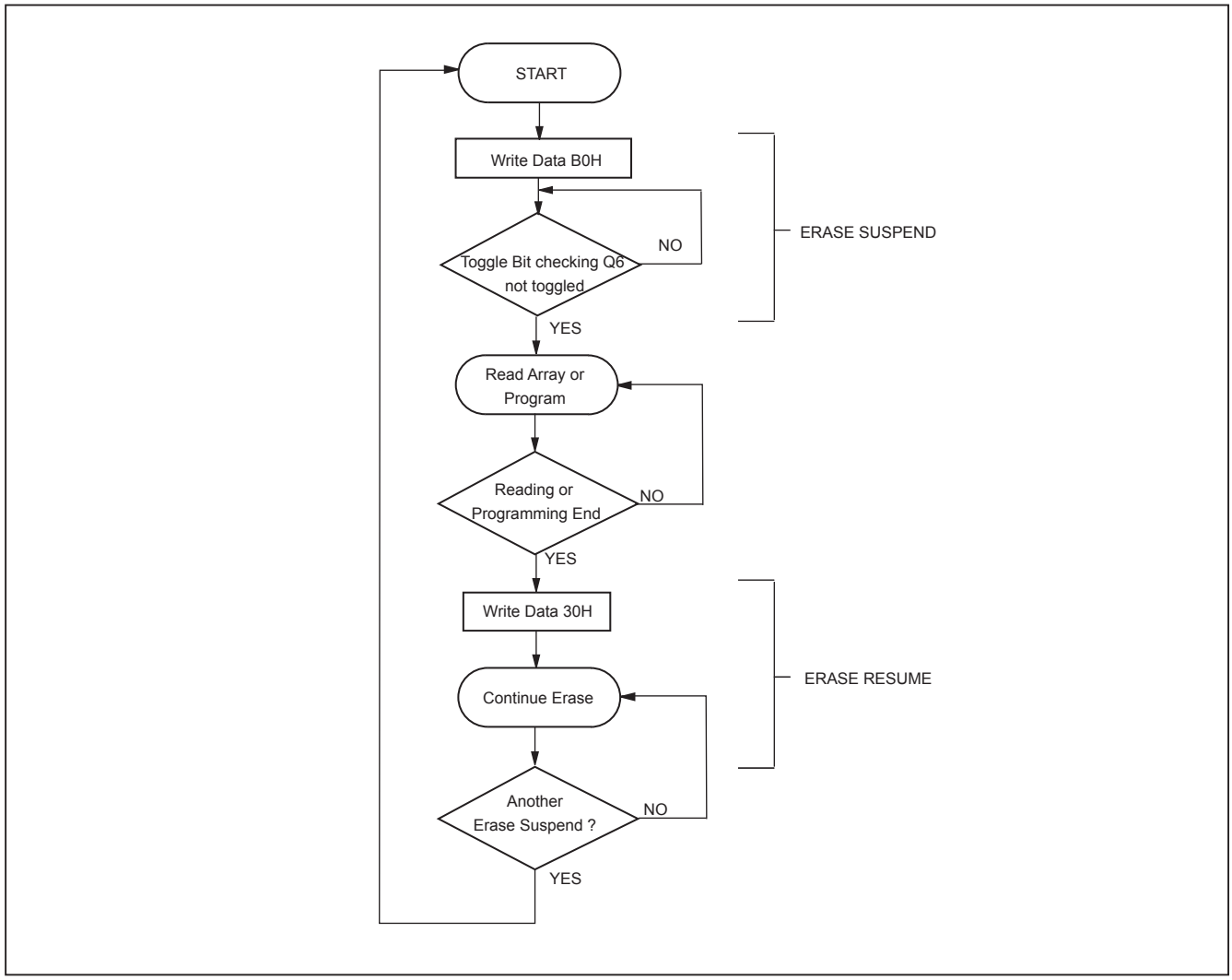


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORM

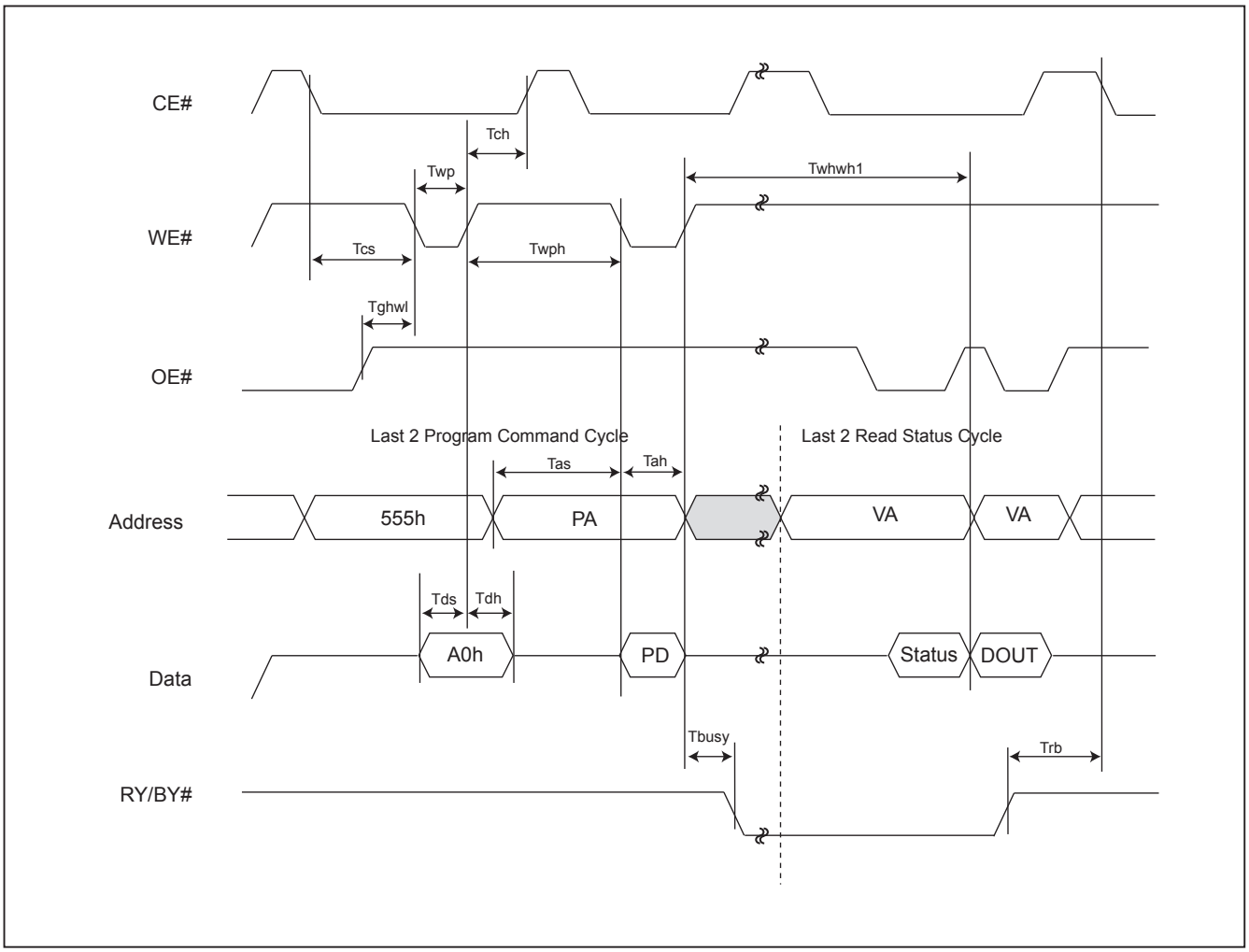


Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM

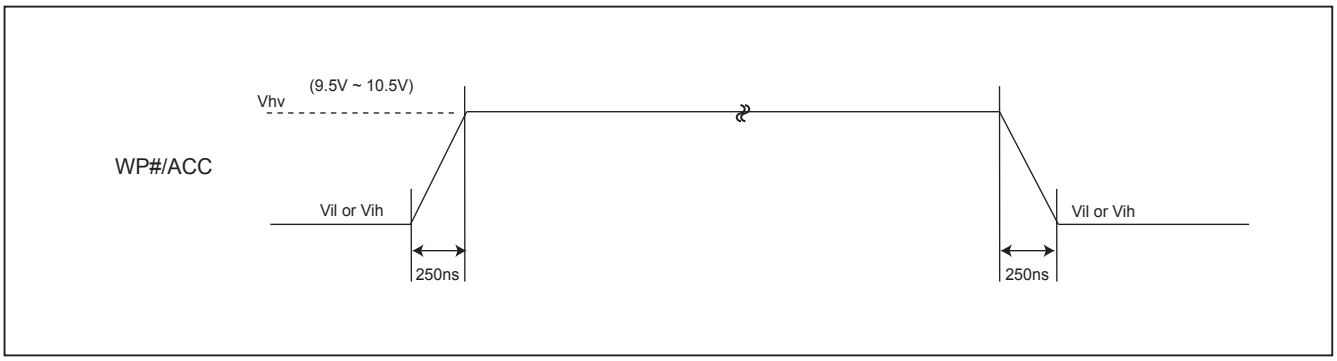


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

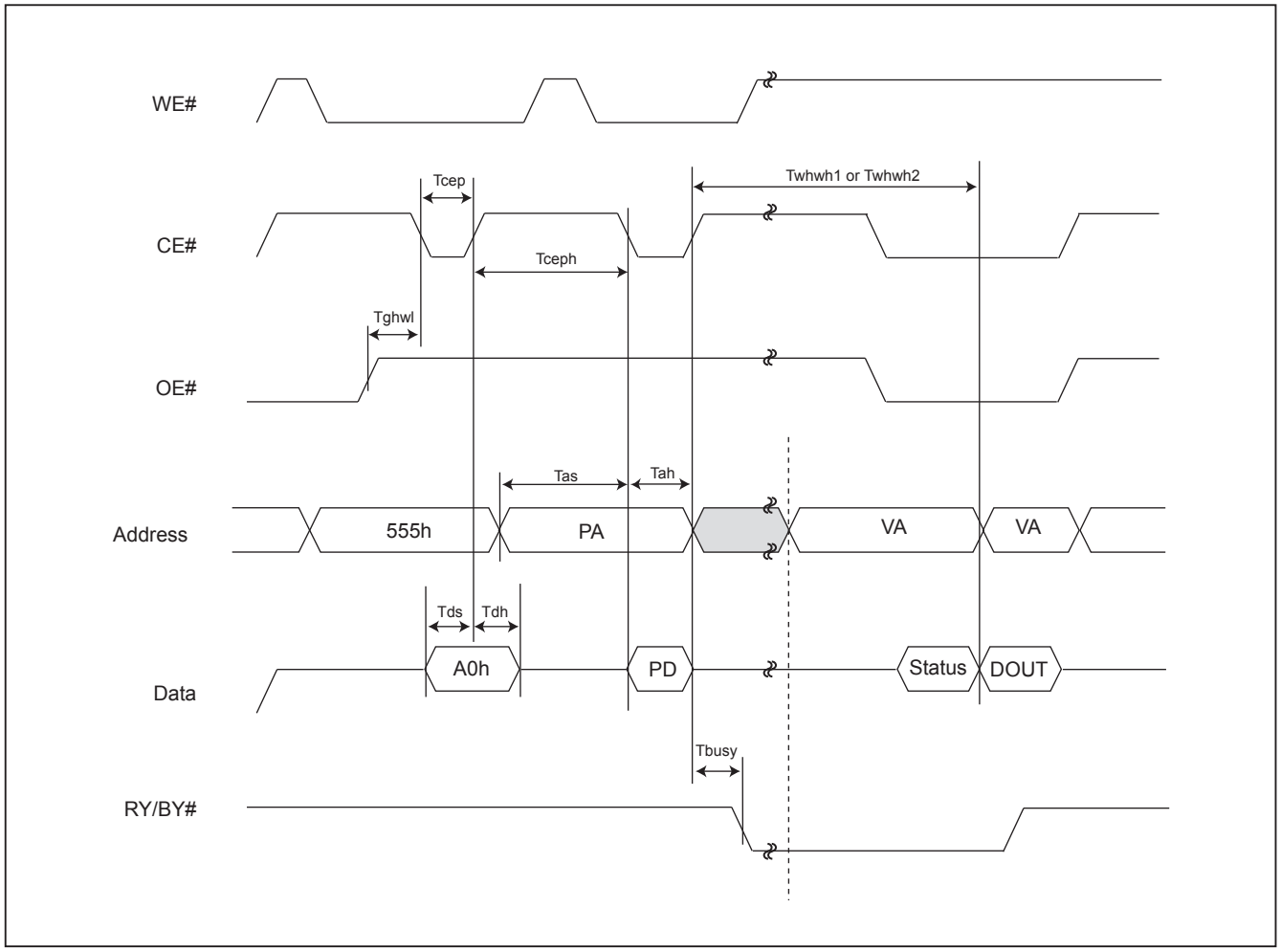
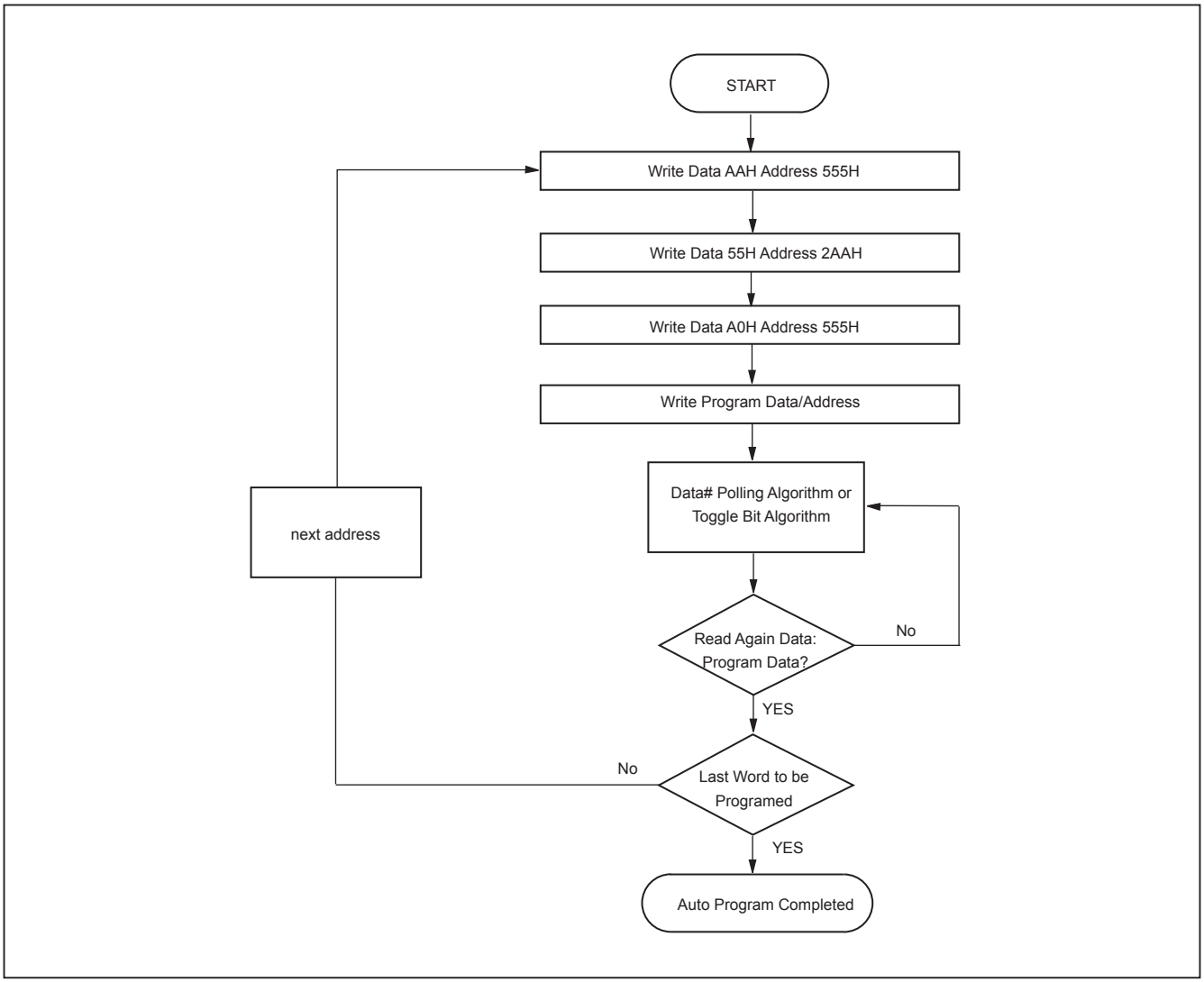


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 13. Sector Group Protect/Chip Unprotect Waveform (RESET# Control)

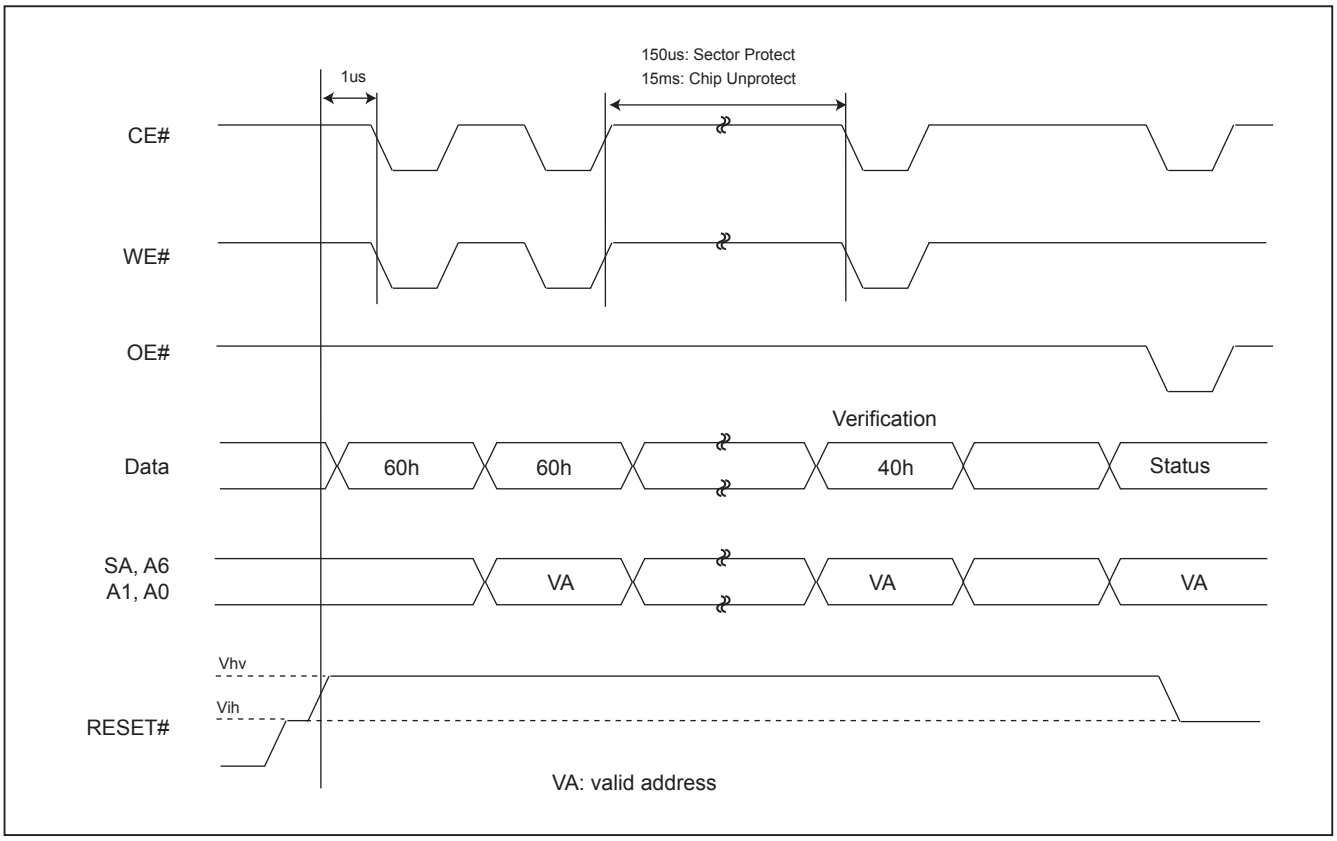


Figure 14. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv

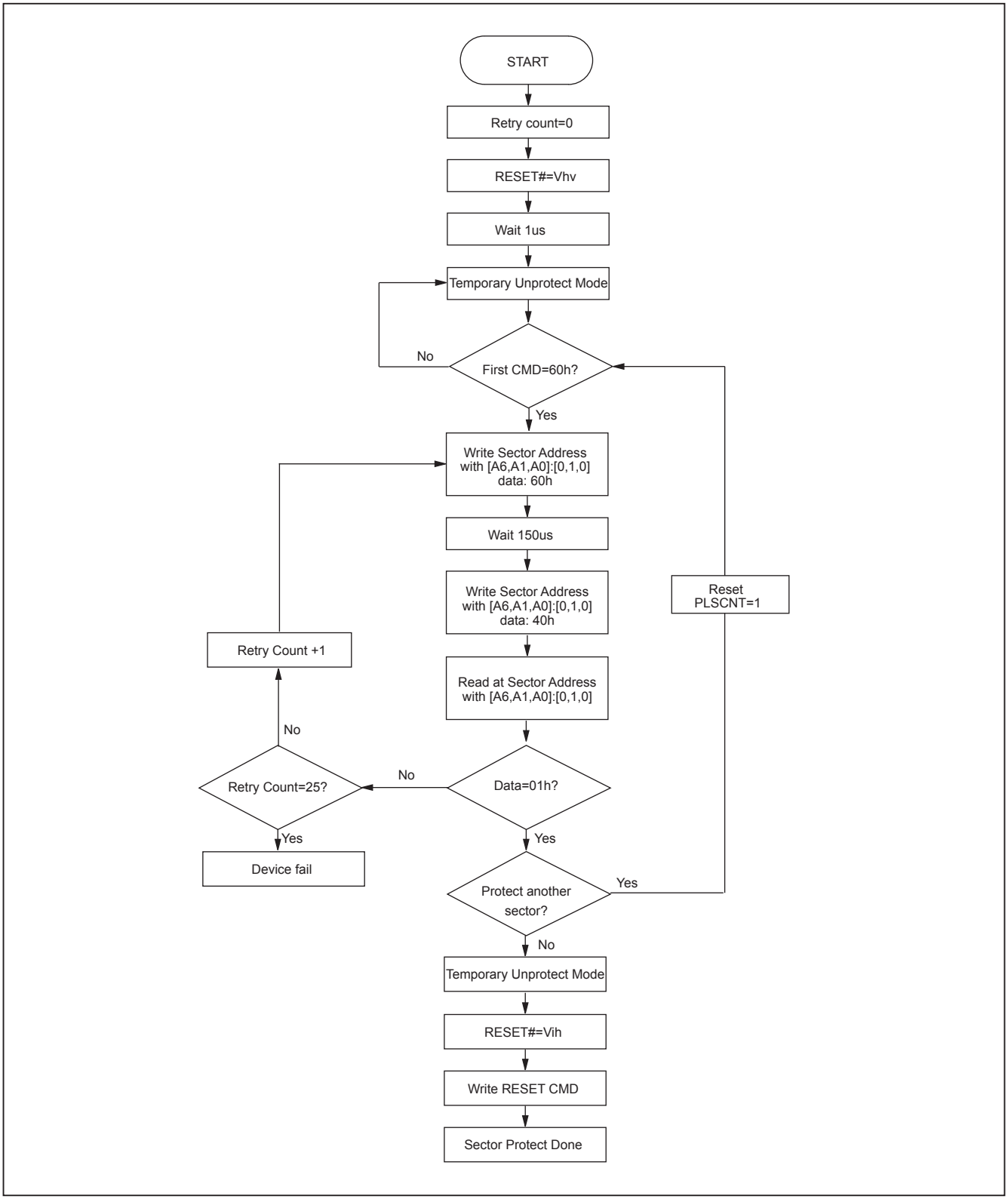


Figure 15. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

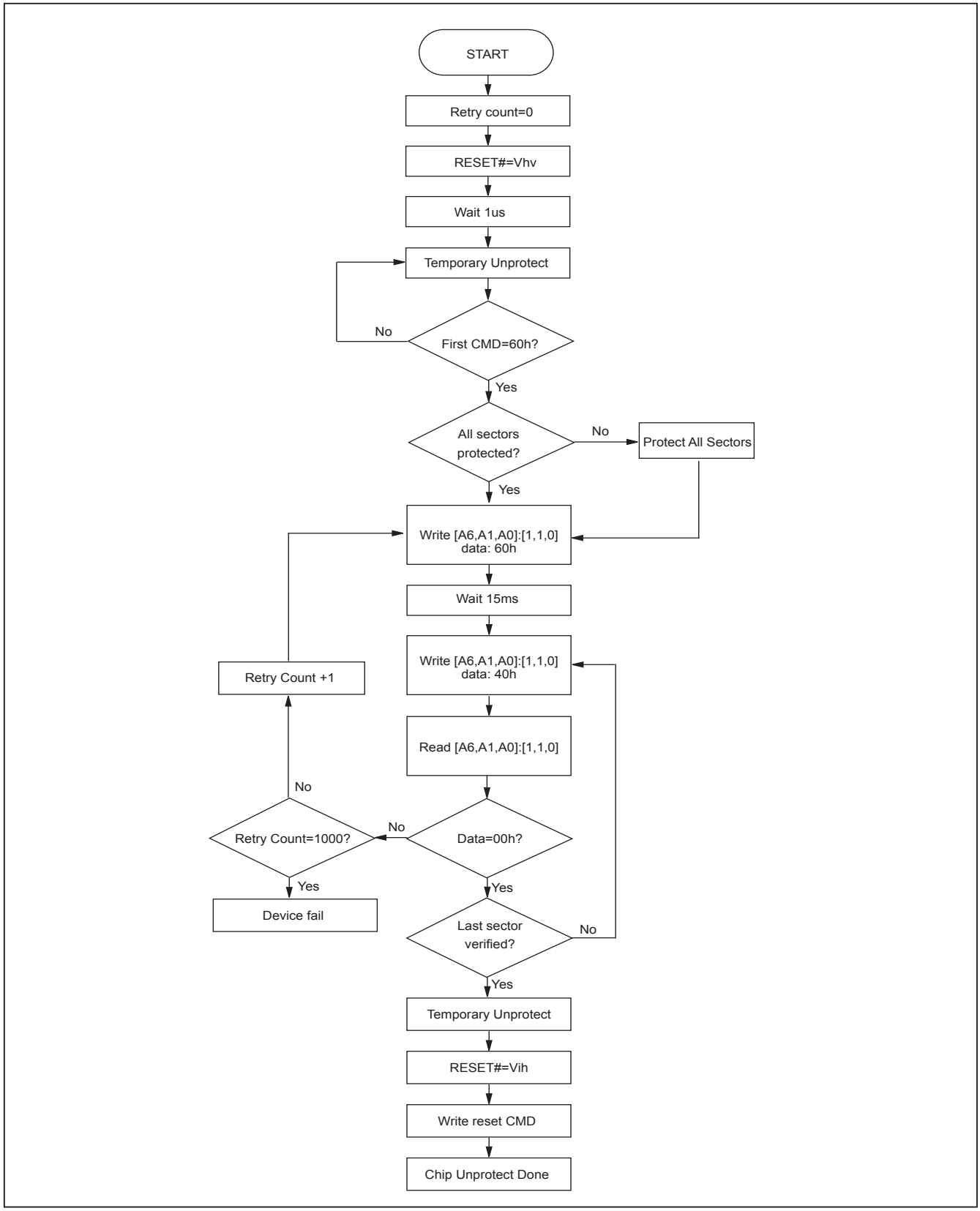


Table 5. TEMPORARY SECTOR GROUP UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 16. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

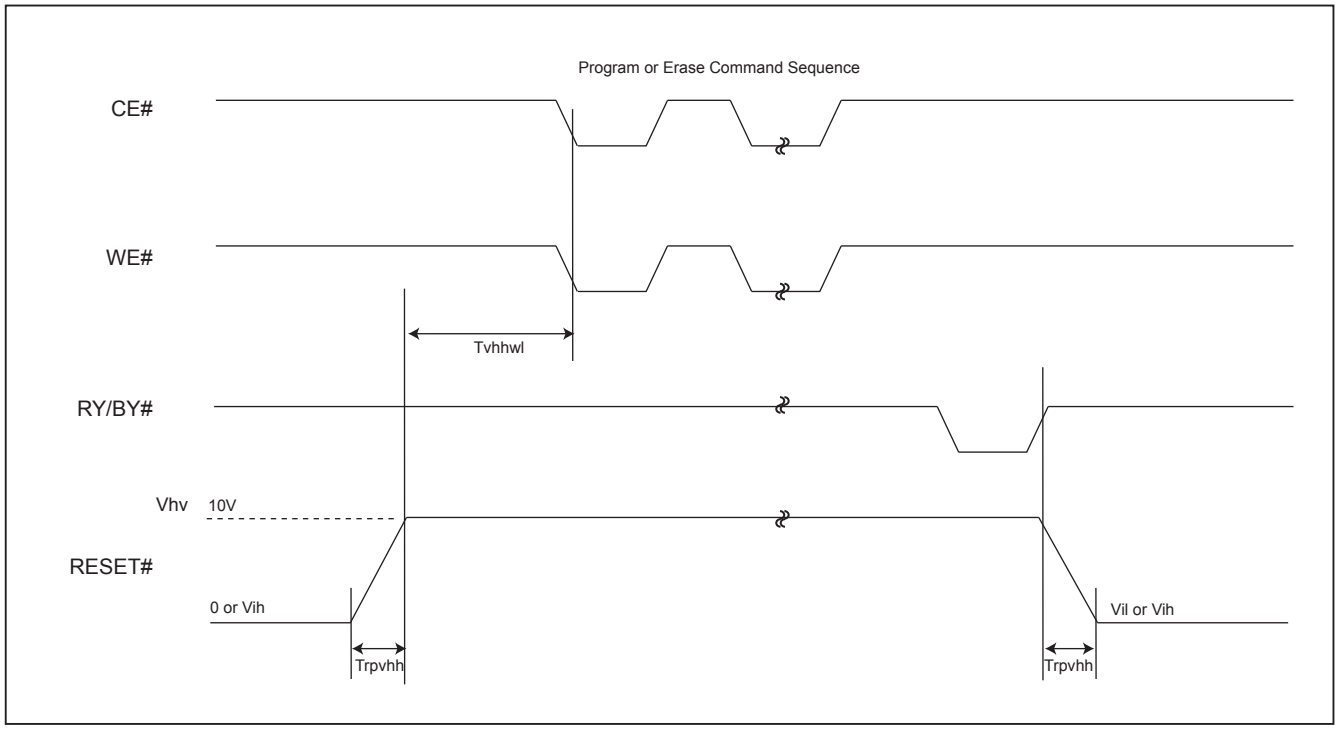
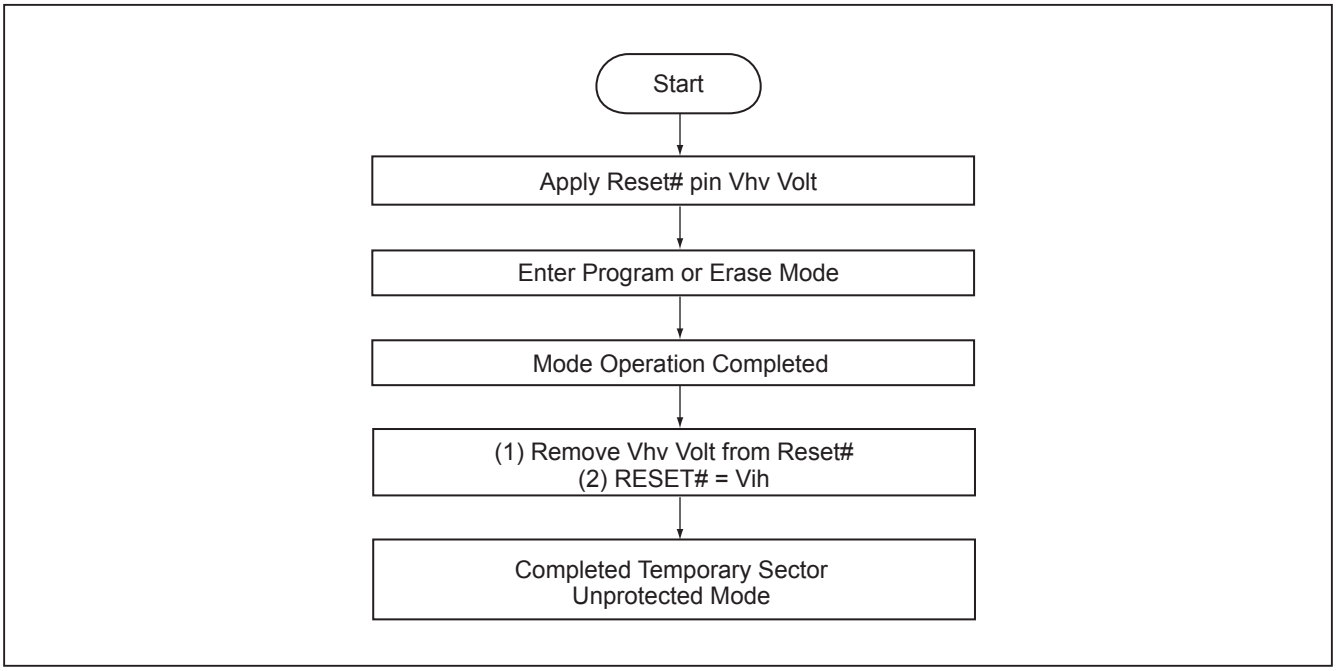
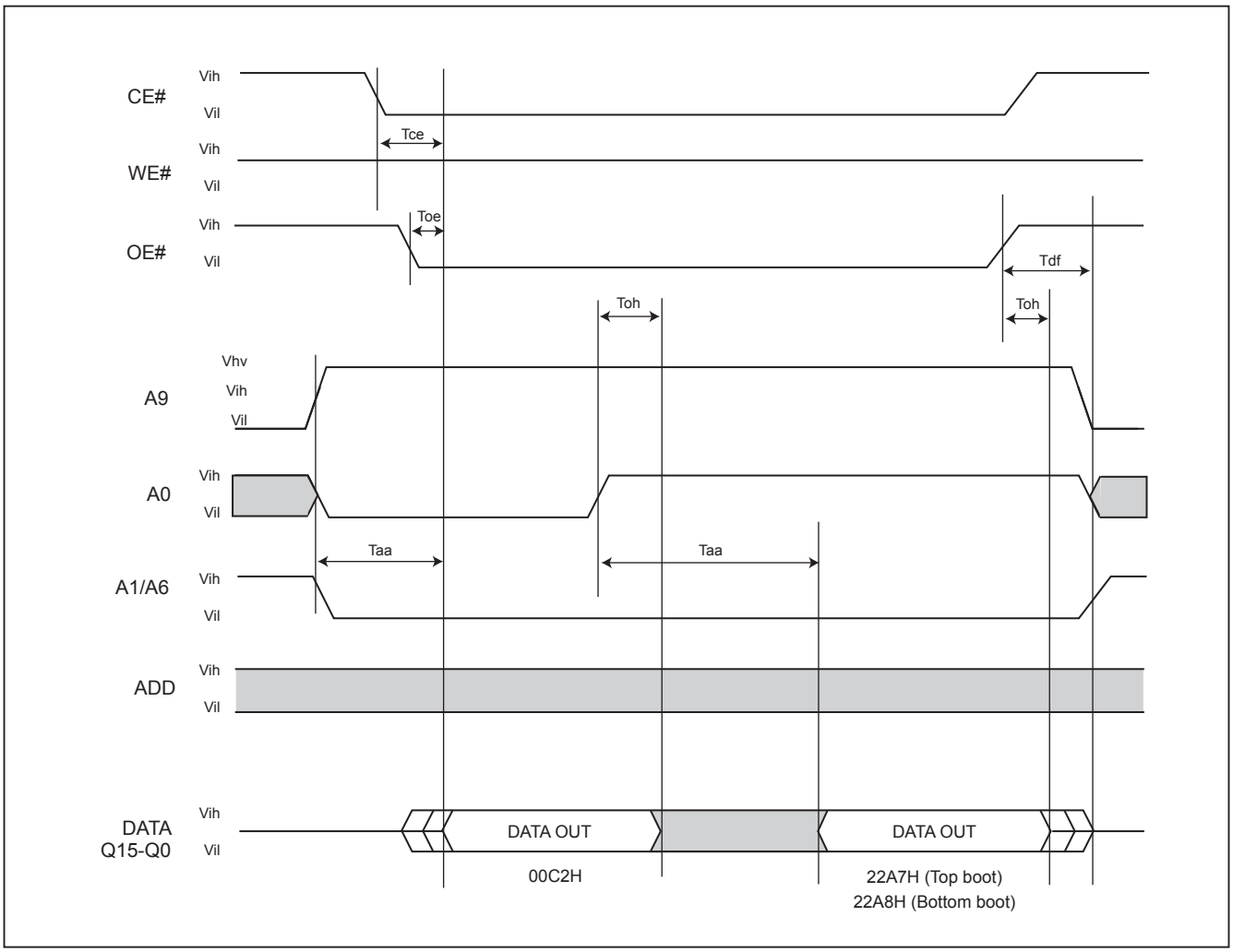


Figure 17. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=9.5~10.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 18. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 19. DATA# POLLING TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM)

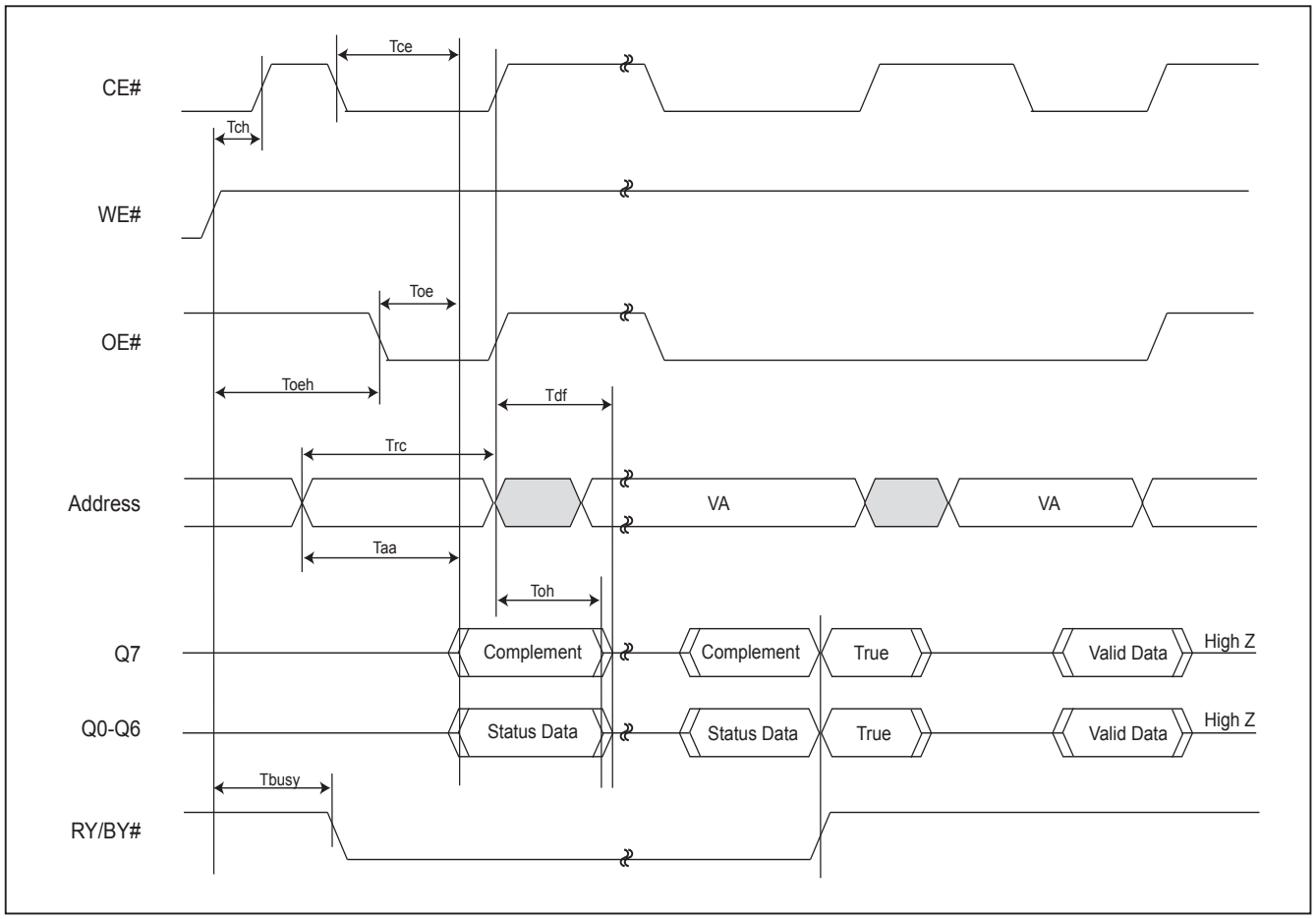
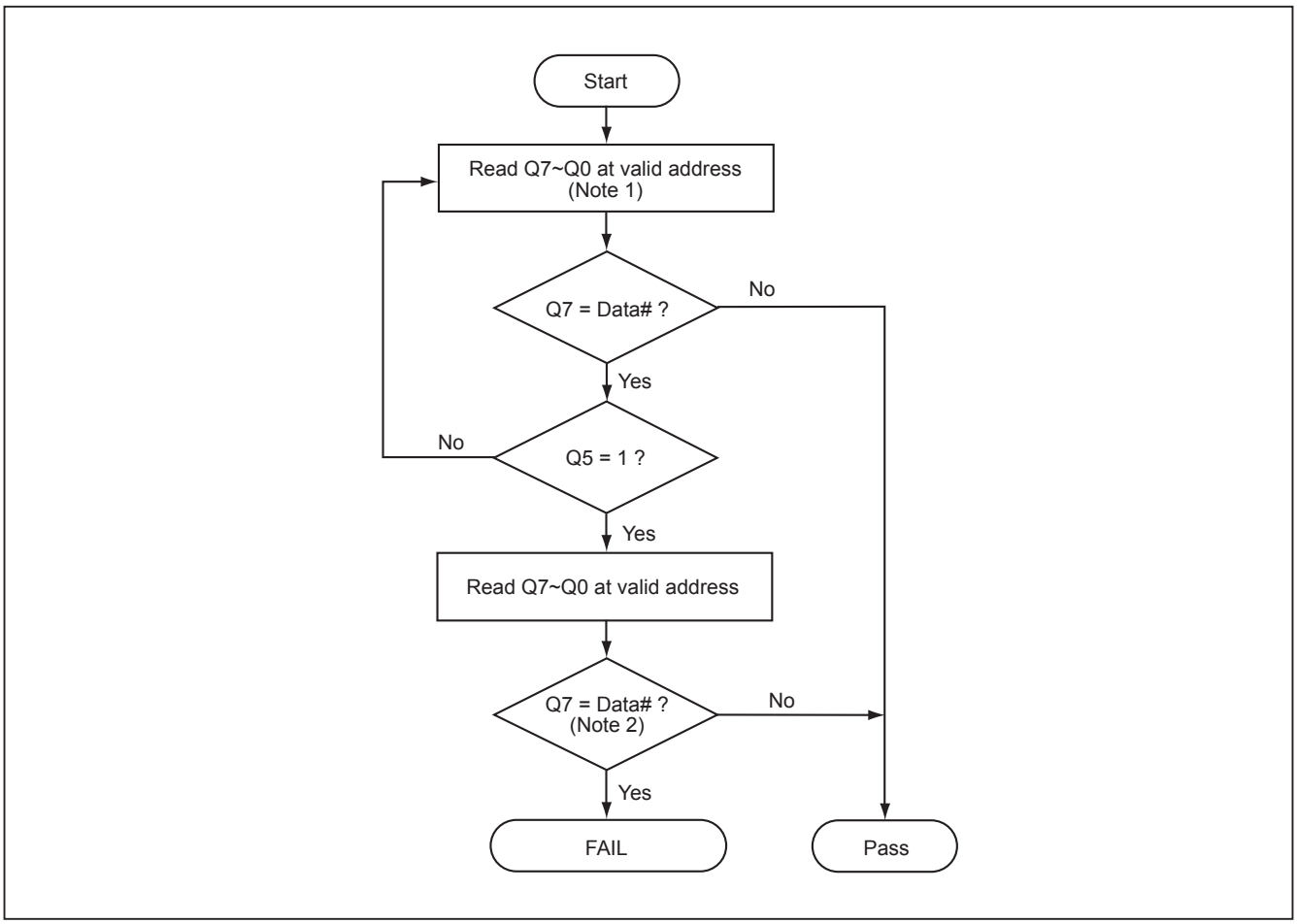


Figure 20. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 21. TOGGLE BIT TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM)

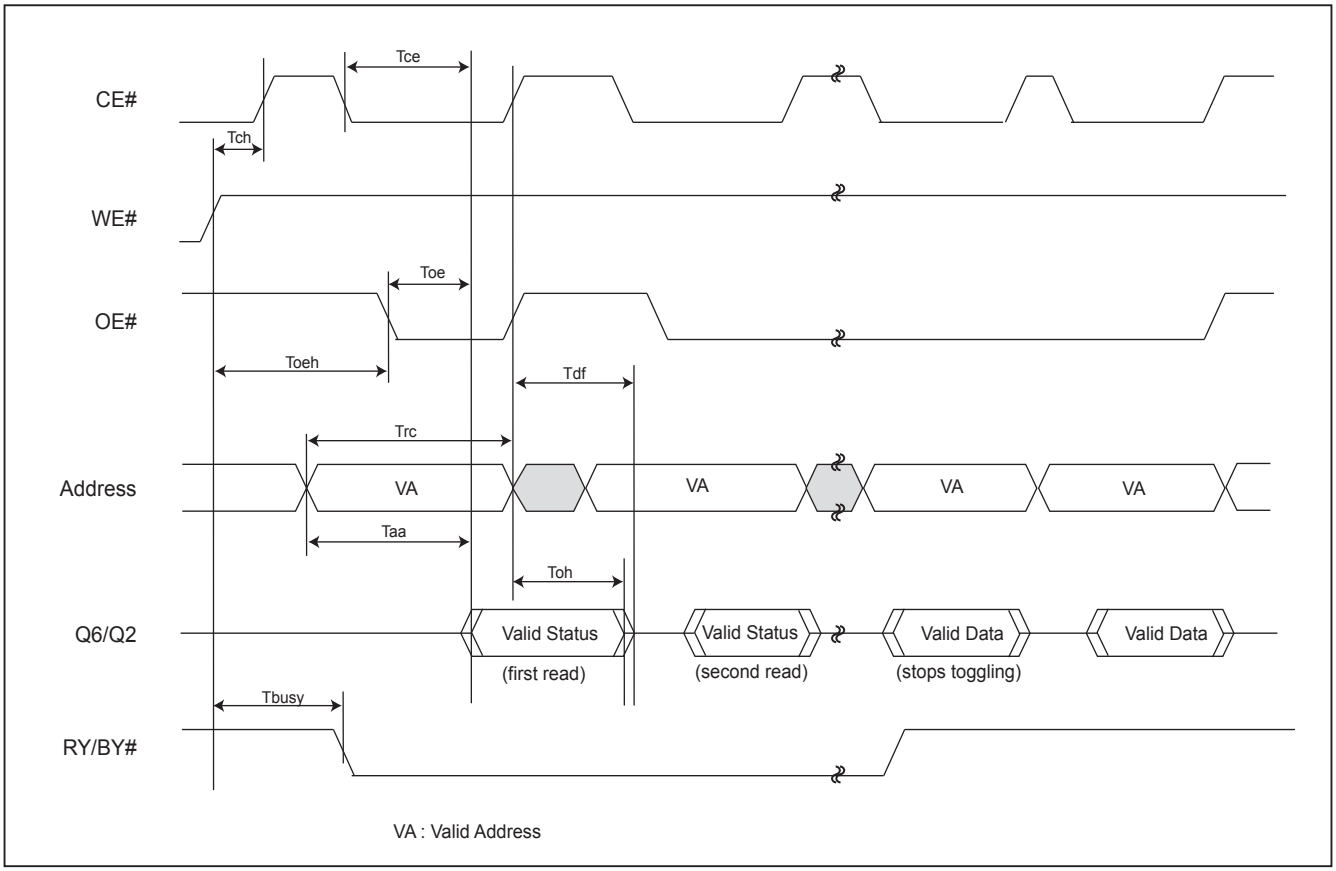
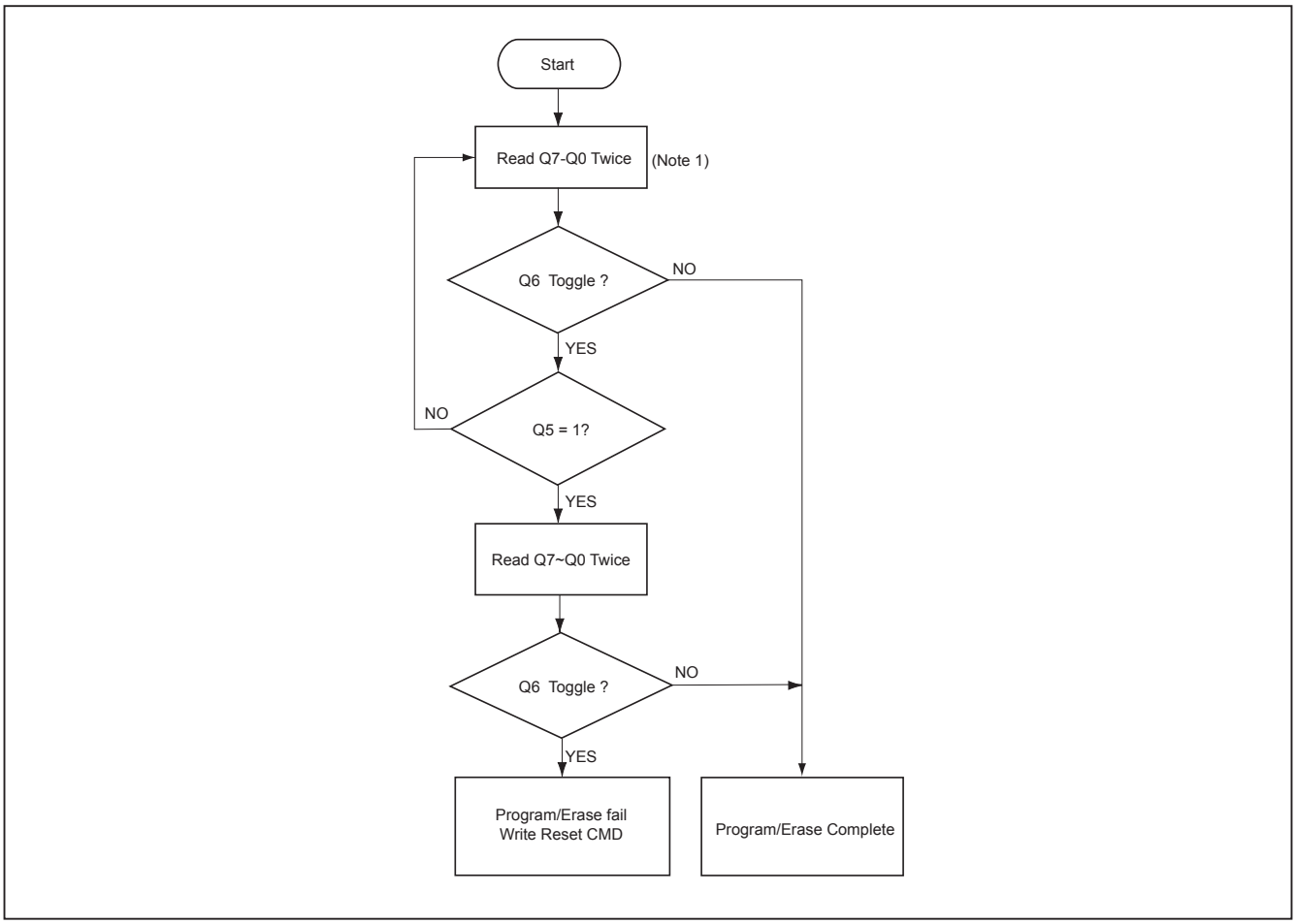


Figure 22. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

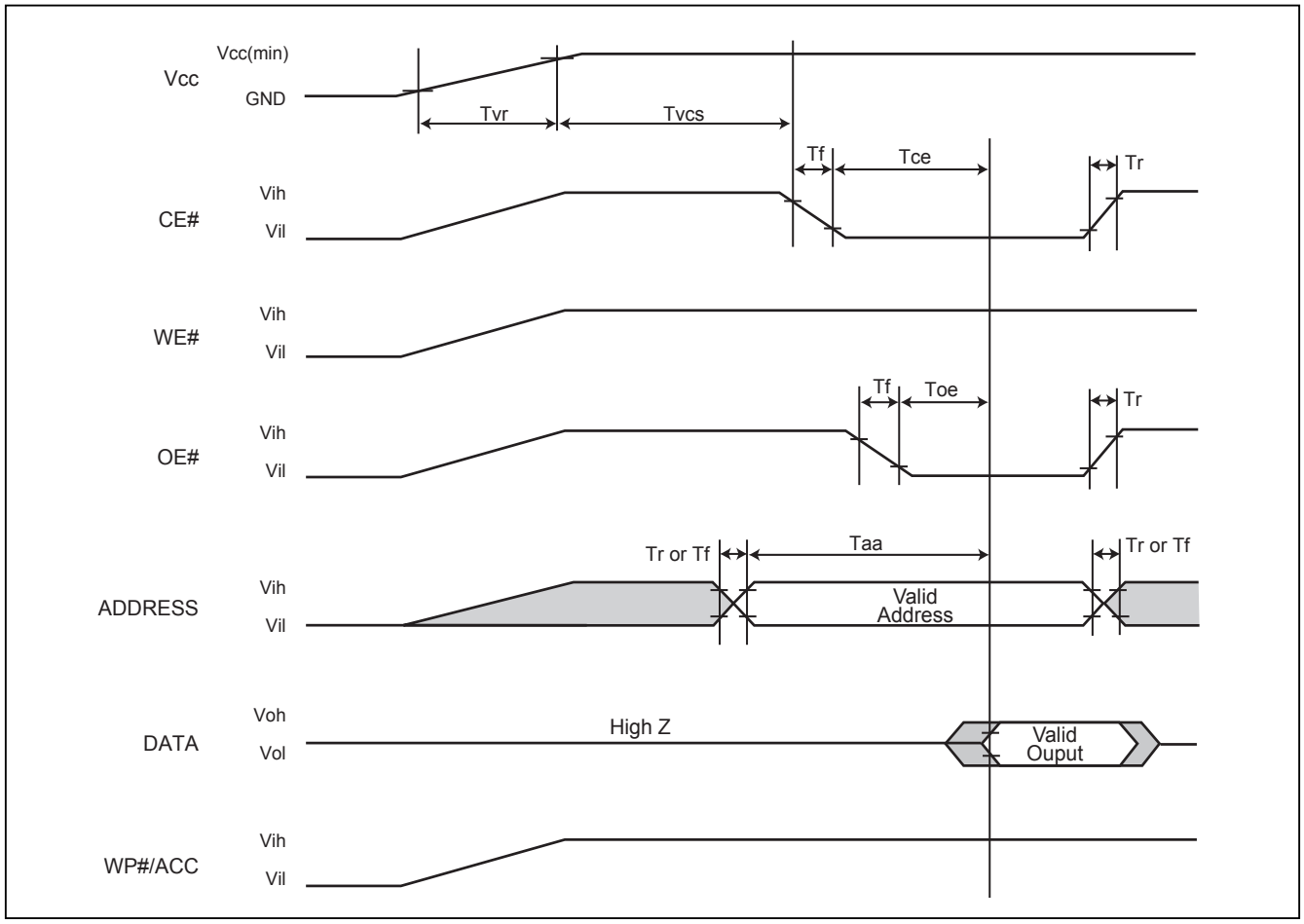


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V
Tvcs	Vcc Setup Time	200		us

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Chip Erase Time		35	50	sec
Sector Erase Time		0.7	2	sec
Erase/Program Cycles		100,000		Cycles
Chip Programming Time		24	72	sec
Word Program Time		11	360	us

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.

DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input voltage difference with GND on all pins except I/O pins	-1.0V	10.5V
Input voltage difference with GND on all I/O pins	-1.0V	1.5 x Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

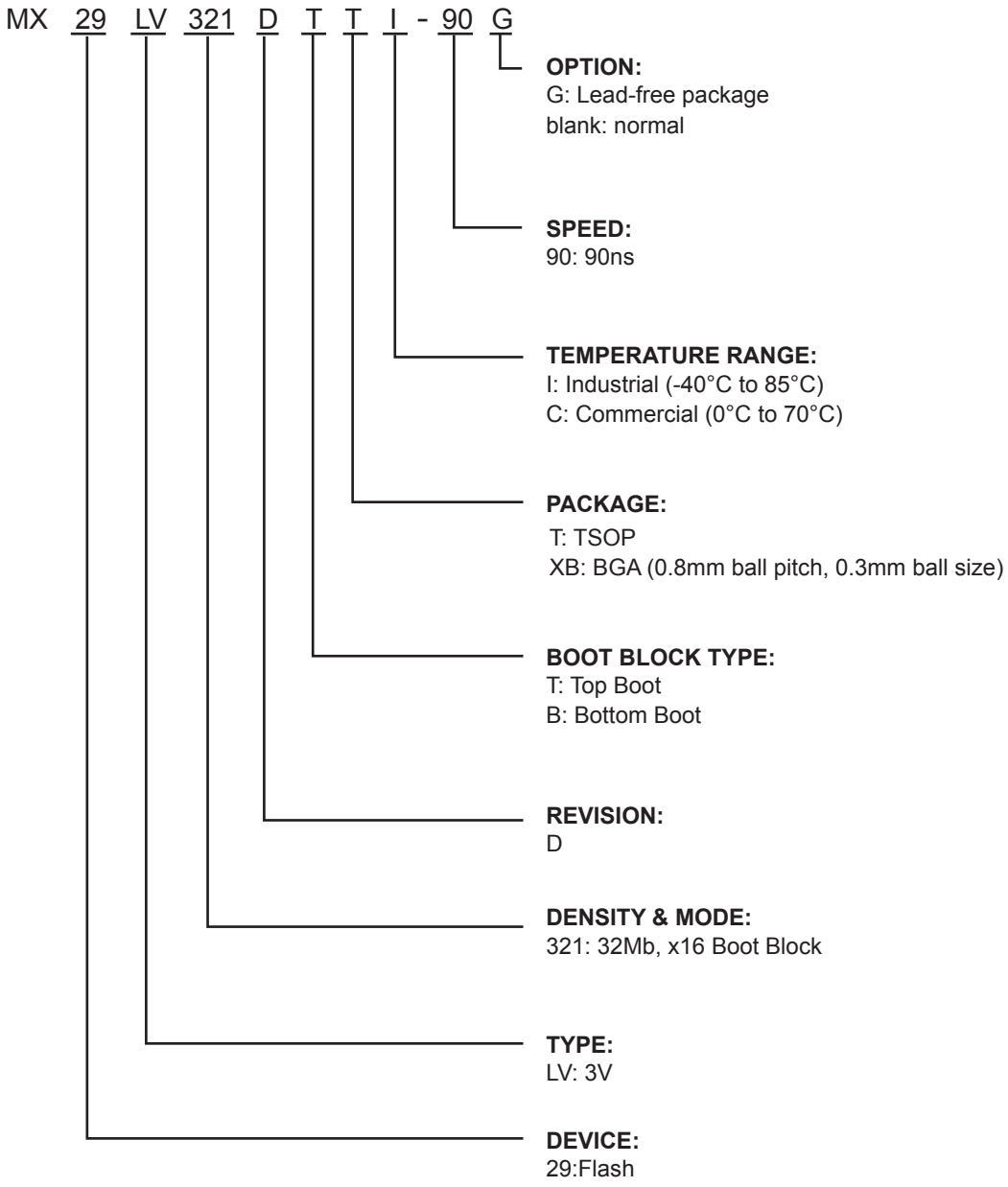
TSOP PIN/BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP.	MAX.	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

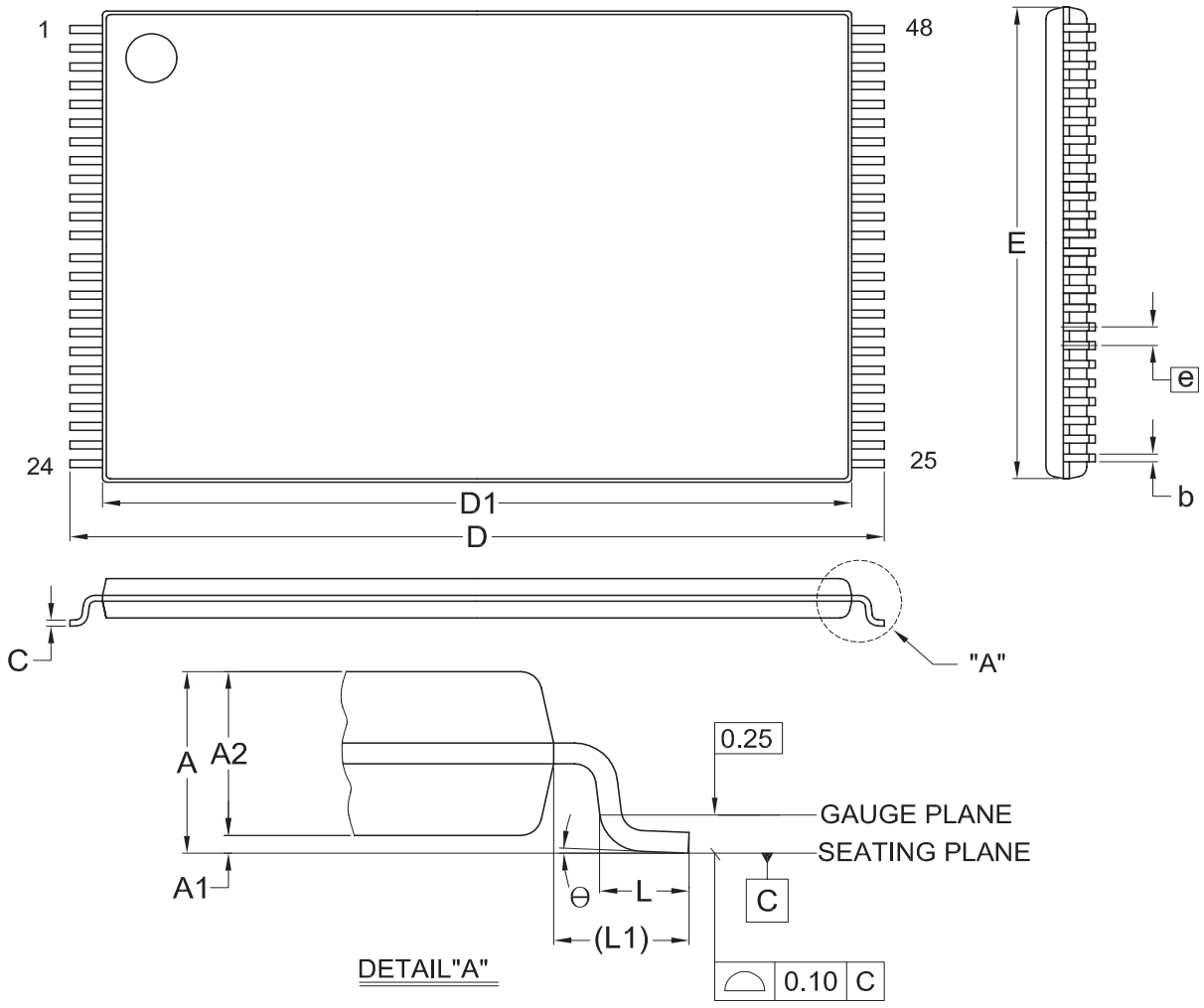
PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball Size	PACKAGE	Remark
MX29LV321DTTI-90G	90	-	48 Pin TSOP	Pb-free
MX29LV321DBTI-90G	90	-	48 Pin TSOP	Pb-free
MX29LV321DTXBI-90G	90	0.8mm/0.3mm	48-Ball BGA	Pb-free
MX29LV321DBXBI-90G	90	0.8mm/0.3mm	48-Ball BGA	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM

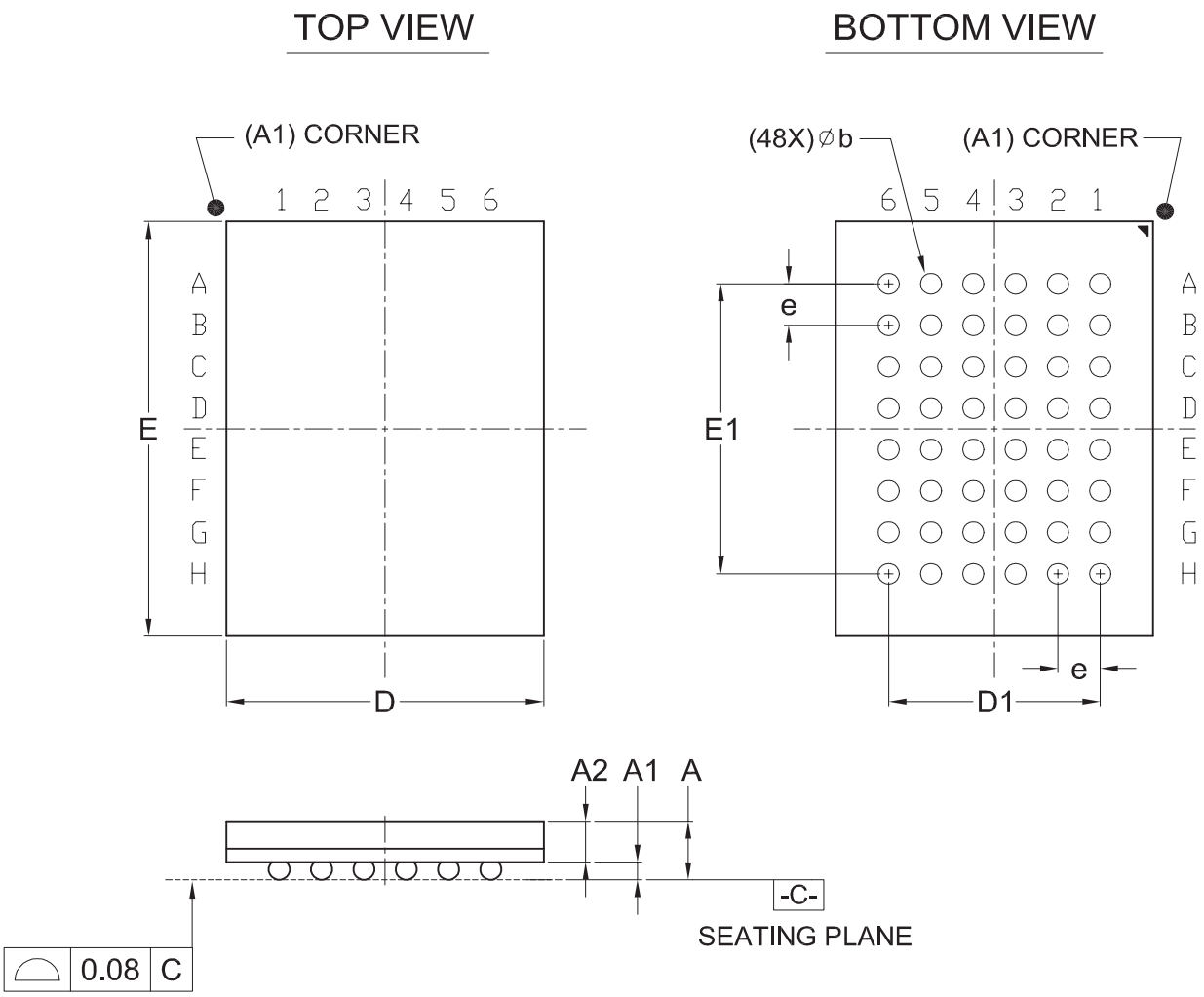


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	—	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	—	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	—	0.020	0.028	0
	Nom.	—	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	—	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

Title: Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	—	0.18	0.65	0.25	5.90		7.90		
	Nom.	—	0.23	—	0.30	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.28	—	0.35	6.10		8.10		
Inch	Min.	---	0.007	0.026	0.010	0.232		0.311		
	Nom.	---	0.009	---	0.012	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.011	---	0.014	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4201	6	MO-210			03-29-'06

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information"	P5	AUG/14/2008
1.1	1. Added 20 years data retention condition	P5,6,58	OCT/02/2009
	2. Modified SA44/SA45 address	P12	

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

Copyright© Macronix International Co., Ltd. 2007~2009. All Rights Reserved. Macronix, MXIC, MXIC Logo, MX Logo, are trademarks or registered trademarks of Macronix International Co., Ltd.. The names and brands of other companies are for identification purposes only and may be claimed as the property of the respective companies.

MACRONIX INTERNATIONAL CO., LTD.

Macronix Offices : Taiwan
Headquarters, FAB2
Macronix, International Co., Ltd.
16, Li-Hsin Road, Science Park, Hsinchu,
Taiwan, R.O.C.
Tel: +886-3-5786688
Fax: +886-3-5632888

Taipei Office
Macronix, International Co., Ltd.
19F, 4, Min-Chuan E. Road, Sec. 3, Taipei,
Taiwan, R.O.C.
Tel: +886-2-2509-3300
Fax: +886-2-2509-2200

Macronix Offices : China
Macronix (Hong Kong) Co., Limited.
702-703, 7/F, Building 9, Hong Kong Science Park,
5 Science Park West Avenue, Sha Tin,
N.T.
Tel: +86-852-2607-4289
Fax: +86-852-2607-4229

Macronix (Hong Kong) Co., Limited,
SuZhou Office
No.5, XingHai Rd, SuZhou Industrial Park,
SuZhou China 215021
Tel: +86-512-62580888 Ext: 3300
Fax: +86-512-62586799

Macronix (Hong Kong) Co., Limited,
Shenzhen Office
Room 1401 & 1404, Block A, TianAN Hi-Tech PLAZA Tower,
Che Gong Miao, FutianDistrict, Shenzhen PRC 518040
Tel: +86-755-83433579
Fax: +86-755-83438078

Macronix Offices : Japan
Macronix Asia Limited.
NKF Bldg. 5F, 1-2 Higashida-cho,
Kawasaki-ku Kawasaki-shi,
Kanagawa Pref. 210-0005, Japan
Tel: +81-44-246-9100
Fax: +81-44-246-9105

Macronix Offices : Korea
Macronix Asia Limited.
#906, 9F, Kangnam Bldg., 1321-4, Seocho-Dong, Seocho-Ku,
135-070, Seoul, Korea
Tel: +82-02-588-6887
Fax: +82-02-588-6828

Macronix Offices : Singapore
Macronix Pte. Ltd.
1 Marine Parade Central, #11-03 Parkway Centre,
Singapore 449408
Tel: +65-6346-5505
Fax: +65-6348-8096

Macronix Offices : Europe
Macronix Europe N.V.
Koningin Astridlaan 59, Bus 1 1780
Wemmel Belgium
Tel: +32-2-456-8020
Fax: +32-2-456-8021

Macronix Offices : USA
Macronix America, Inc.
680 North McCarthy Blvd. Milpitas, CA 95035,
U.S.A.
Tel: +1-408-262-8887
Fax: +1-408-262-8810

http : //www.macronix.com