MX29LV320C T/B

32M-BIT [4M x 8 / 2M x 16] SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- 4,194,304 x 8 / 2,097,152 x 16 switchable
- Sector Structure
  - 8K-Byte x 8 and 64K-Byte x 63
- Extra 64K-Byte sector for security
  - Features factory locked and identifiable, and customer lockable
- Twenty-Four Sector Groups
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector group unprotect function for code changing in previously protected sector groups
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit : Vcc <= 1.4V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- **Fully compatible with MX29LV320A T/B device**

PERFORMANCE

- High Performance
  - Fast access time: 70/90nS
  - Fast program time: 7uS/word typical utilizing accelerate function
  - Fast erase time: 0.9s/sector, 35s/chip (typical)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 200nA (typical)
- Minimum 100,000 erase/program cycle
- 10 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Provides accelerated program capability

PACKAGE

- 48-Pin TSOP
- 48-Ball CSP
- **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

MX29LV320CT/B is a 32Mbit flash memory that can be organized as 4Mbytes of 8 bits each or as 2Mbytes of 16 bits each. These devices operate over a voltage range of 2.7V to 3.6V typically using a 3V power supply input. The memory array is divided into 64 equal 64 Kilo byte blocks. However, depending on the device being used as a Top-Boot or Bottom-Boot device, the top or the bottom first block is further subdivided into 8 equal 8Kbyte blocks. The outermost two sectors at the top or at the bottom are respectively the boot blocks for this device. This flash memory also provides an additional factory lockable or customer lockable 64Kbyte sector to provide security feature.

The MX29LV320CT/B is offered in a 48-pin TSOP and a 48-ball CSP JEDEC standard package. These packages are offered in leaded, as well as lead-free versions that are compliant to the RoHS specifications. The software algorithm used for this device also adheres to the JEDEC standard for single power supply devices. These flash parts can be programmed in system or on commercially available EPROM/Flash programmers.

Separate OE# and CE# (Output Enable and Chip Enable) signals are provided to simplify system design. When used with high speed processors, the 70ns read access time of this flash memory permits operation with minimal time lost due to system timing delays.

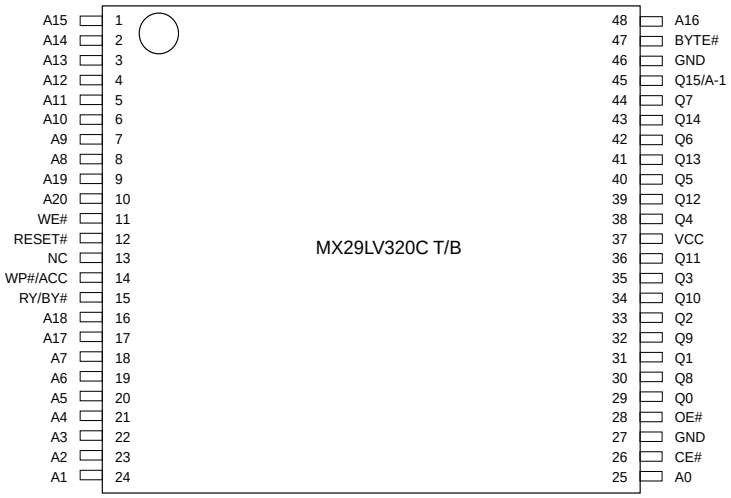
The automatic write algorithm provided on Macronix flash memories perform an automatic erase prior to write. The user only needs to provide a write command to the command register. The on-chip state machine automatically controls the program and erase functions including all necessary internal timings. Since erase and write operations take much longer time than read operations, erase/write can be interrupted to perform read operations in other sectors of the device. For this, Erase Suspend operation along with Erase Resume operation are provided. Data# polling or Toggle bits are used to indicate the end of the erase/write operation.

These devices are manufactured at the Macronix fabrication facility using the time tested and proven PACAND (Paired Array Contactless based AND) TECHNOLOGY. This propreitary non-epi process provides a very high degree of latch-up protection for stresses up to 100 milliamperes on address and data pins from -1V to Vcc+1V.

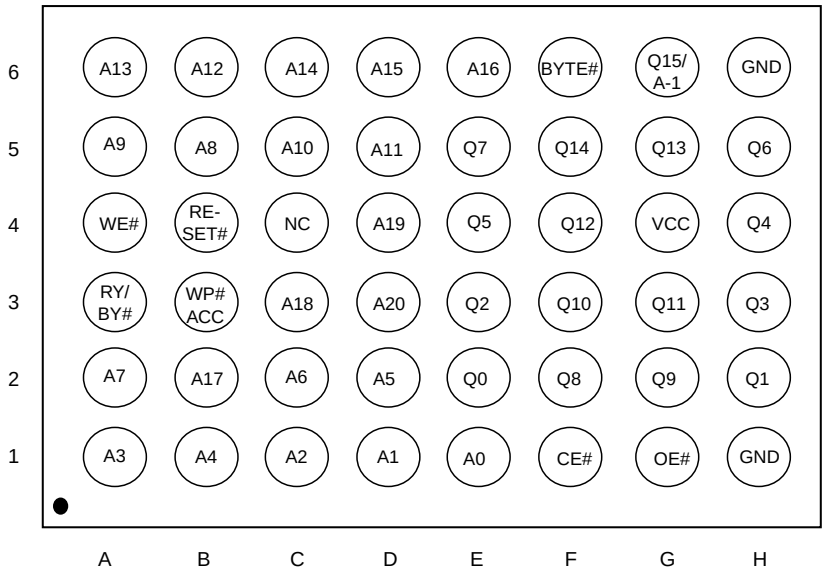
With low power consumption and enhanced hardware and software features, this flash memory retains data reliably for at least ten years. Erase and programming functions have been tested to meet a minimum specification of 100,000 cycles of operation.

PIN CONFIGURATION

48 TSOP



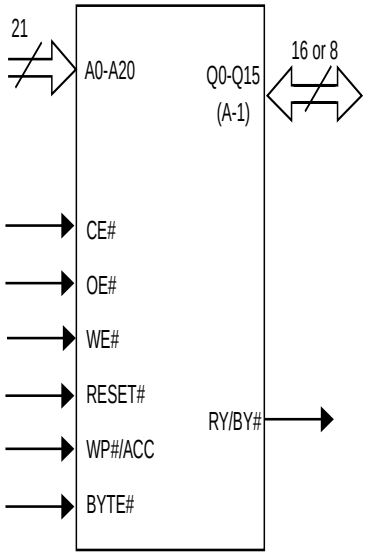
48-Ball CSP 6mm x 8mm (Ball Pitch = 0.8 mm), Top View, Balls Facing Down



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15/A-1	Q15(Data Input/Output, word mode); A-1(LSB Address Input, byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
BYTE#	Word/Byte Selection Input
RESET#	Hardware Reset Pin, Active Low
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply
WP#/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM

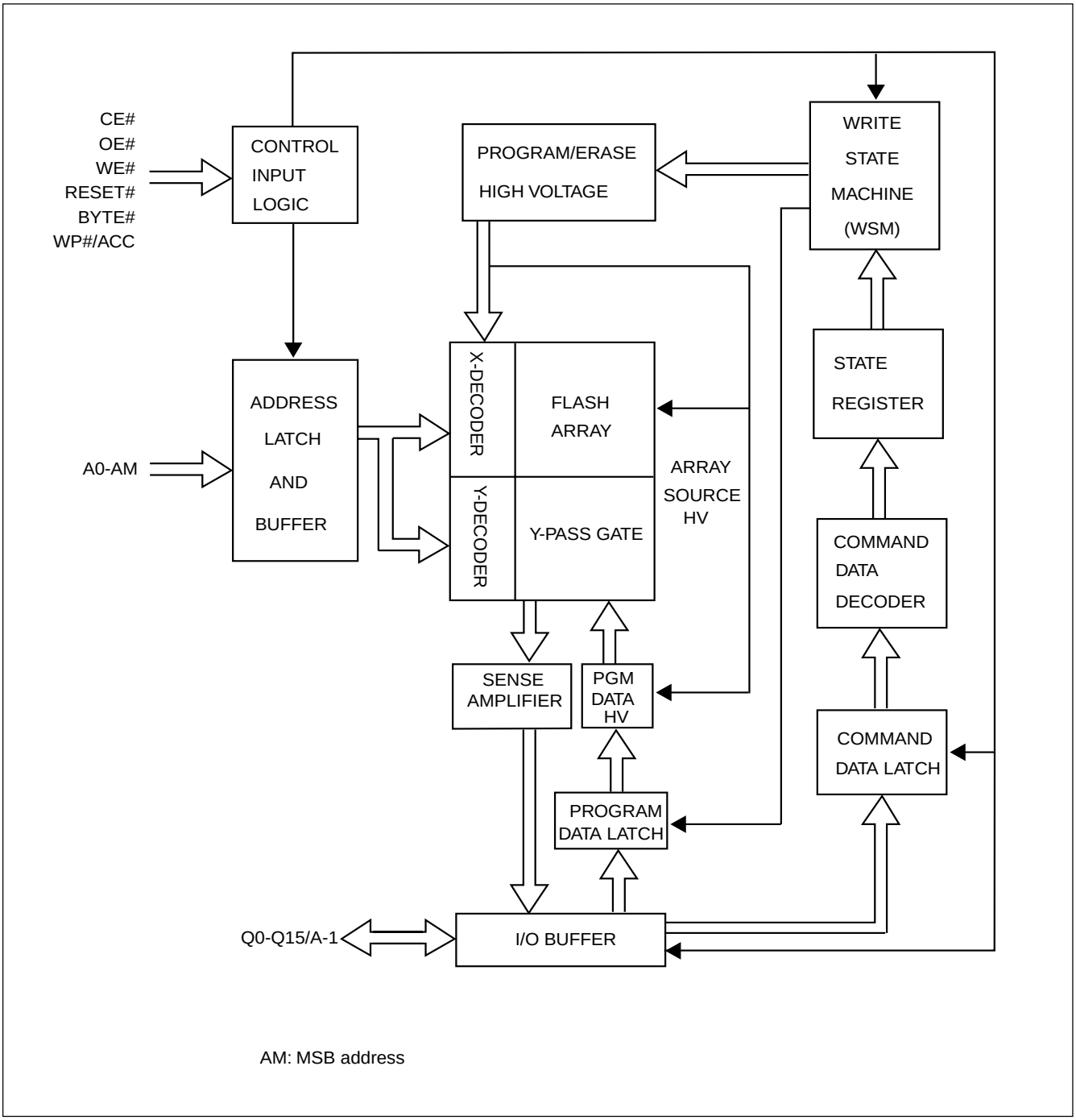


Table 1.a: MX29LV320CT SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	000000xxx	64/32	000000h-00FFFFh	000000h-07FFFh
1	SA1	000001xxx	64/32	010000h-01FFFFh	008000h-0FFFFh
1	SA2	000010xxx	64/32	020000h-02FFFFh	010000h-17FFFh
1	SA3	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
2	SA4	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
2	SA5	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
2	SA6	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
2	SA7	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
3	SA8	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
3	SA9	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
3	SA10	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
3	SA11	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
4	SA12	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
4	SA13	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
4	SA14	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
4	SA15	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
5	SA16	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
5	SA17	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
5	SA18	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
5	SA19	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
6	SA20	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
6	SA21	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
6	SA22	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
6	SA23	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
7	SA24	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
7	SA25	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
7	SA26	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
7	SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
8	SA28	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
8	SA29	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
8	SA30	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
8	SA31	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
9	SA32	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
9	SA33	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
9	SA34	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
9	SA35	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
10	SA36	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
10	SA37	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
10	SA38	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
10	SA39	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
11	SA40	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
11	SA41	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
11	SA42	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
11	SA43	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
12	SA44	101100xxx	64/32	2C0000h-2CFFFFh	160000h-147FFFh
12	SA45	101101xxx	64/32	2D0000h-2DFFFFh	168000h-14FFFFh
12	SA46	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
12	SA47	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
13	SA48	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
13	SA49	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
13	SA50	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
13	SA51	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
14	SA52	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
14	SA53	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
14	SA54	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
14	SA55	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
15	SA56	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
15	SA57	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
15	SA58	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
15	SA59	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
16	SA60	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
16	SA61	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
16	SA62	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
17	SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
18	SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
19	SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
20	SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
21	SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
22	SA68	111111101	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
23	SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
24	SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Top Boot Security Sector Addresses

Sector Address A20~A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh

Table 1.b: MX29LV320CB SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
2	SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
3	SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
4	SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
5	SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
6	SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
7	SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
8	SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
9	SA8	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
9	SA9	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
9	SA10	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
10	SA11	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
10	SA12	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
10	SA13	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
10	SA14	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
11	SA15	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
11	SA16	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
11	SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
11	SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
12	SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
12	SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
12	SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
12	SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
13	SA23	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
13	SA24	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
13	SA25	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
13	SA26	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
14	SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
14	SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
14	SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
14	SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
15	SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
15	SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
15	SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
15	SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
16	SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
16	SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
16	SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
16	SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
17	SA39	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
17	SA40	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
17	SA41	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
17	SA42	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
18	SA43	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
18	SA44	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
18	SA45	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
18	SA46	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
19	SA47	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
19	SA48	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
19	SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
19	SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
20	SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
20	SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
20	SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
20	SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
21	SA55	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
21	SA56	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
21	SA57	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
21	SA58	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
22	SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
22	SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
22	SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
22	SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
23	SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
23	SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
23	SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
23	SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
24	SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
24	SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
24	SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
24	SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh

Bottom Boot Security Sector Addresses

Sector Address A20~A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
111111xxx	64/32	000000h-00FFFFh	00000h-07FFFh

Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Data (I/O) Q0~Q7	Byte# Vil Data (I/O) Q8~Q15	Byte# Vih Data (I/O) Q8~Q15	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ	L/H
Standby Mode	Vcc± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ	H
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ Q15= A-1	DOUT	L/H
Write(Note1)	H	L	L	H	AIN	DIN		DIN	Note3
Accelerate Program	H	L	L	H	AIN	DIN		DIN	Vhv
Temporary Sector-Group Unprotect	Vhv	X	X	X	AIN	DIN	HighZ	DIN	Note3
Sector-Group Protect (Note2)	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	X	X	L/H
Chip Unprotect (Note2)	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	X	X	Note3

Notes:
1. All sectors will be unprotected if WP#/ACC=Vhv.
2. The two outmost boot sectors are protected if WP#/ACC=Vil.
3. When WP#/ACC = Vih, the protection conditions of the two outmost boot sectors depend on previous protection conditions."Sector/Sector Block Protection and Unprotection" describes the protect and unprotect method.
4. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
5. In Word Mode (Byte#=Vih), the addresses are AM to A0.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15).
6. AM: MSB of address.

BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0~Q7	Q8~Q15
	CE#	WE#	OE#										
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)	x
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2H	x
Read Silicon ID MX29LV320CT	L	H	L	x	x	V_{hv}	x	L	x	L	H	A7H	22h(Word)
													x (Byte)
Read Silicon ID MX29LV320CB	L	H	L	x	x	V_{hv}	x	L	x	L	H	A8H	22h(Word)
													x (Byte)
Read Indicator Bit (Q7) For Security Sector	L	H	L	x	x	V_{hv}	x	L	x	H	H	99h or 19h (Note2)	x

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: 99h. Factory unlocked code: 19h.
3. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

ACCELERATED PROGRAM OPERATION

The accelerated program can improve programming performance compared with word/byte program. By applying Vhv on WP#/ACC pin, the device will enter accelerated program and draw current no more than Icw from WP#/ACC pin. Removing the Vhv from WP#/ACC pin will put the device back to normal operation (not accelerated).

RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready1 for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR GROUP PROTECT OPERATION

When a sector group is protected, program or erase operation will be disabled on these sectors. MX29LV320C T/B provides two methods for sector group protection.

Once the sector group is protected, the sector group remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector group unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV320C T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors groups are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

WRITE PROTECT (WP#)

Another function of the WP#/ACC pin is to provide write protection function on the two outermost 8 Kbyte boot sectors. When ViL is asserted on WP#/ACC pin, the two boot sectors are protected regardless of the previous state of protection implemented by aforementioned Sector Group Protect/Chip Unprotect. For MX29LV320T, the two outermost sectors are the two boot sectors of the highest addresses. For MX29LV320C T/B, the two outermost sectors are the two boot sectors of the lowest addresses.

Note that the WP#/ACC should be either Vhv, Vih, or Vil, and must not be floated or unconnected; otherwise the device may not function properly.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV320C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires V_{hv} on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A20 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra memory space of 64Kbytes(32Kwords) in length. The security sectors can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the security silicon region is permanently locked after shipping from factory. The device will have a 16-byte (8-word) ESN in the security region. In bottom boot device, the ESN occupies addresses 00000h to 0000Fh in byte mode or 00000h to 00007h in word mode. In top boot device, the ESN occupies addresses 3F0000h to 3F000Fh in byte mode or 1F8000h to 1F8007h in word mode.

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space. The security silicon sector can be read, programmed, or erased just as normal sectors with the same endurance limitations.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

The first method is to write a three-cycle command of Enter Security Region, and then follow the sector group protect algorithm as illustrated in Figure 14, except that RESET# pin may at either Vih or Vhv.

The other method is to write a three-cycle command of Enter Security Region, and then follow the alternate method of sector protect with A9, OE# at Vhv.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV320C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV320C T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select								Enter Security Sector Region Enable	
				Silicon ID		Device ID		Sector Factory		Sector Protect Verify			
	Hex			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cyc	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cyc	Addr			2AA	555	2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55	55	55
3rd Bus Cyc	Addr			555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	90	90	88	88
4th Bus Cyc	Addr			X00	X00	X01	X02	X03	X06	(Sector) X02	(Sector)X 04		
	Data			C2H	C2H	ID	ID	99/19	99/19	00/01	00/01		
5th Bus Cyc	Addr												
	Data												
6th Bus Cyc	Addr												
	Data												

Command		Exit Security Sector		Program		Chip Erase		Sector Erase		CFI Read		Erase Suspend	Erase Resume
	Hex	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Byte/Word	Byte/Word
1st Bus Cyc	Addr	555	AAA	555	AAA	555	AAA	555	AAA	55	AA	XXX	XXX
	Data	AA	AA	AA	AA	AA	AA	AA	AA	98	98	B0	30
2nd Bus Cyc	Addr	2AA	555	2AA	555	2AA	555	2AA	555				
	Data	55	55	55	55	55	55	55	55				
3rd Bus Cyc	Addr	555	AAA	555	AAA	555	AAA	555	AAA				
	Data	90	90	A0	A0	80	80	80	80				
4th Bus Cyc	Addr	XXX	XXX	Addr	Addr	555	AAA	555	AAA				
	Data	00	00	Data	Data	AA	AA	AA	AA				
5th Bus Cyc	Addr					2AA	555	2AA	555				
	Data					55	55	55	55				
6th Bus Cyc	Addr					555	AAA	Sector	Sector				
	Data					10	10	30	30				

Notes: ID 22A7h(Top), 22A8h(Bottom).

RESET

In the following situations, executing reset command will reset device back to read array mode:
- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

		Address	Data (Hex)	Representation
Manufacturer ID	Word	X00	C2	
	Byte	X00	C2	
Device ID	Word	X01	22A7/22A8	Top/Bottom Boot Sector
	Byte	X02	A7/A8	Top/Bottom Boot Sector
Secured Silicon	Word	X03	99/19	Factory locked/unlocked
	Byte	X06	99/19	Factory locked/unlocked
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected
	Byte	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LV320C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV320C T/B is less than 36 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	togging	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Togging	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Togging	0	0	Toggling	0
In progress	0	Togging	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400uS interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV320C T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command, 98H, to address 55H/AAH (depending on Word/Byte mode) any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4. A reset command is required to exit CFI mode and go back to ready array mode or erase suspend mode. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code	17	2E	0000
	18	30	0000
Address for alternate algorithm extended query table	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	36	0027
Vcc supply maximum program/erase voltage	1C	38	0036
VPP supply minimum program/erase voltage	1D	3A	0000
VPP supply maximum program/erase voltage	1E	3C	0000
Typical timeout per single word/byte write, 2^n uS	1F	3E	0004
Typical timeout for maximum-size buffer write, 2^n uS	20	40	0000
Typical timeout per individual block erase, 2^n mS	21	42	000A
Typical timeout for full chip erase, 2^n mS	22	44	0000
Maximum timeout for word/byte write, 2^n times typical	23	46	0005
Maximum timeout for buffer write, 2^n times typical	24	48	0000
Maximum timeout per individual block erase, 2^n times typical	25	4A	0004
Maximum timeout for chip erase, 2^n times typical	26	4C	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Device size = 2^n in number of bytes	27	4E	0016
Flash device interface description (02=asynchronous x8/x16)	28	50	0002
	29	52	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	54	0000
	2B	56	0000
Number of erase regions within device	2C	58	0002
Index for Erase Bank Area 1	2D	5A	0007
[2E,2D] = # of same-size sectors in region 1-1	2E	5C	0000
[30, 2F] = sector size in multiples of 256-bytes	2F	5E	0020
	30	60	0000
Index for Erase Bank Area 2	31	62	003E
	32	64	0000
	33	66	0000
	34	68	0001
Index for Erase Bank Area 3	35	6A	0000
	36	6C	0000
	37	6E	0000
	38	70	0000
Index for Erase Bank Area 4	39	72	0000
	3A	74	0000
	3B	76	0000
	3C	78	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0031
Unlock recognizes address (0= recognize, 1= don't recognize)	45	8A	0000
Erase suspend (2= to both read and program)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0004
Temporary sector unprotect (1=supported)	48	90	0001
Sector protect/Chip unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode (0=not supported)	4B	96	0000
Page mode (0=not supported)	4C	98	0000
Maximum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	9A	00B5
Minimum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	9C	00C5
Top/Bottom boot block indicator 02h=bottom boot device 03h=top boot device	4F	9E	000X

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . -0.5 V to +4.0 V
RESET#, A9 and OE# . . . . . -0.5 V to +12.5 V
The other pins. . . . . -0.5 V to Vcc +0.5 V
Output Short Circuit Current (less than one second) . . . . . 200 mA

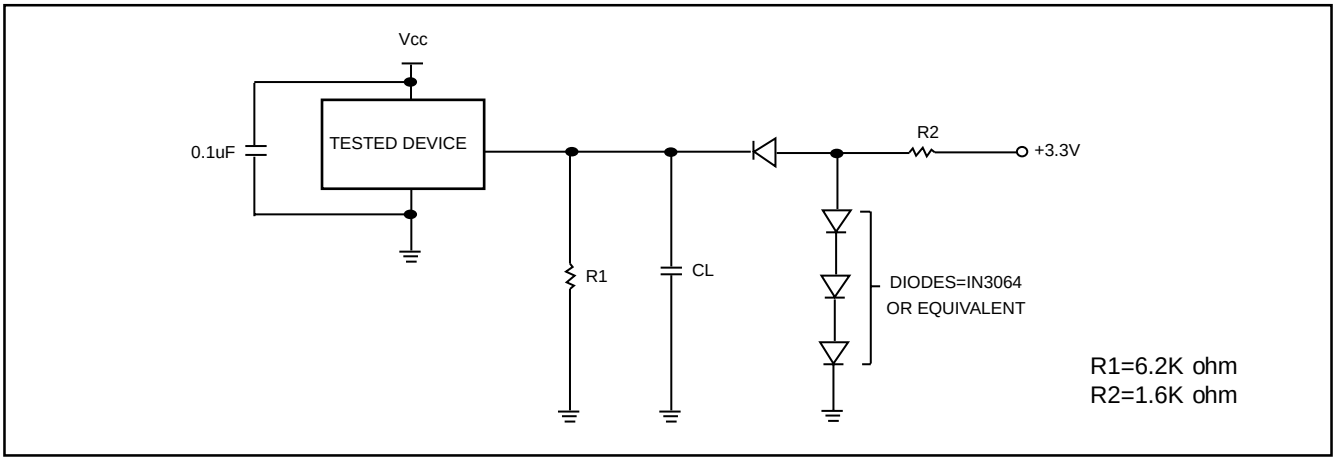
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade
Surrounding Temperature (T_A). . . . . 0°C to +70°C
Industrial (I) Grade
Surrounding Temperature (T_A). . . . . -40°C to +85°C
V_{CC} Supply Voltages
V_{CC} range. . . . . +2.7 V to 3.6 V

DC CHARACTERISTICS

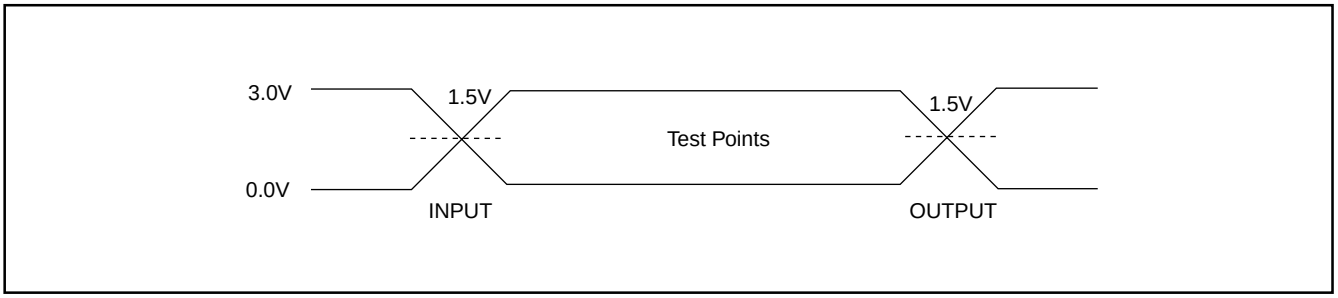
Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			±1.0uA	
Iilk9	A9 Leak			35uA(0~70°C)/ 45uA(-40~85°C)	A9=12.5V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current(5MHz)		10mA	16mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		0.2uA	15uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		0.2uA	15uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		0.2uA	15uA	
Icp1	Accelerated Pgm Current, WP#/Acc pin(Word/Byte)		5mA	10mA	CE#=Vil, OE#=Vih,
Icp2	Accelerated Pgm Current, Vcc pin,(Word/Byte)		15mA	30mA	CE#=Vil, OE#=Vih,
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/Accelerated Program/Auto Select/Temporary Unprotect	11.5V		12.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF(70nS)/100pF(90nS)
Rise/Fall Times : 5nS
In/Out reference levels :1.5V

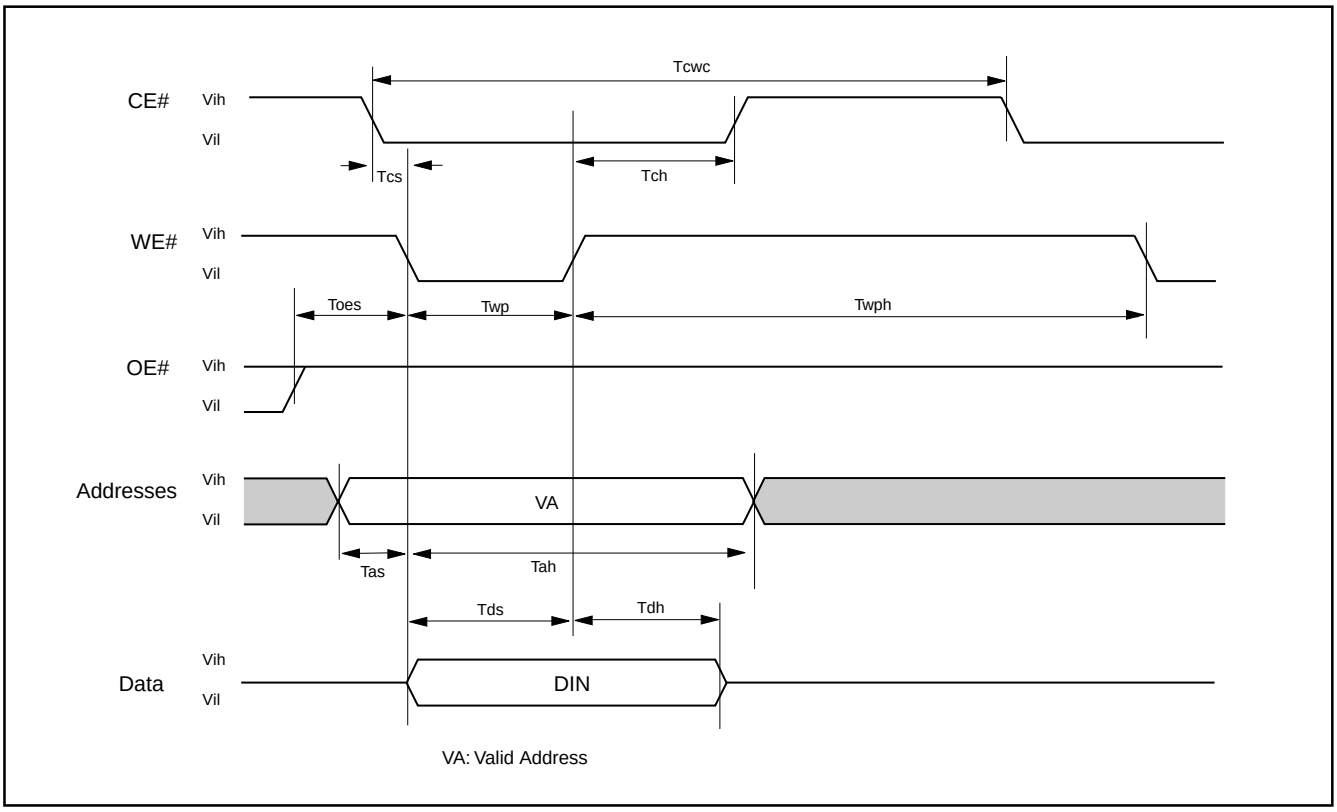
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

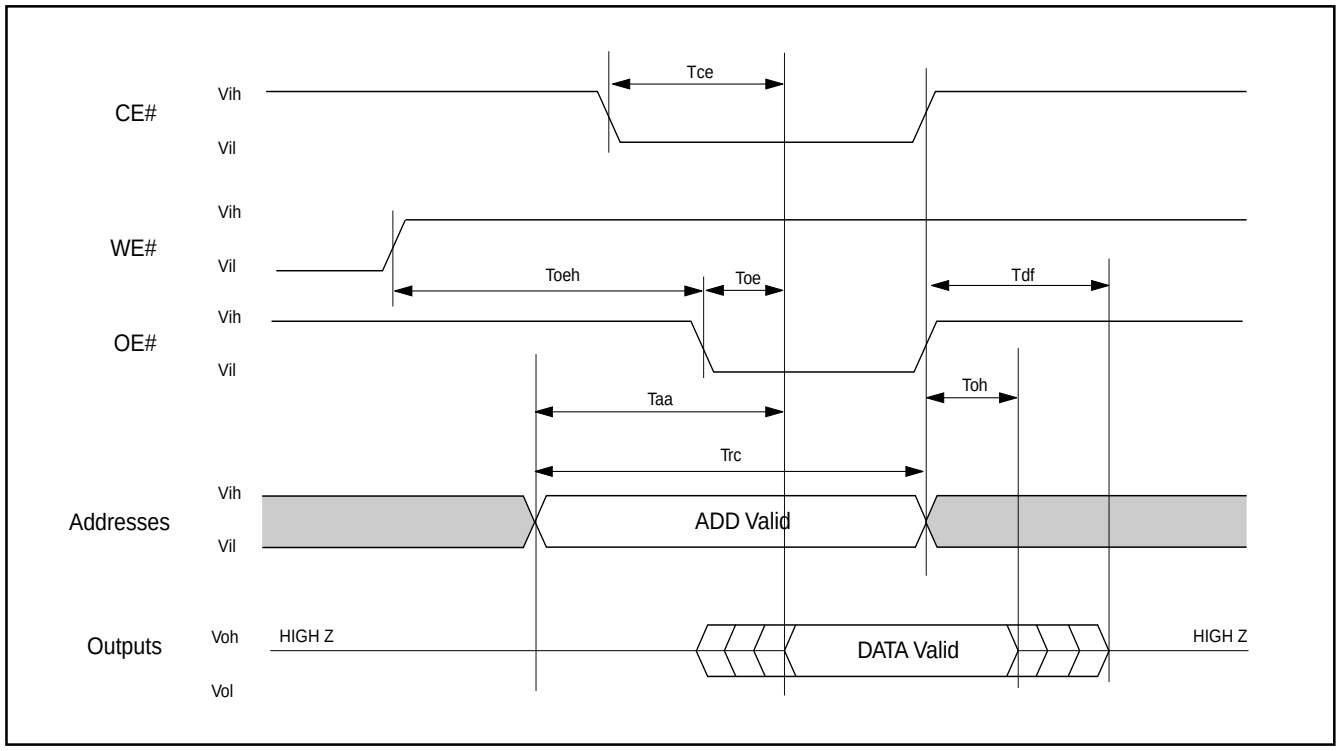
Symbol	Description		Min	Typ	Max	Unit
Taa	Valid data output after address				70/90	nS
Tce	Valid data output after CE# low				70/90	nS
Toe	Valid data output after OE# low				40	nS
Tdf	Data output floating after OE# high				30	nS
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			nS
Trc	Read period time		70/90			nS
Twc	Write period time		70/90			nS
Tcwc	Command write period time		70/90			nS
Tas	Address setup time		0			nS
Tah	Address hold time		45			nS
Tds	Data setup time		45			nS
Tdh	Data hold time		0			nS
Tvcs	Vcc setup time		50			uS
Tcs	Chip enable Setup time		0			nS
Tch	Chip enable hold time		0			nS
Toes	Output enable setup time		0			nS
Toeh	Output enable hold time	Read	0			nS
Toeh		Toggle & Data# Polling	10			nS
Tws	WE# setup time		0			nS
Twh	WE# hold time		0			nS
Tcep	CE# pulse width		45			nS
Tceph	CE# pulse width high		30			nS
Twp	WE# pulse width		35			nS
Twph	WE# pulse width high		30			nS
Tbusy	Program/Erase active time by RY/BY#				90	nS
Tghwl	Read recover time before write		0			nS
Tghel	Read recover time before write		0			nS
Twhwh1	Program operation	Byte		9		uS
Twhwh1	Program operation	Word		11		uS
Twhwh1	Acc program operation (Word/Byte)			7		uS
Twhwh2	Sector erase operation			0.9		sec
Tbal	Sector add hold time				50	uS

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

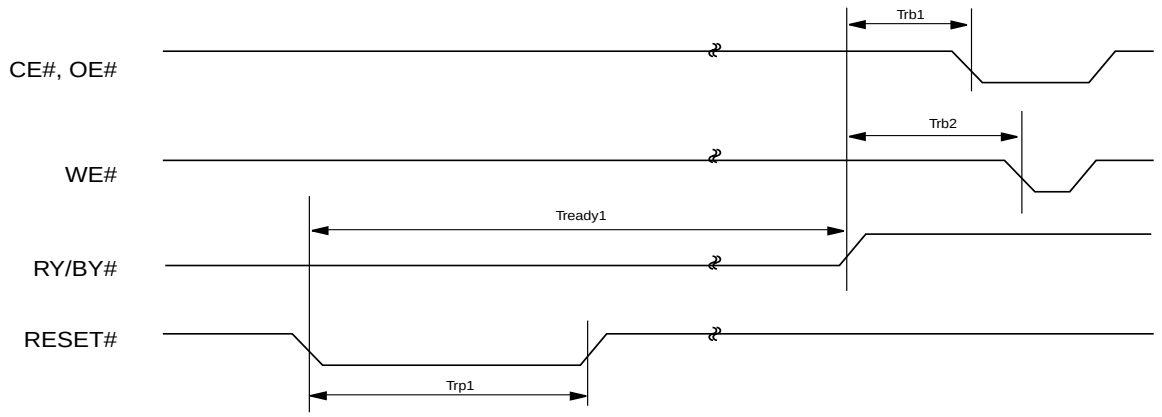
Figure 2. READ TIMING WAVEFORMS



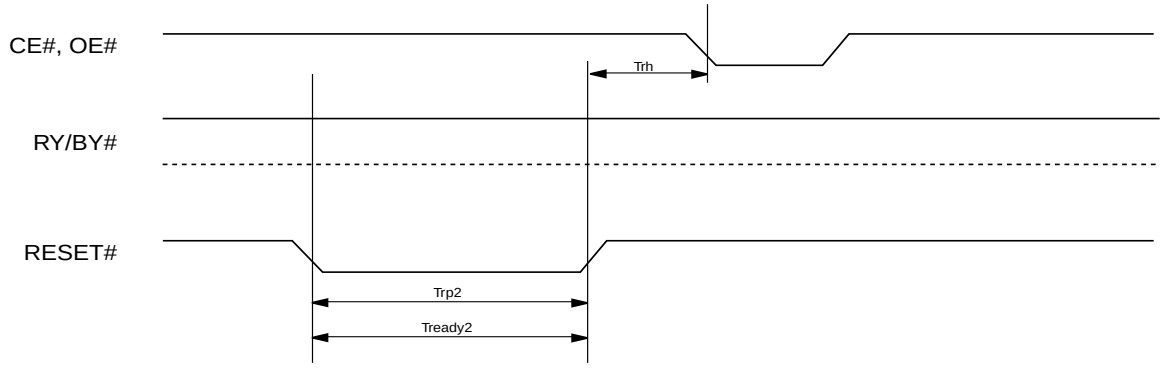
AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	uS
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	nS
Trh	RESET# High Time Before Read	MIN	70	nS
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	nS
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	nS
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	uS
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	nS

Figure 3. RESET# TIMING WAVEFORM



Reset Timing during Automatic Algorithms



Reset Timing NOT during Automatic Algorithms

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

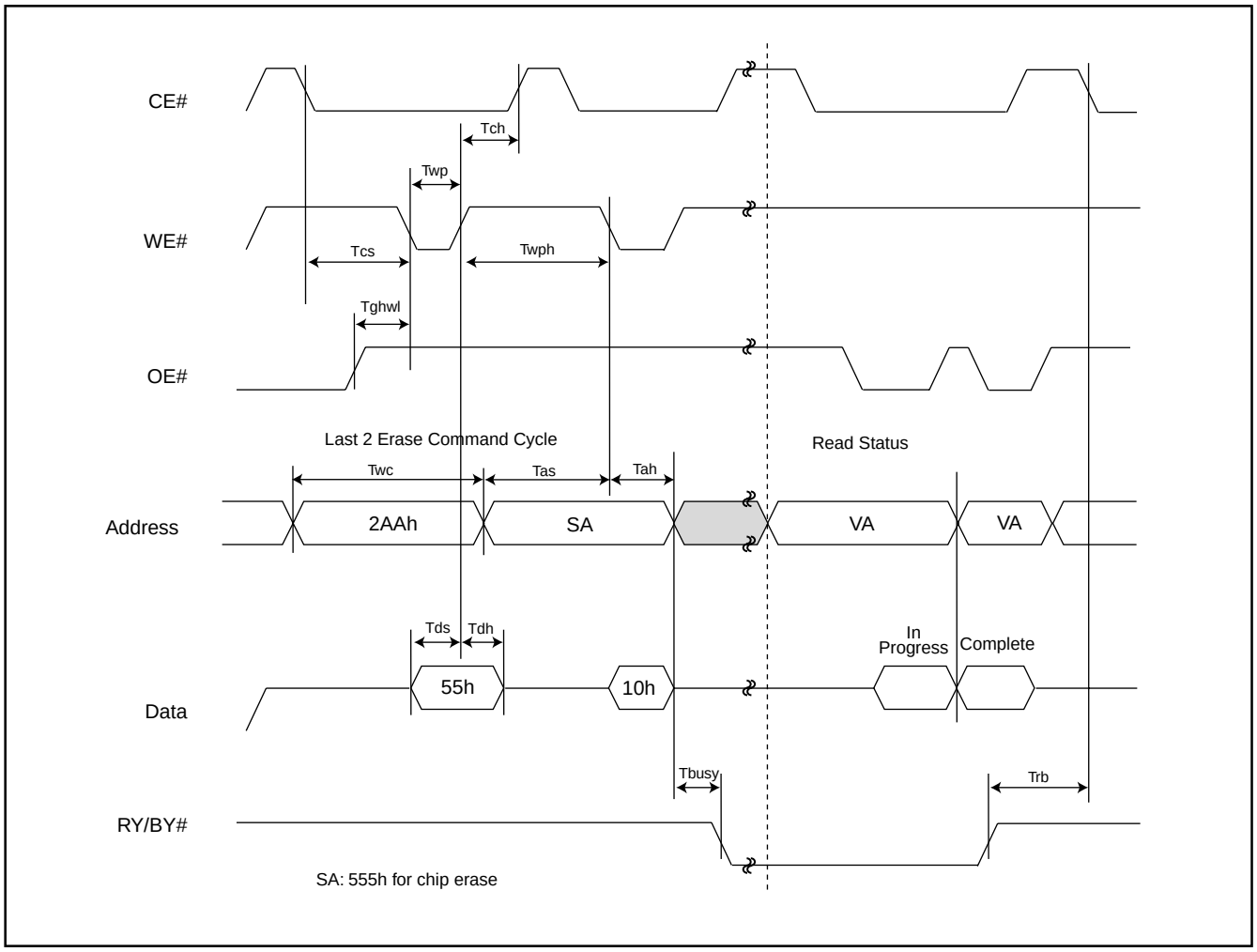


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

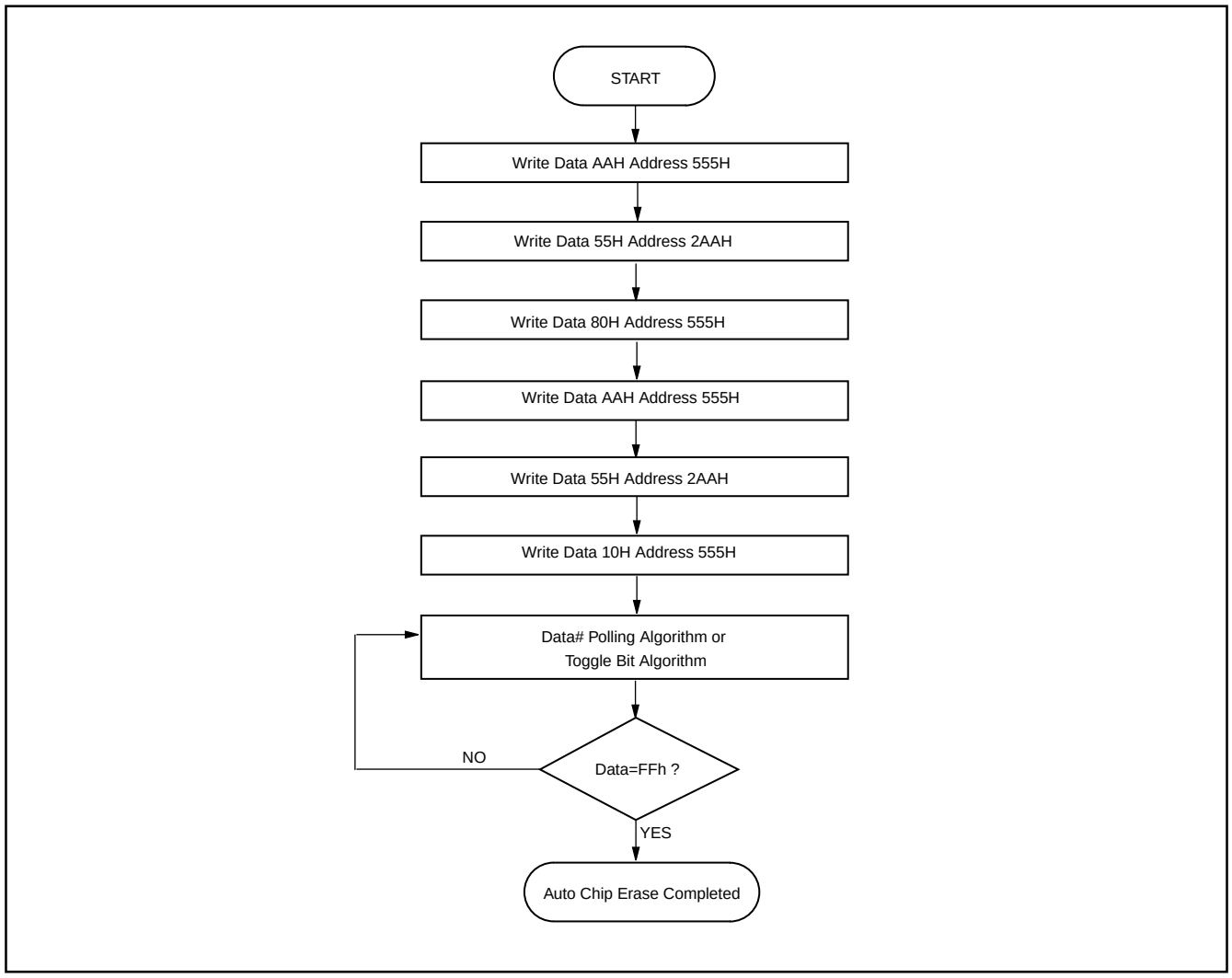


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

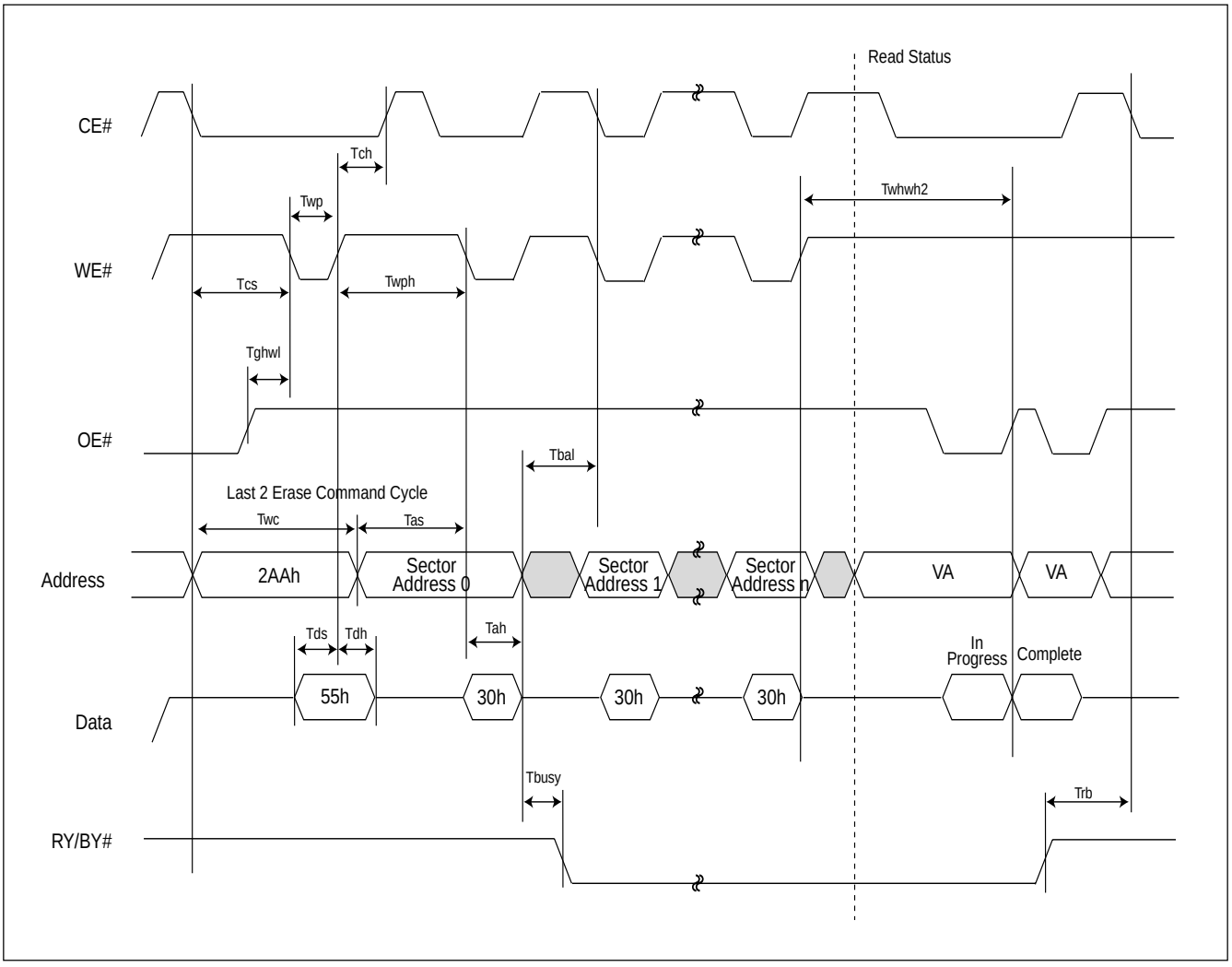


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

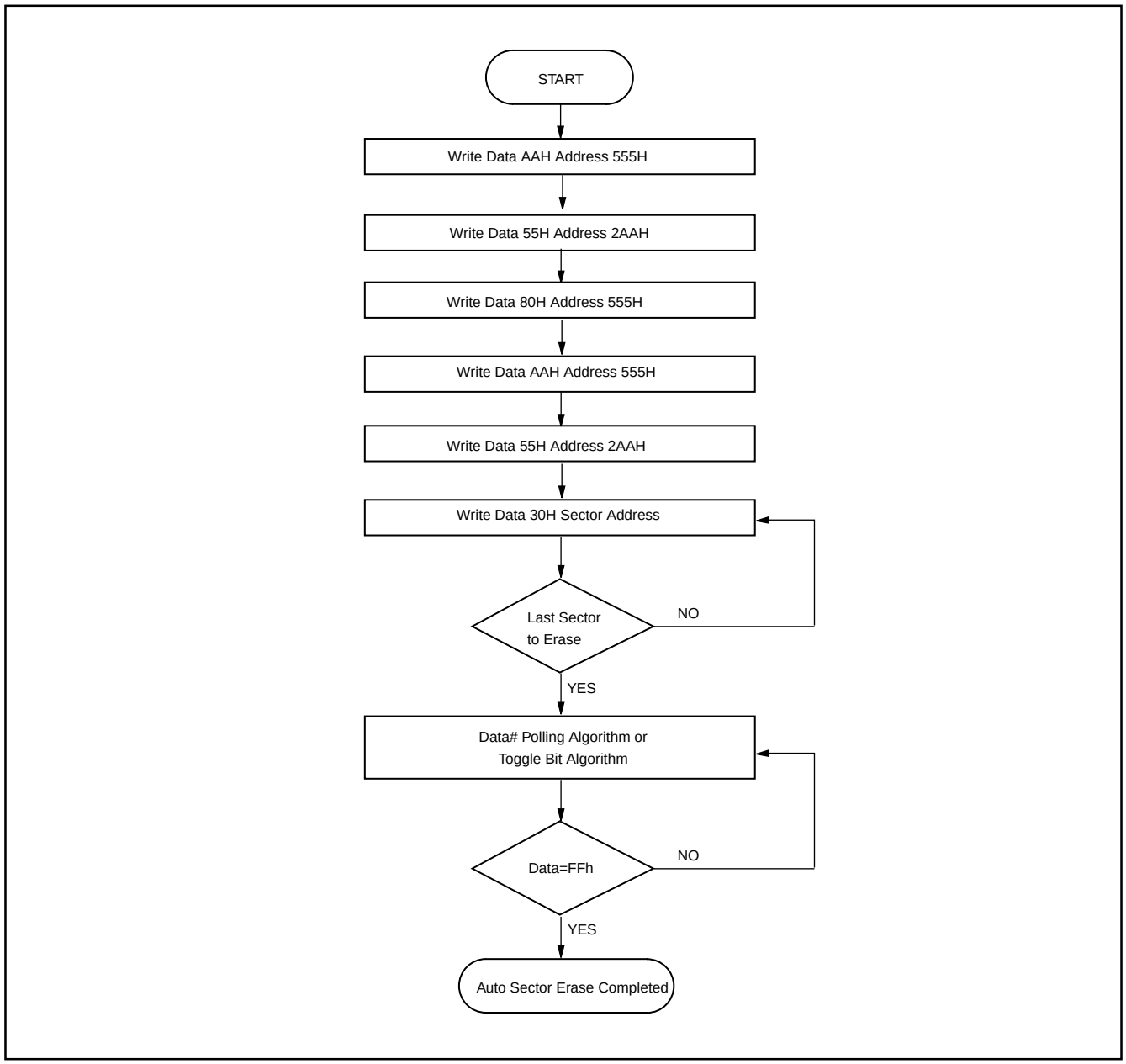


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

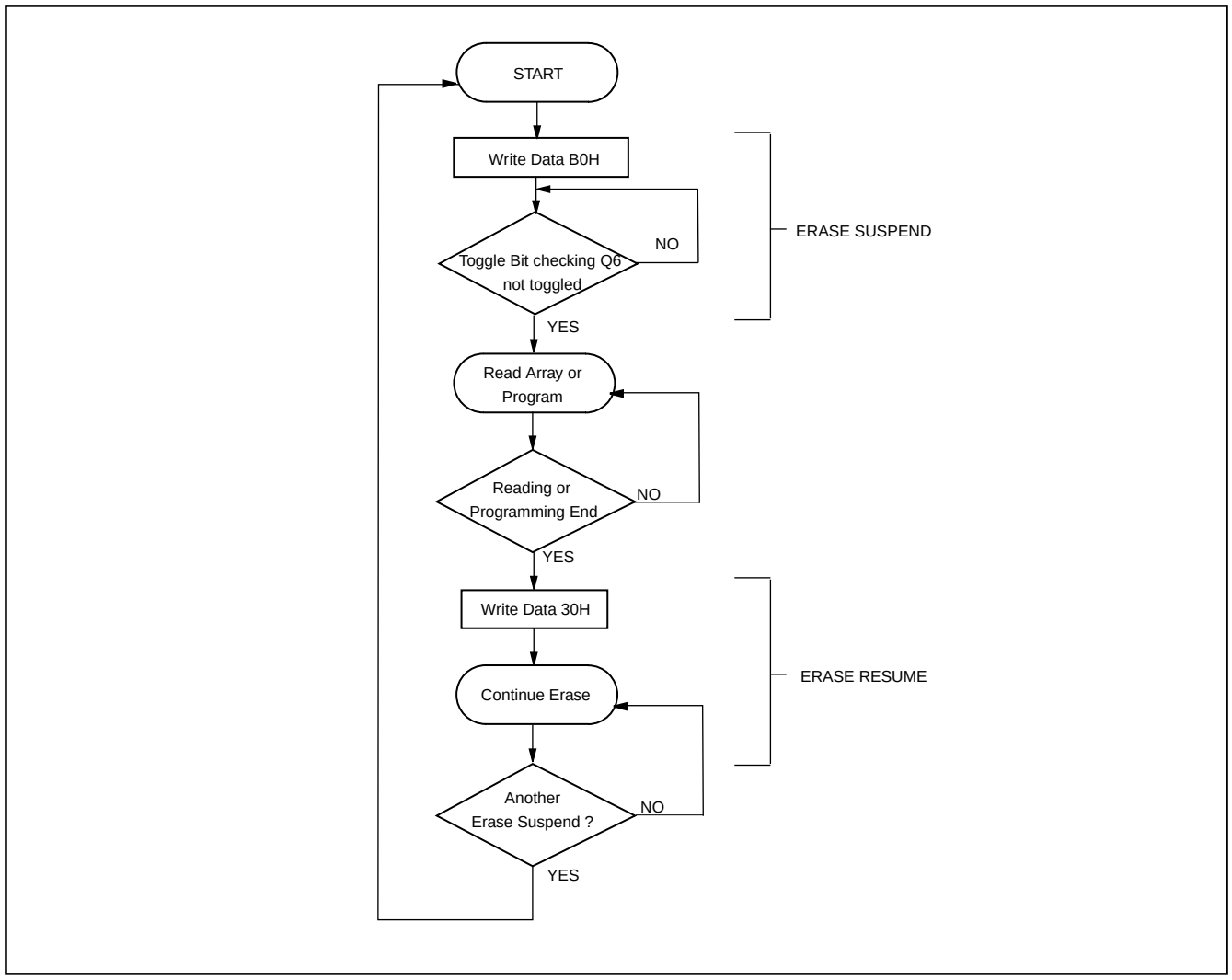


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

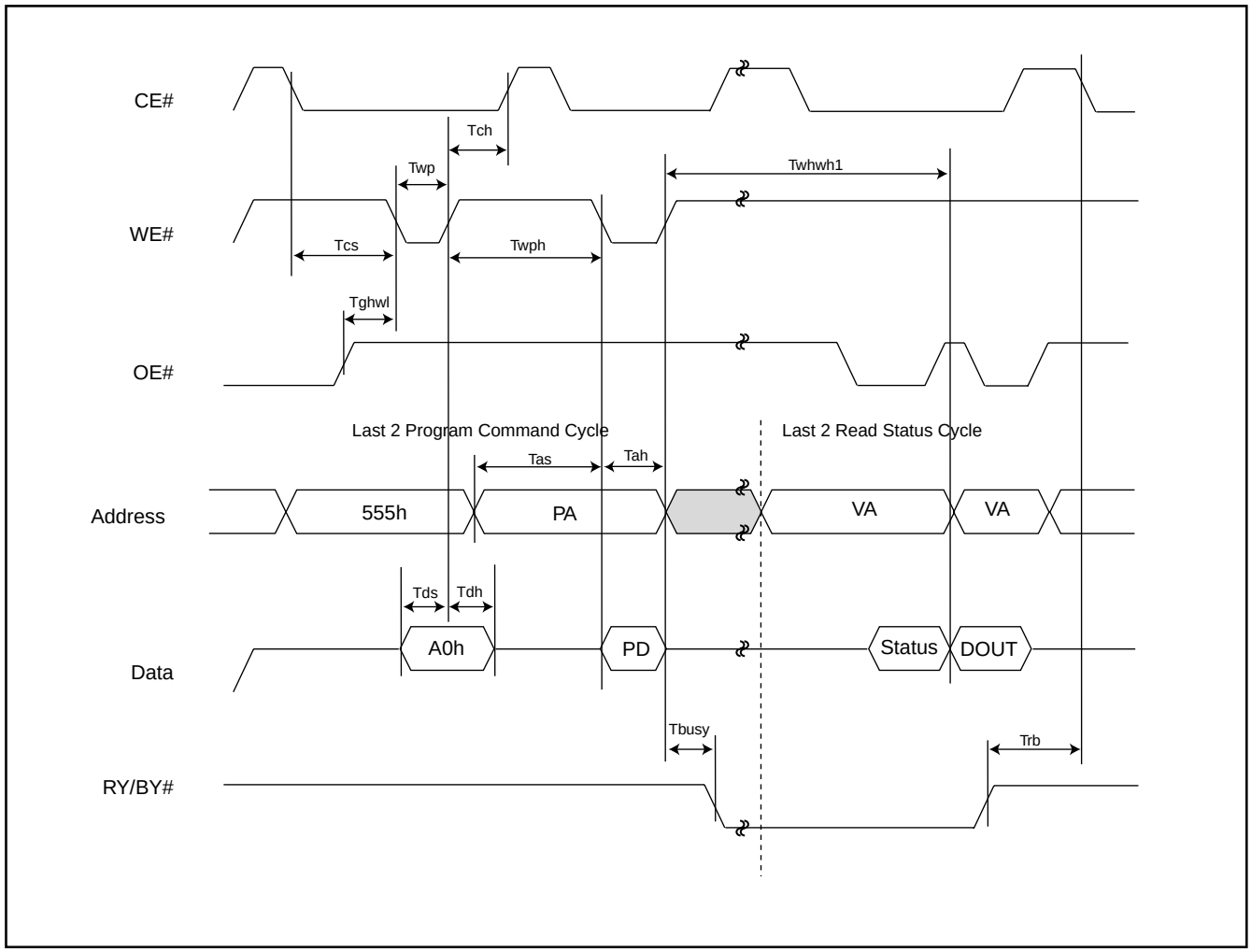


Figure 10. Accelerated Program Timing Diagram

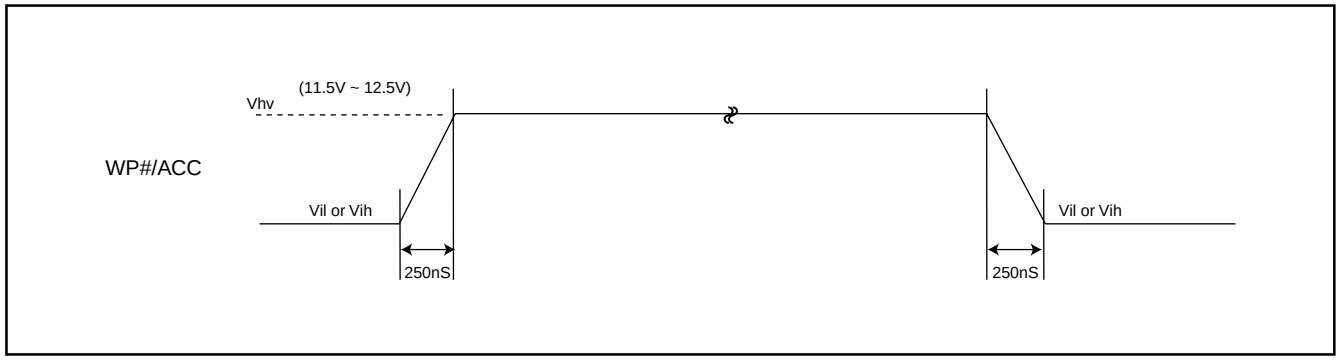


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

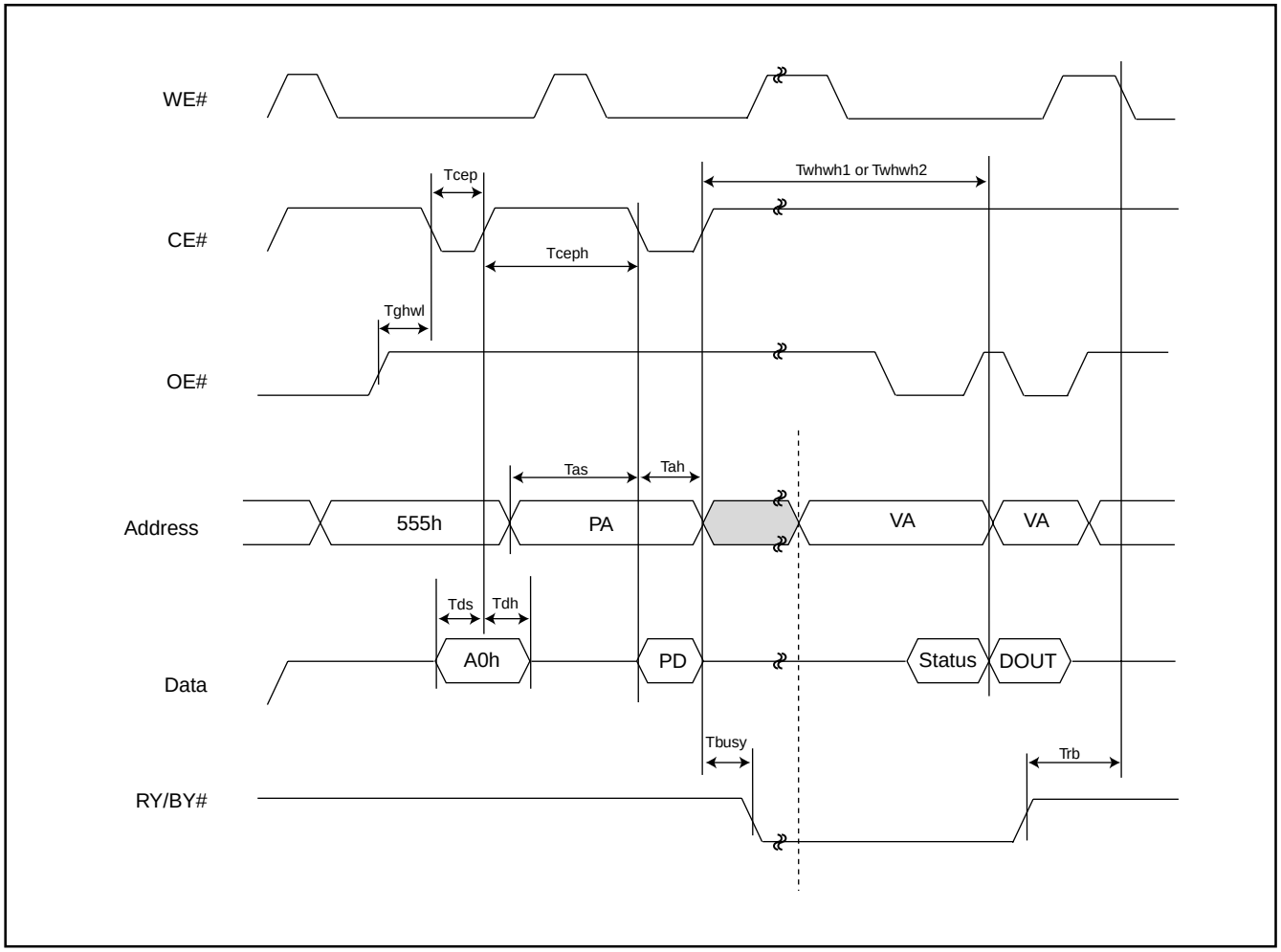
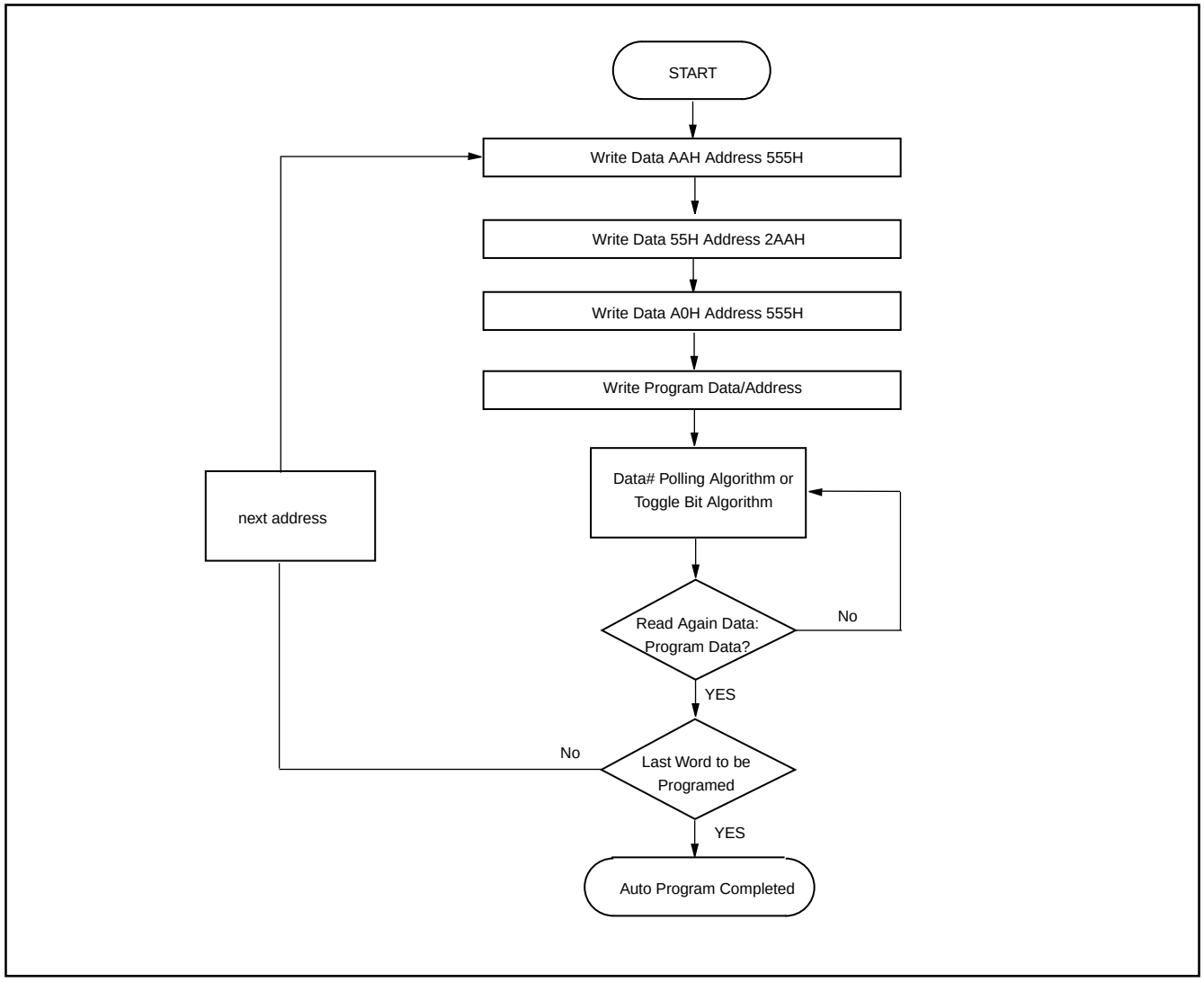


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 13. Sector Group Protect/Chip Unprotect Waveform (RESET# Control)

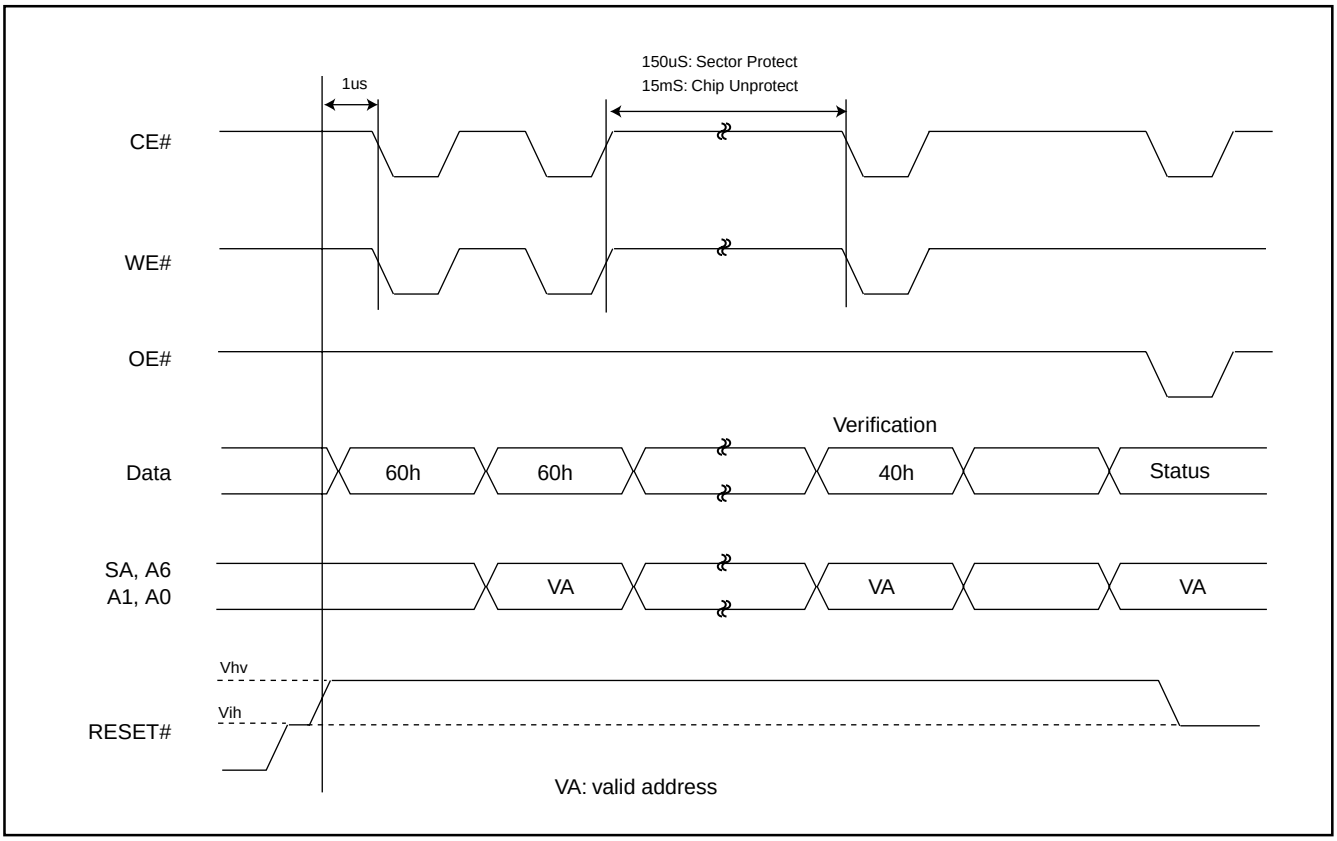


Figure 14-1. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv

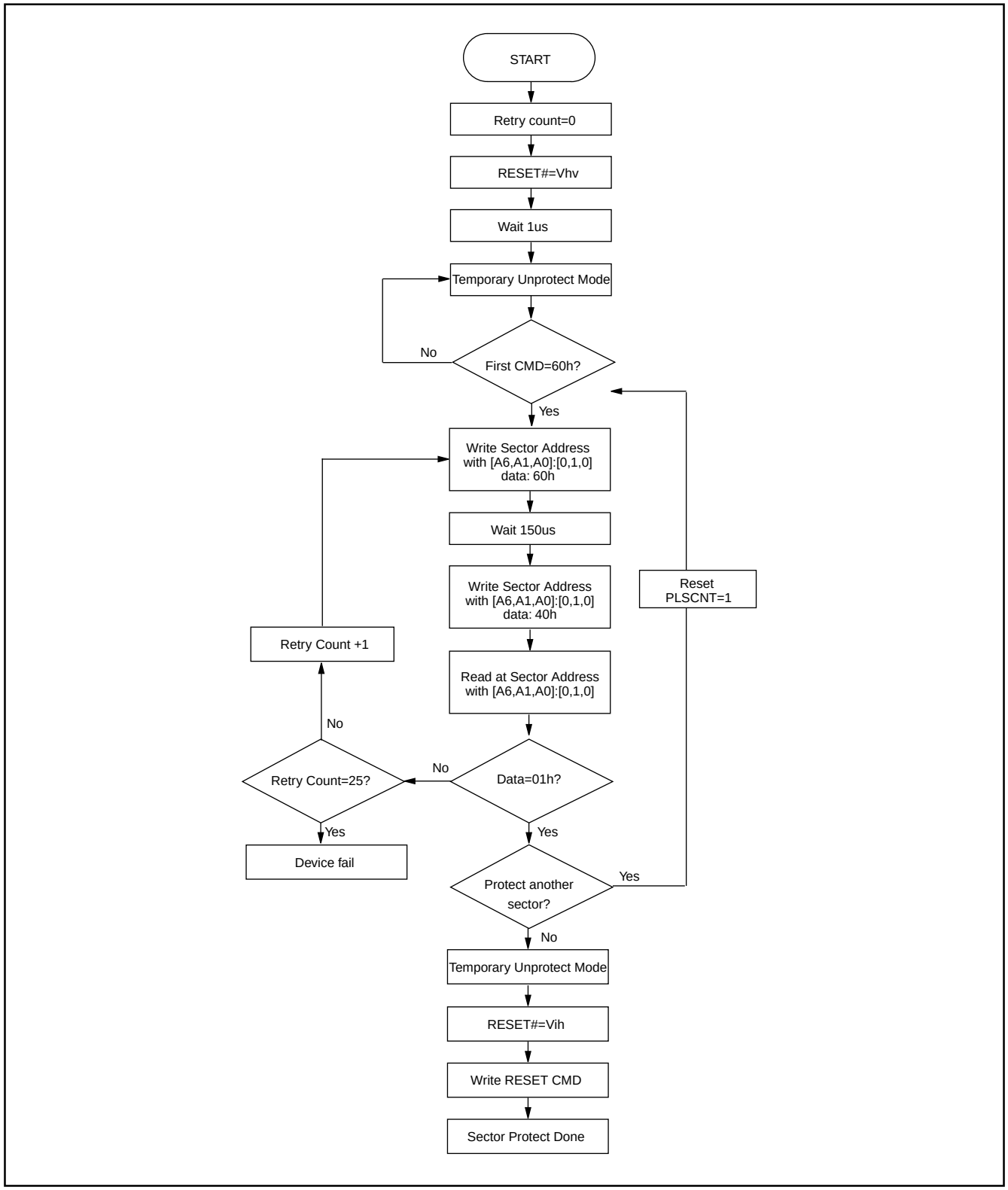


Figure 14-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

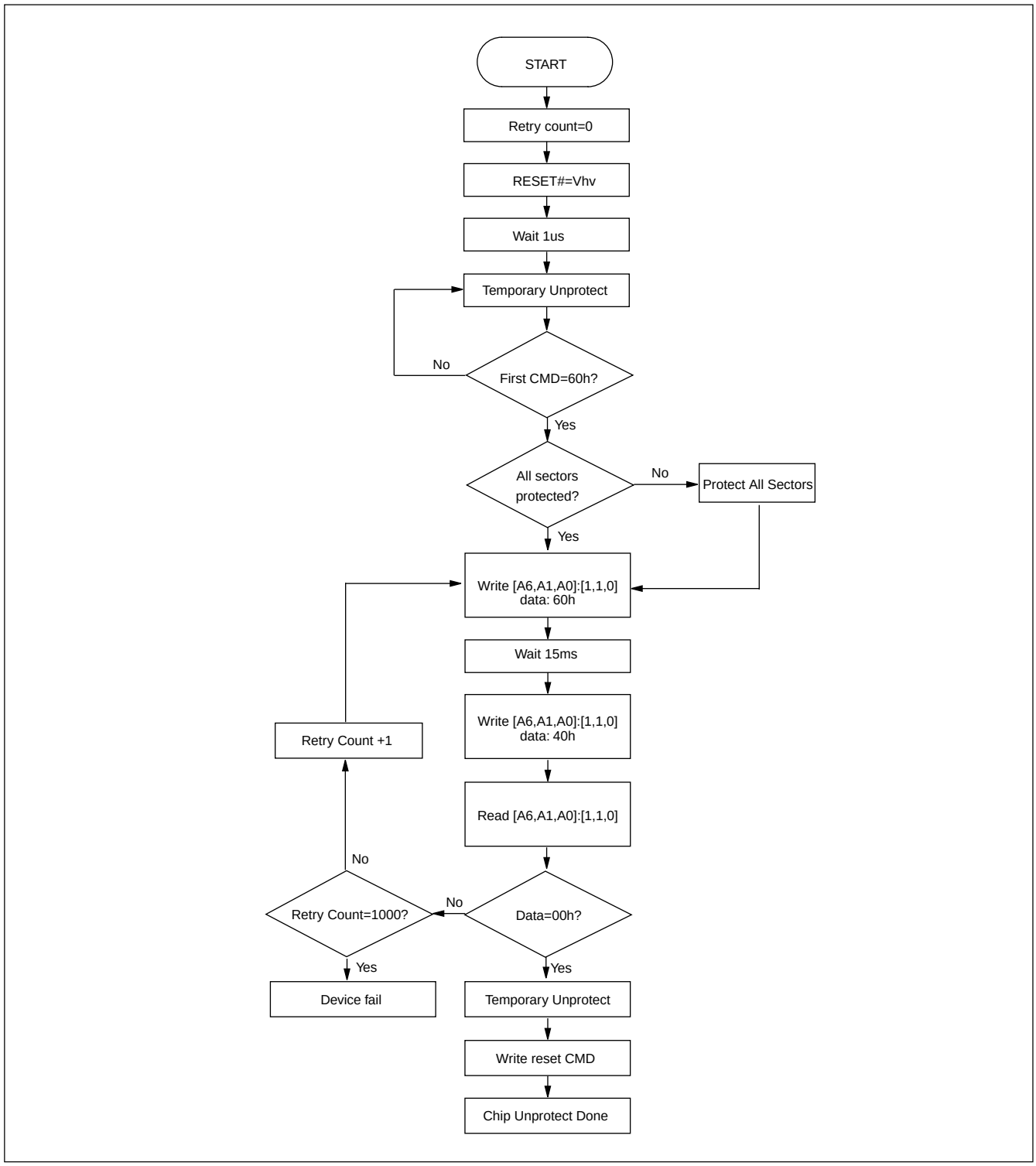


Table 5. TEMPORARY SECTOR GROUP UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	nS
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	uS

Figure 15. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

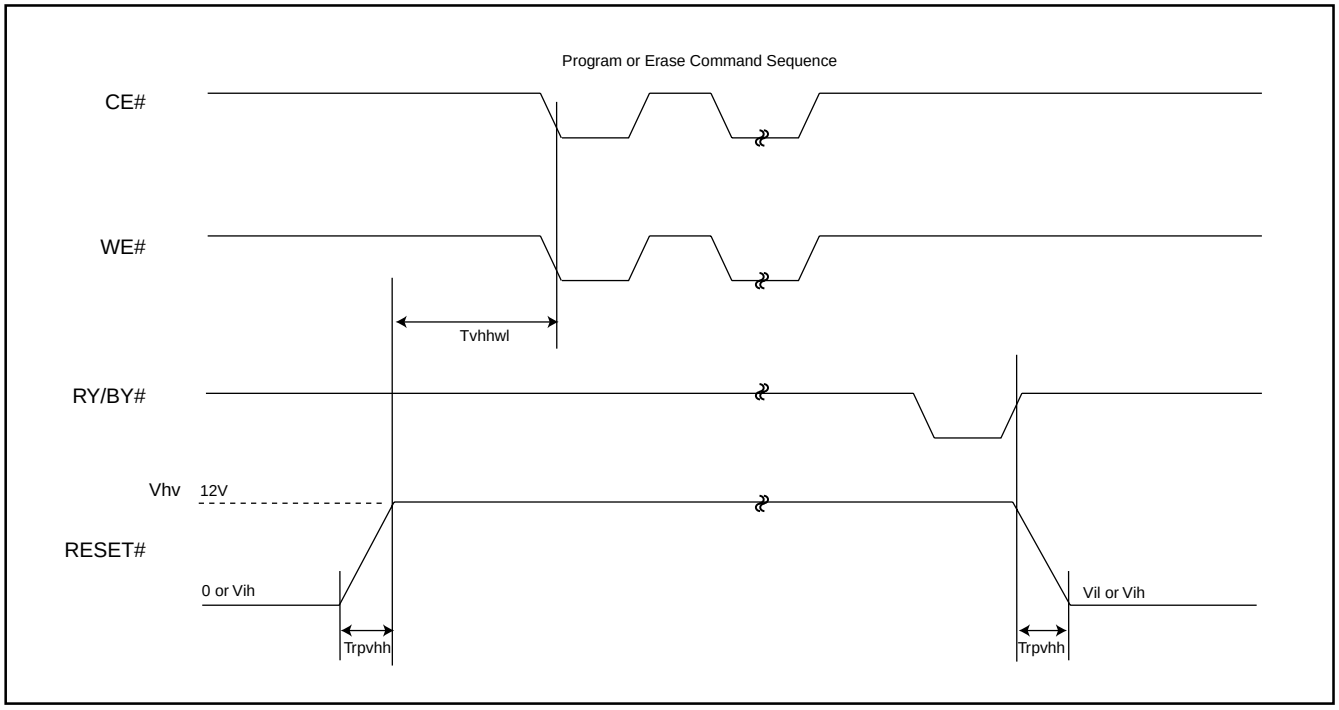
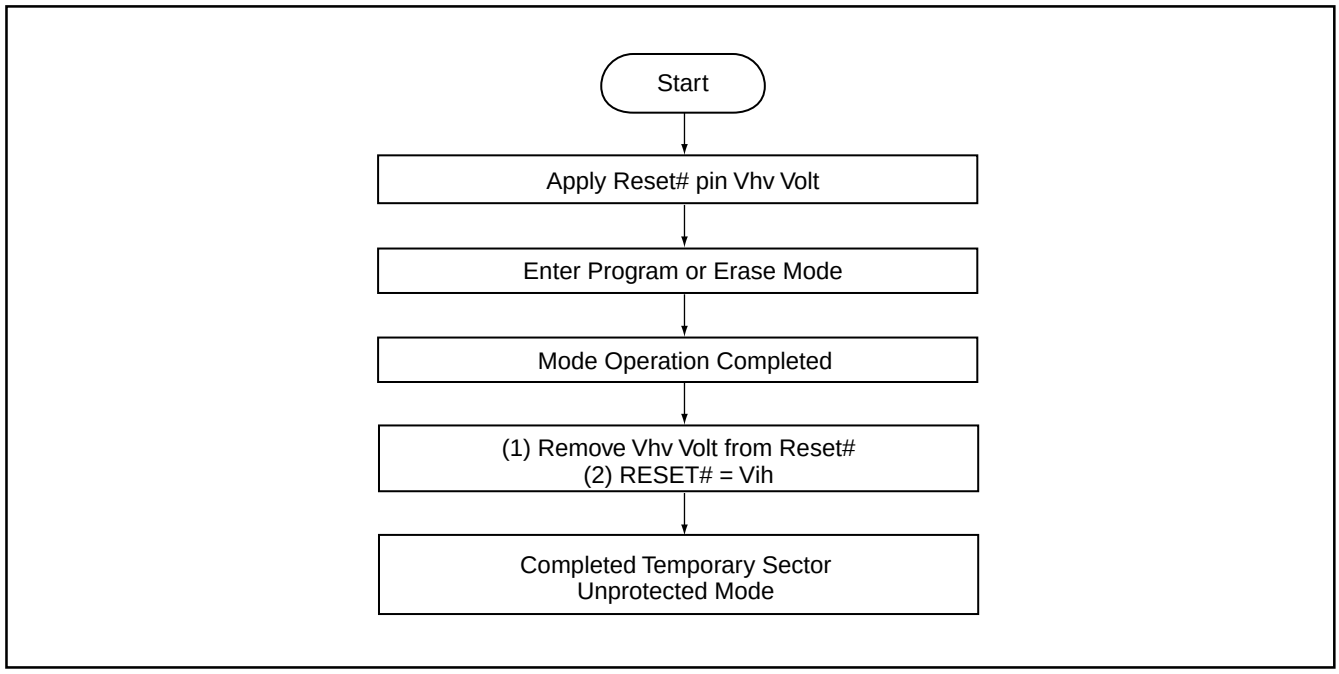
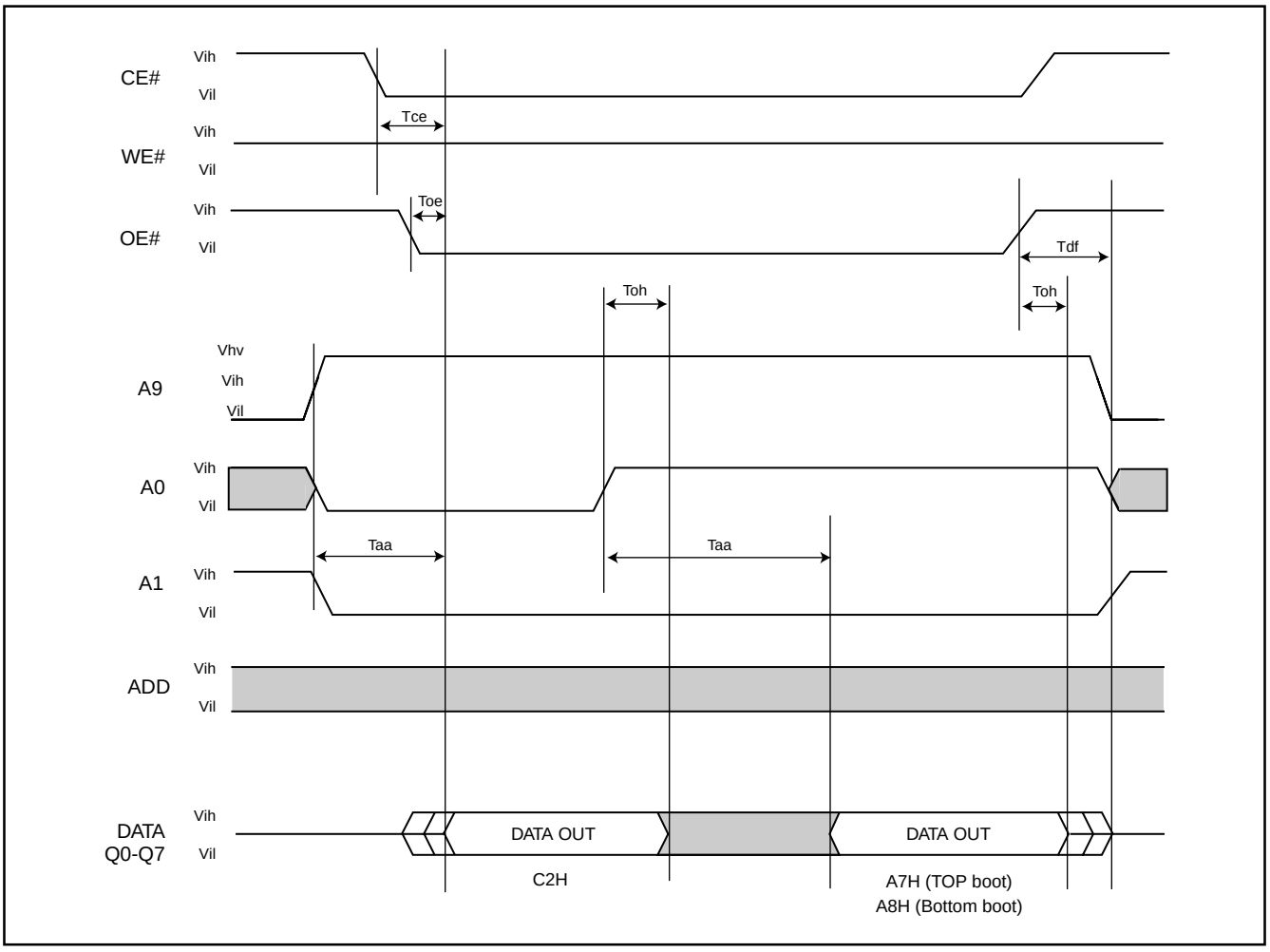


Figure 16. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=11.5~12.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 17. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 18. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

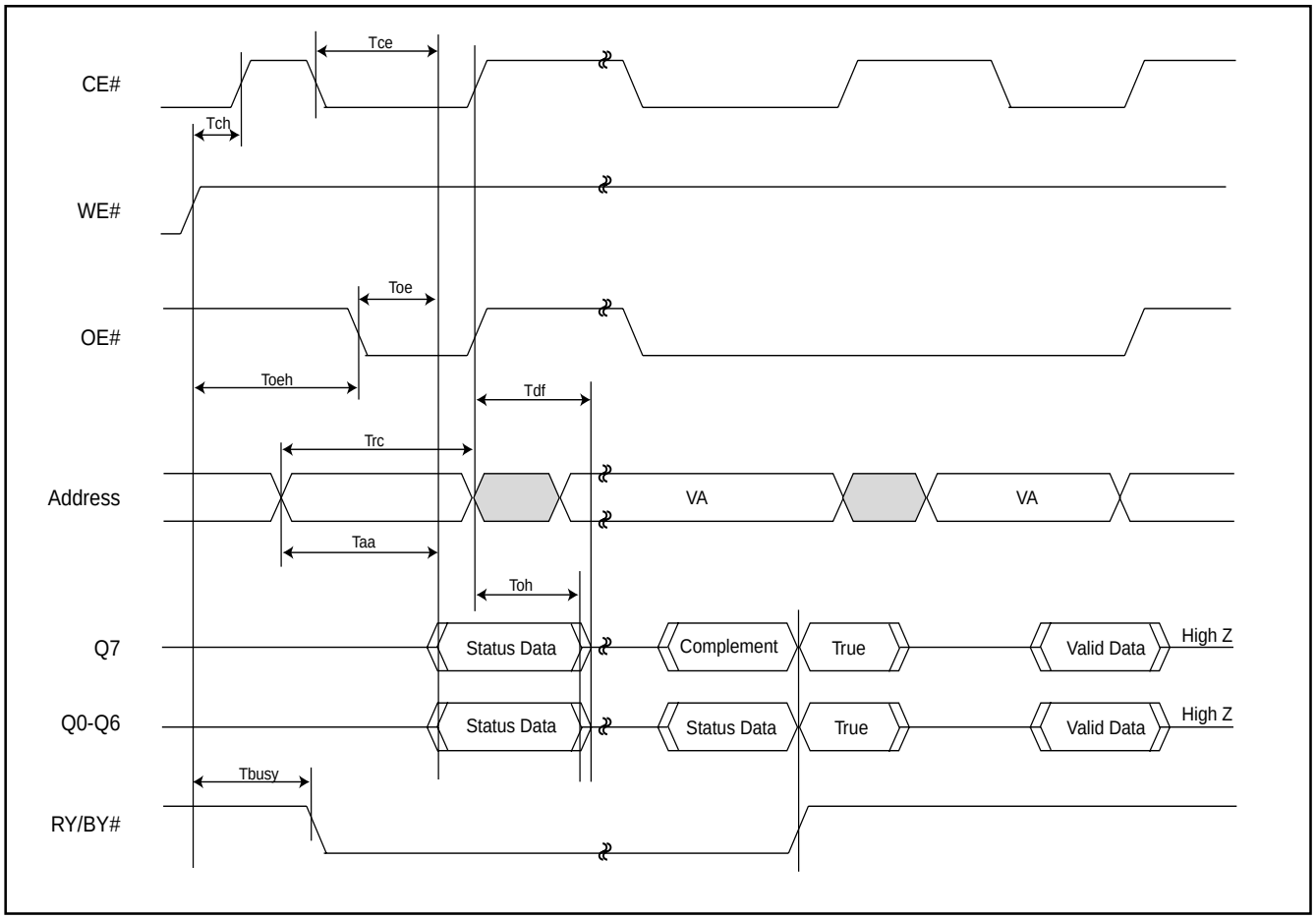
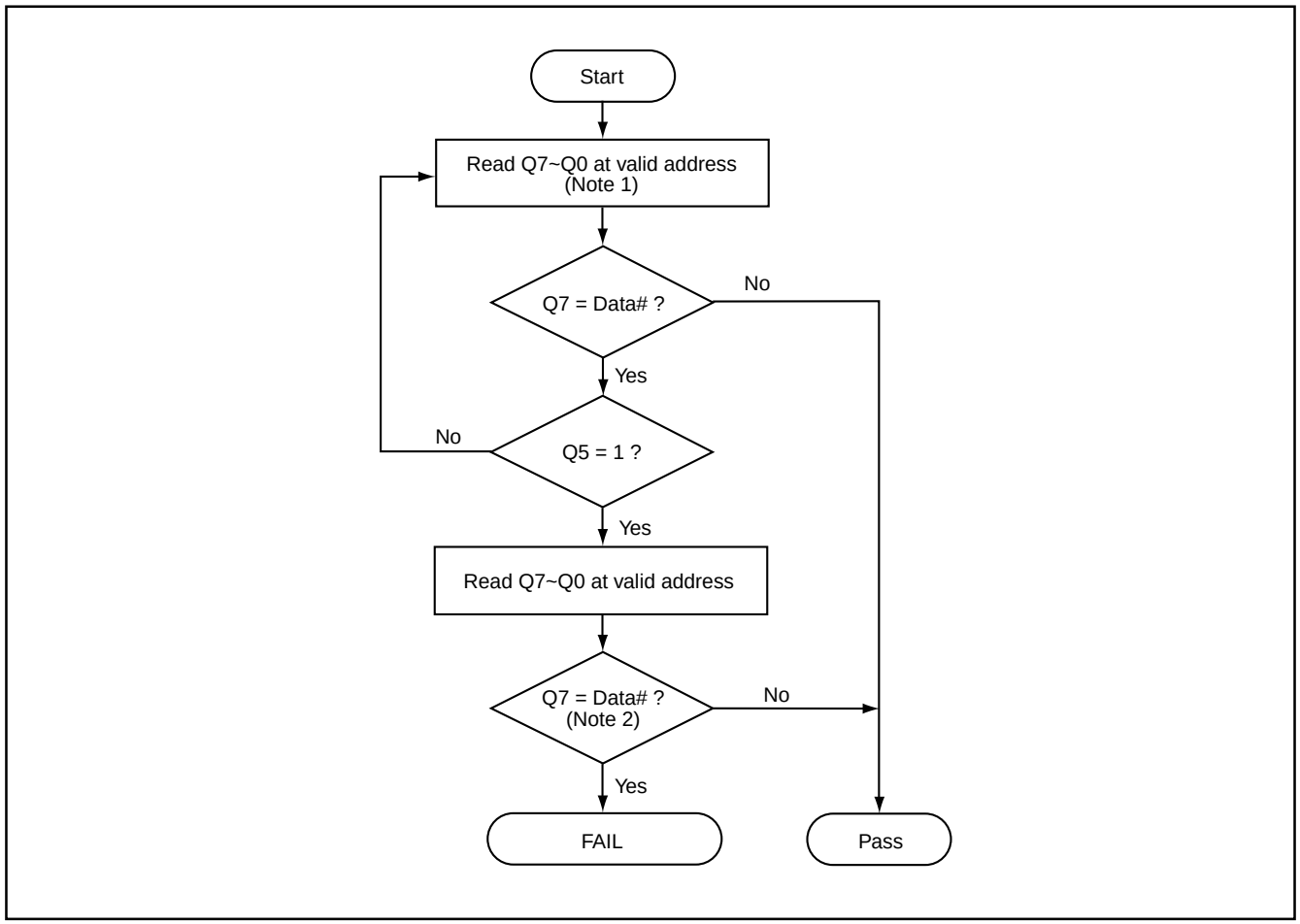


Figure 19. Data# Polling Algorithm



Notes:
1. For programming, valid address meas program address.
   For erasing, valid address meas erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

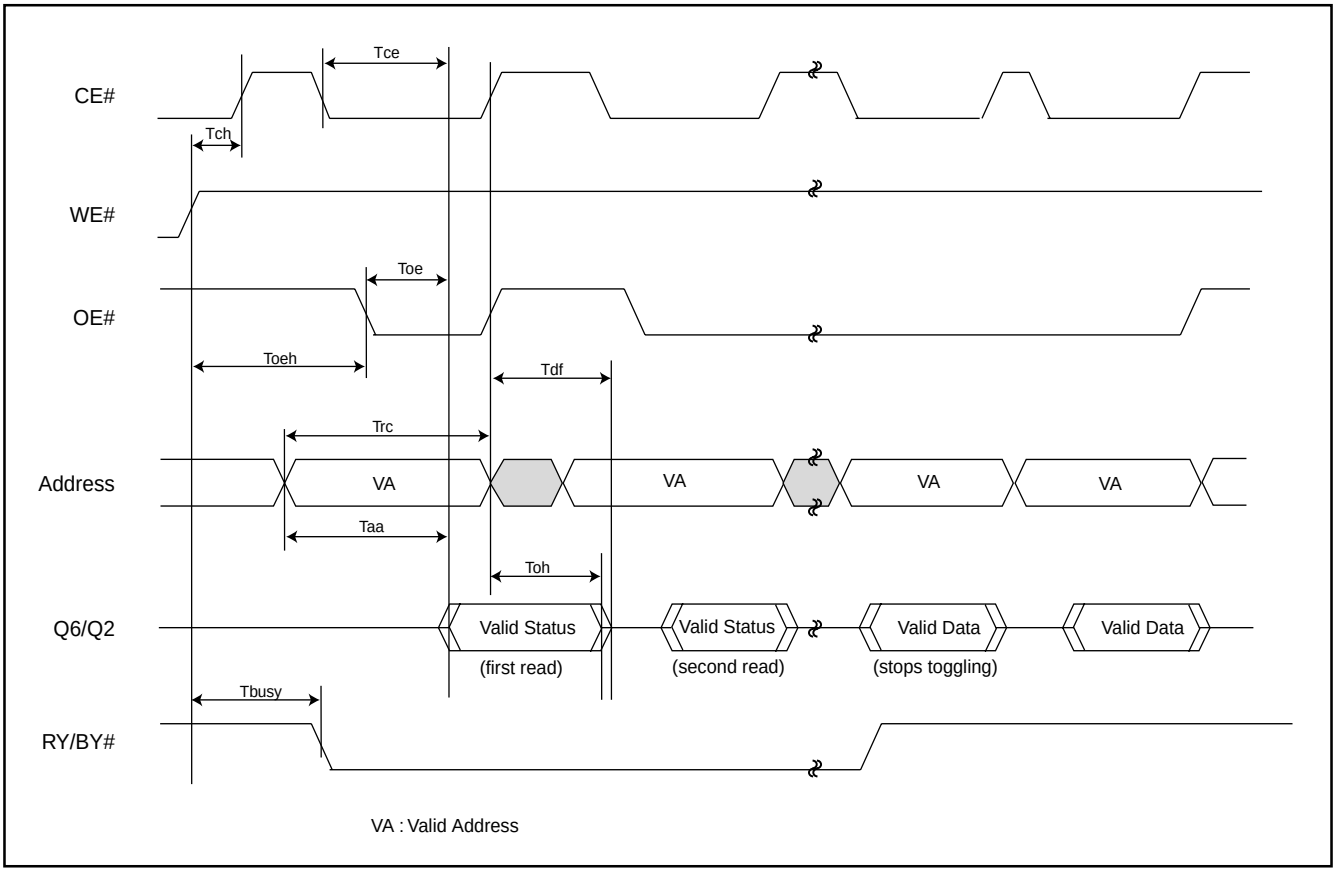
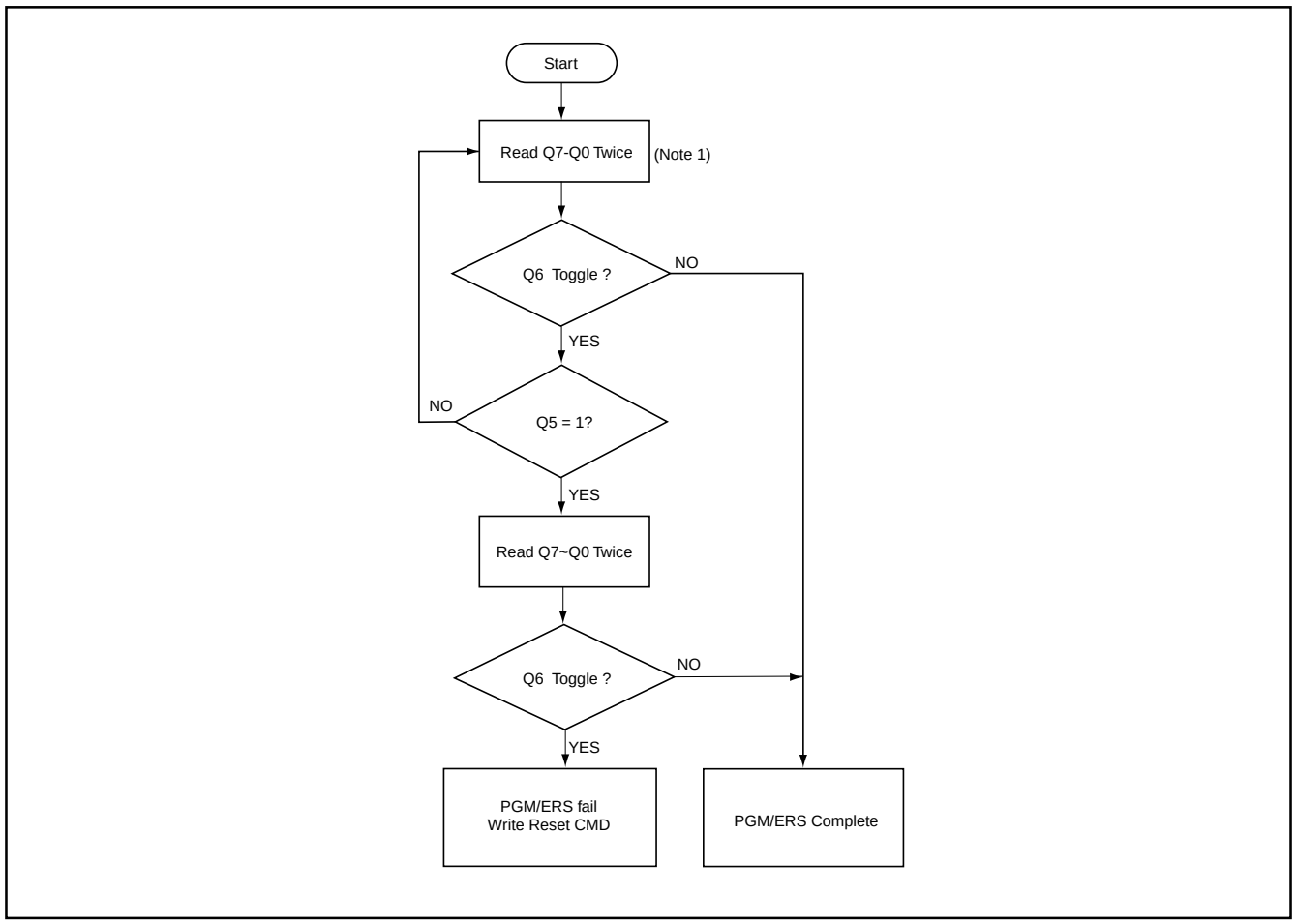


Figure 21. Toggle Bit Algorithm



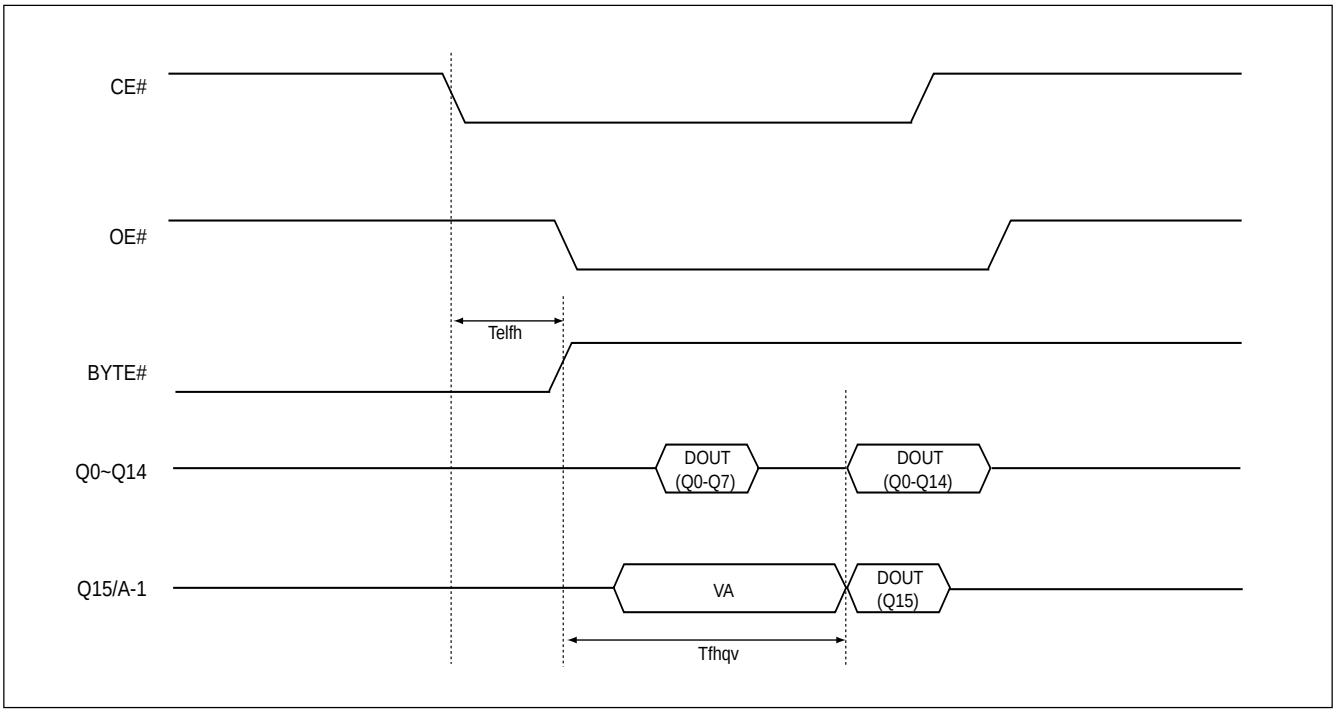
Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

AC CHARACTERISTICS

WORD/BYTE CONFIGURATION (BYTE#)

Parameter	Description		Speed Options		Unit
			-70	-90	
Telfl/Telfh	CE# to BYTE# from L/H	MAX	5	5	nS
Tflqz	BYTE# from L to Output Hiz	MAX	25	30	nS
Tfhqv	BYTE# from H to Output Active	MIN	70	90	nS

Figure 22. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

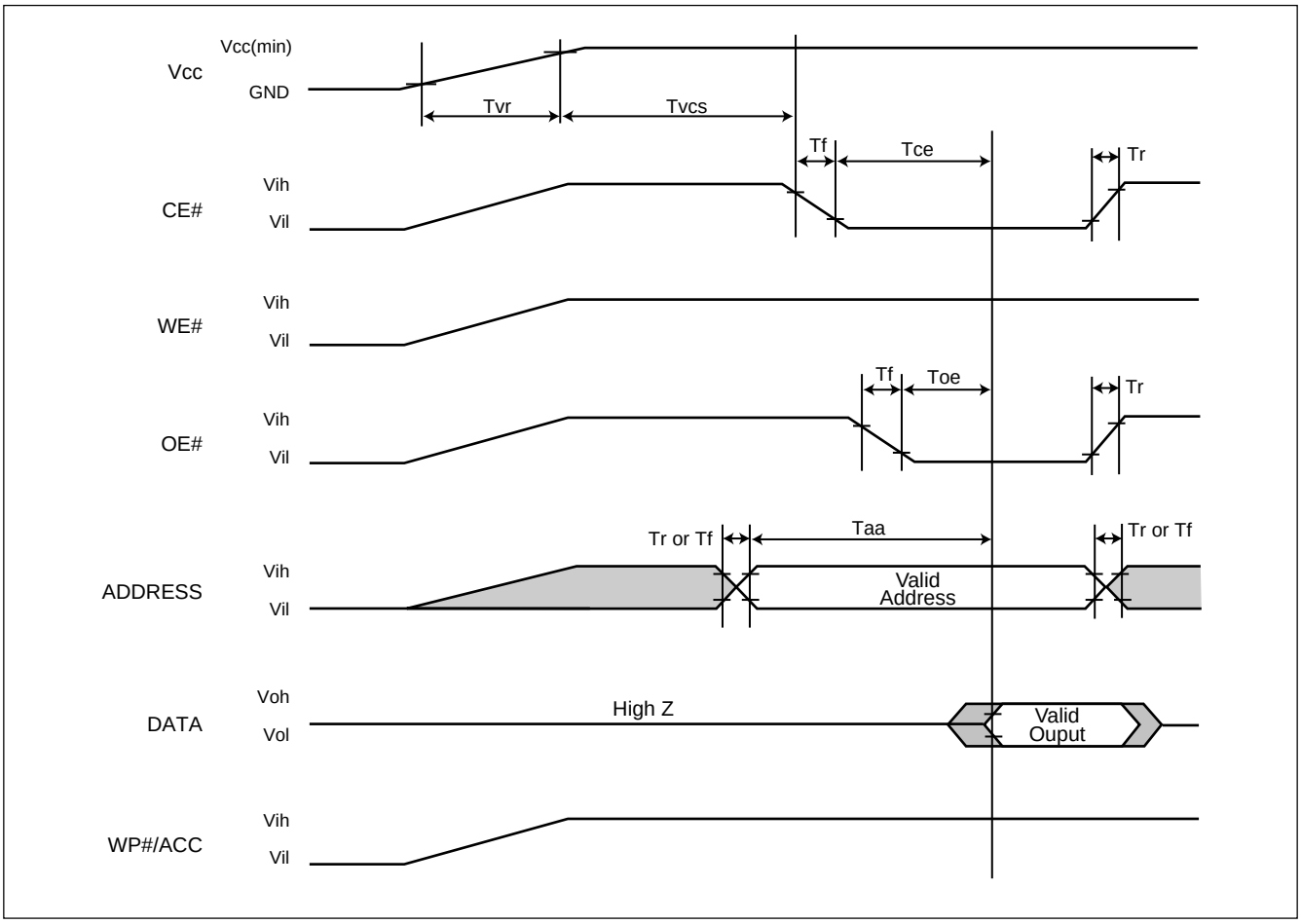


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	uS/V
Tr	Input Signal Rise Time		20	uS/V
Tf	Input Signal Fall Time		20	uS/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		LIMITS MIN.	TYP.	MAX.	UNITS
Chip Erase Time			35	50	sec
Sector Erase Time			0.9	15	sec
Erase/Program Cycles		100,000			Cycles
Chip Programming Time	Byte Mode		36	108	sec
	Word Mode		24	72	sec
Accelerated Byte/Word Program Time			7	210	uS
Word Program Time			11	360	uS
Byte Programming Time			9	300	uS

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage voltage difference with GND on all pins except I/O pins	-1.0V	12.5V
Input Voltage voltage difference with GND on all I/O pins	-1.0V	Vcc + 1.0V
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

TSOP PIN CAPACITANCE

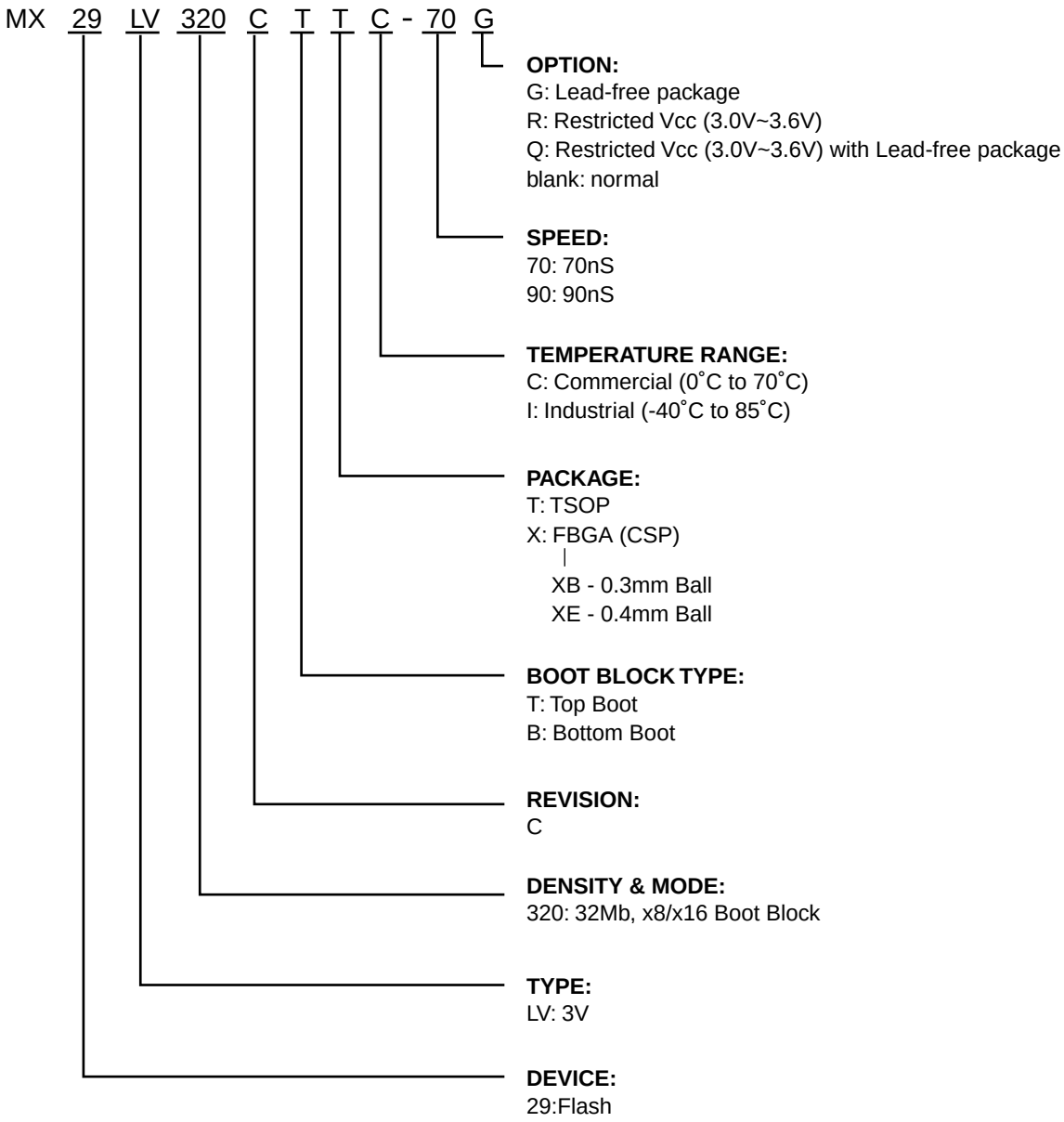
Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball Size	PACKAGE	Remark
MX29LV320CTTC-70	70	-	48 Pin TSOP	
MX29LV320CBTC-70	70	-	48 Pin TSOP	
MX29LV320CTTI-70	70	-	48 Pin TSOP	
MX29LV320CBTI-70	70	-	48 Pin TSOP	
MX29LV320CTTC-90	90	-	48 Pin TSOP	
MX29LV320CBTC-90	90	-	48 Pin TSOP	
MX29LV320CTTI-90	90	-	48 Pin TSOP	
MX29LV320CBTI-90	90	-	48 Pin TSOP	
MX29LV320CTXBC-70	70	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CBXBC-70	70	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CTXEC-70	70	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CBXEC-70	70	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CTXBI-70	70	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CBXBI-70	70	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CTXEI-70	70	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CBXEI-70	70	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CTXBC-90	90	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CBXBC-90	90	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CTXEC-90	90	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CBXEC-90	90	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CTXBI-90	90	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CBXBI-90	90	0.8mm/0.3mm	48-Ball CSP	
MX29LV320CTXEI-90	90	0.8mm/0.4mm	48-Ball CSP	
MX29LV320CBXEI-90	90	0.8mm/0.4mm	48-Ball CSP	

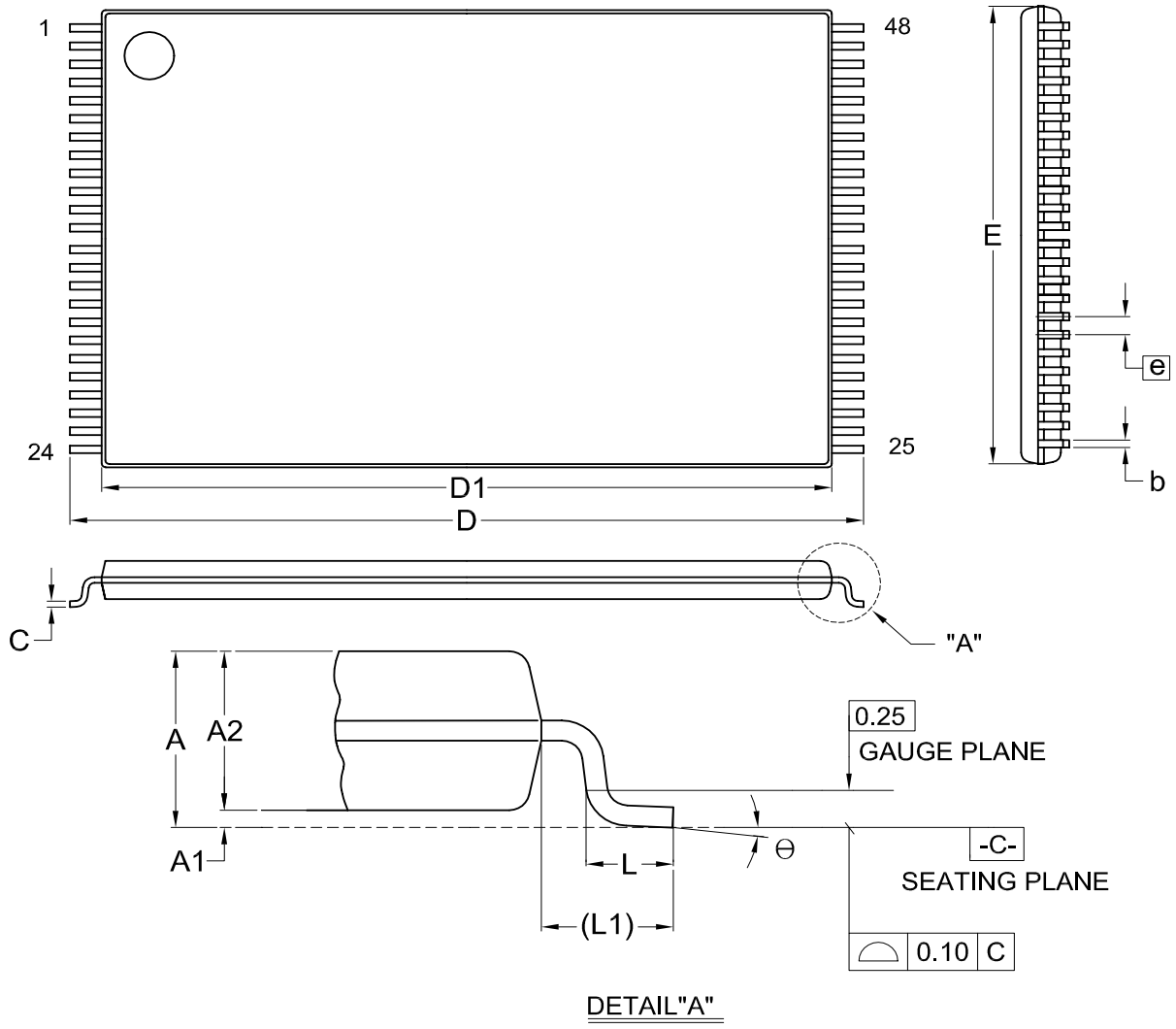
PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball Size	PACKAGE	Remark
MX29LV320CTTC-70G	70	-	48 Pin TSOP	Pb-free
MX29LV320CBTC-70G	70	-	48 Pin TSOP	Pb-free
MX29LV320CTTI-70G	70	-	48 Pin TSOP	Pb-free
MX29LV320CBTI-70G	70	-	48 Pin TSOP	Pb-free
MX29LV320CTTC-90G	90	-	48 Pin TSOP	Pb-free
MX29LV320CBTC-90G	90	-	48 Pin TSOP	Pb-free
MX29LV320CTTI-90G	90	-	48 Pin TSOP	Pb-free
MX29LV320CBTI-90G	90	-	48 Pin TSOP	Pb-free
MX29LV320CTXBC-70G	70	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CBXBC-70G	70	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CTXEC-70G	70	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CBXEC-70G	70	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CTXBI-70G	70	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CBXBI-70G	70	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CTXEI-70G	70	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CBXEI-70G	70	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CTXBC-90G	90	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CBXBC-90G	90	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CTXEC-90G	90	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CBXEC-90G	90	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CTXBI-90G	90	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CBXBI-90G	90	0.8mm/0.3mm	48-Ball CSP	Pb-free
MX29LV320CTXEI-90G	90	0.8mm/0.4mm	48-Ball CSP	Pb-free
MX29LV320CBXEI-90G	90	0.8mm/0.4mm	48-Ball CSP	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM

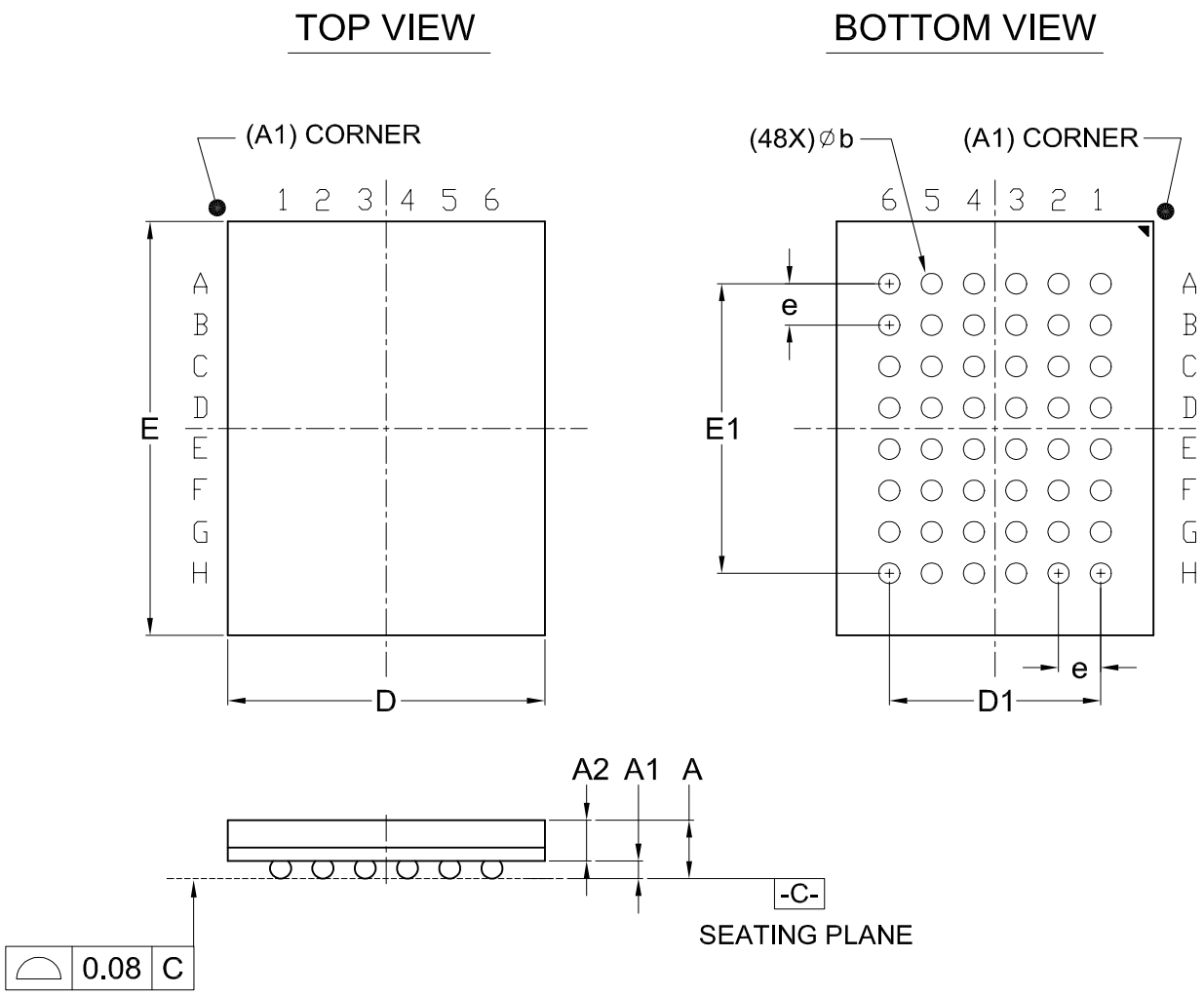


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

Title: **Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)**



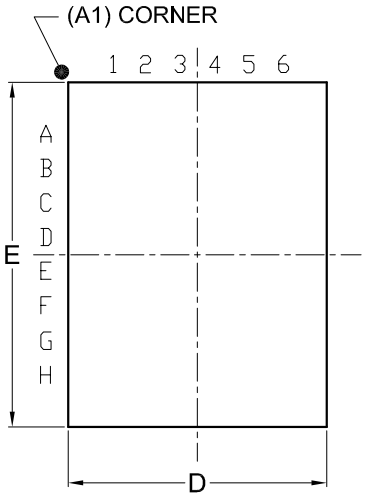
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.18	0.65	0.25	5.90		7.90		
	Nom.	---	0.23	---	0.30	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.28	---	0.35	6.10		8.10		
Inch	Min.	---	0.007	0.026	0.010	0.232		0.311		
	Nom.	---	0.009	---	0.012	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.011	---	0.014	0.240		0.319		

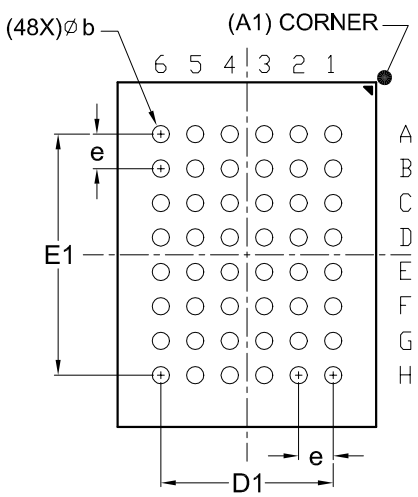
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4201	6	MO-210			03-29-'06

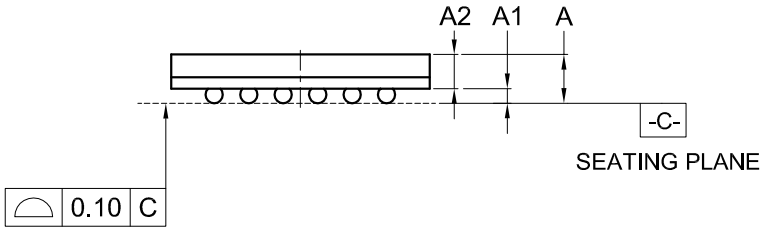
Title: **Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)**

TOP VIEW



BOTTOM VIEW





Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	—	0.010	0.026	0.014	0.232		0.311		
	Nom.	—	0.012	—	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	—	0.018	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4202	4	MO-219			12-12-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary"	P1	AUG/02/2005
	2. Added "Pb-free devices are RoHS Compliant"	P1	
1.1	1. Modified tWES-->tWS; tWEH-->tWH	P30	MAR/29/2006
	2. Added note 2	P30	
1.2	1. Modified tVCS	P30	MAY/26/2006
1.3	1. Datasheet format changed	All	AUG/15/2006
1.4	1. Data modification	All	AUG/17/2005
1.5	1. Added statement	P60	NOV/06/2006

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

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