# MX29LV065B

## 64M-BIT [8M x 8] CMOS EQUAL SECTOR FLASH MEMORY

## FEATURES

### GENERAL FEATURES

- 8,388,608 x 8 byte structure
- One hundred twenty-eight Equal Sectors with 64K byte each
  - Any combination of sectors can be erased with erase suspend/resume function
- Sector Protection/Chip Unprotected
  - Provides sector group protect function to prevent pro gram or erase operation in the protected sector group
  - Provides chip unprotected function to allow code changing
  - Provides temporary sector group unprotected function for code changing in previously protected sector groups
- Secured Silicon Sector
  - Provides a 128-byte area for code or data that can be permanently protected.
  - Once this sector is protected, it is prohibited to program or erase within the sector again.
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit is equal to or less than 2.5V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

### PERFORMANCE

- High Performance
  - Fast access time: 90/120ns
  - Fast program time: 7us, 42s/chip (typical)
  - Fast erase time: 0.9s/sector, 45s/chip (typical)
- Low Power Consumption
  - Low active read current: 9mA (typical) at 5MHz
  - Low standby current: 0.2uA(typ.)
- Minimum 100,000 erase/program cycle
- 20-years data retention

### SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access.
- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion

### HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- ACC pin
  - Accelerates programming time for higher throughput during system production

### PACKAGE

- 48-pin TSOP
- **All Pb-free devices are RoHS Compliant**

## GENERAL DESCRIPTION

The MX29LV065B is a 64-mega bit Flash memory organized as 8M bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write nonvolatile random access memory. The MX29LV065B is packaged in 48-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV065B offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV065B has separate chip enable (CE#) and output enable (OE#) controls.

MXIC's Flash memories augment EPROM functionality

with in-circuit electrical erasure and programming. The MX29LV065B uses a command register to manage this functionality.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29LV065B uses a 3.0V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

## AUTOMATIC PROGRAMMING

The MX29LV065B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29LV065B is less than 42sec.

## AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to Data# Polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

## AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 205 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

## AUTOMATIC SECTOR ERASE

The MX29LV065B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

## AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

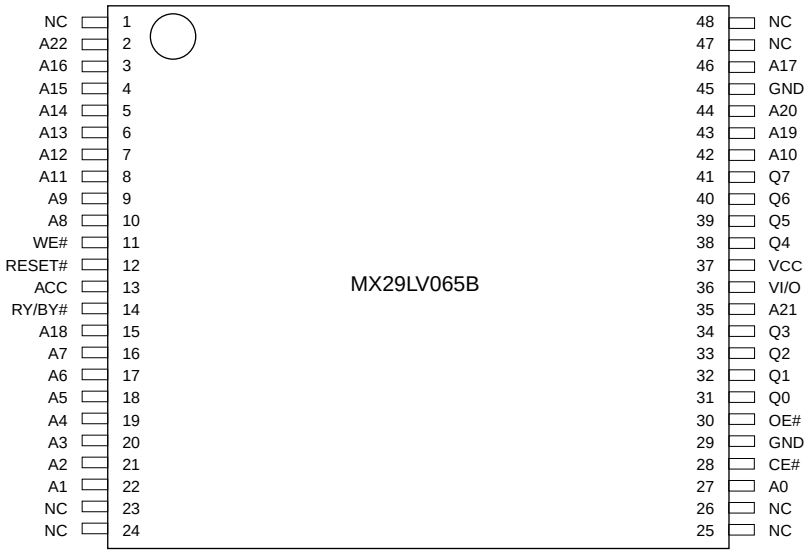
Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE# .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV065B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

## PIN CONFIGURATION

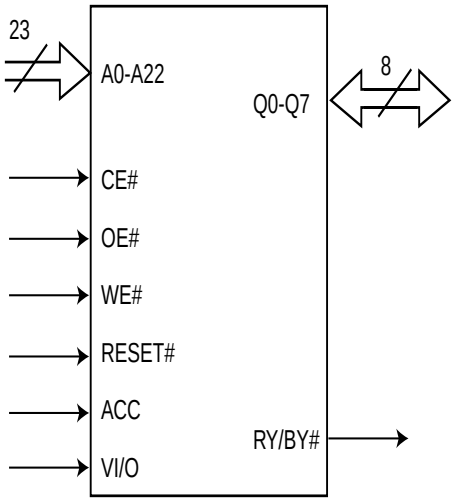
### 48 TSOP



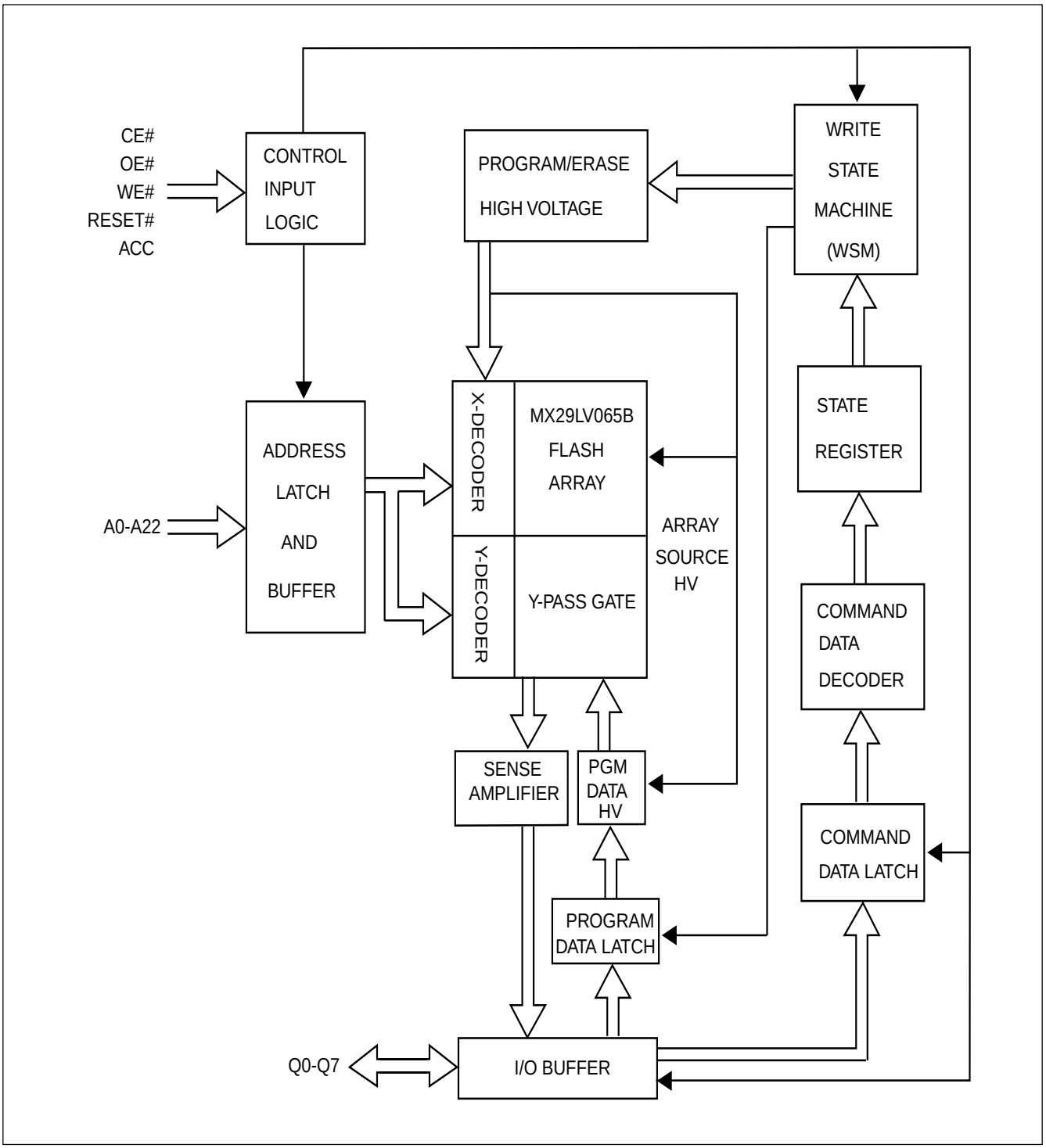

## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| A0~A22 | Address Input |
| Q0~Q7 | 8 Data Inputs/Outputs |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| RESET# | Hardware Reset Pin, Active Low |
| ACC | Programming Acceleration Input |
| RY/BY# | Read/Busy Output |
| VCC | +3.0V single power supply |
| VI/O | Input/Output buffer (2.7V~3.6V) this input should be tied directly to VCC |
| GND | Device Ground |
| NC | Pin Not Connected Internally |

## LOGIC SYMBOL



## BLOCK DIAGRAM



## SECTOR (GROUP) STRUCTURE

| Sector | A22 | A21 | A20 | A19 | A18 | A17 | A16 | 8-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000-00FFFF |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 010000-01FFFF |
| SA2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 020000-02FFFF |
| SA3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 030000-03FFFF |
| SA4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 040000-04FFFF |
| SA5 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 050000-05FFFF |
| SA6 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 060000-06FFFF |
| SA7 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 070000-07FFFF |
| SA8 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 080000-08FFFF |
| SA9 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 090000-09FFFF |
| SA10 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A0000-0AFFFF |
| SA11 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B0000-0BFFFF |
| SA12 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C0000-0CFFFF |
| SA13 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D0000-0DFFFF |
| SA14 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E0000-0EFFFF |
| SA15 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F0000-0FFFFF |
| SA16 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 100000-10FFFF |
| SA17 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 110000-11FFFF |
| SA18 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 120000-12FFFF |
| SA19 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 130000-13FFFF |
| SA20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 140000-14FFFF |
| SA21 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 150000-15FFFF |
| SA22 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 160000-16FFFF |
| SA23 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 170000-17FFFF |
| SA24 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 180000-18FFFF |
| SA25 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 190000-19FFFF |
| SA26 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1A0000-1AFFFF |
| SA27 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1B0000-1BFFFF |
| SA28 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C0000-1CFFFF |
| SA29 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D0000-1DFFFF |
| SA30 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E0000-1EFFFF |
| SA31 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F0000-1FFFFF |
| SA32 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 200000-20FFFF |
| SA33 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 210000-21FFFF |
| SA34 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 220000-22FFFF |
| SA35 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 230000-23FFFF |
| SA36 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 240000-24FFFF |
| SA37 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 250000-25FFFF |

| Sector | A22 | A21 | A20 | A19 | A18 | A17 | A16 | 8-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|
| SA38 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 260000-26FFFF |
| SA39 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 270000-27FFFF |
| SA40 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 280000-28FFFF |
| SA41 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 290000-29FFFF |
| SA42 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A0000-2AFFFF |
| SA43 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B0000-2BFFFF |
| SA44 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C0000-2CFFFF |
| SA45 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D0000-2DFFFF |
| SA46 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E0000-2EFFFF |
| SA47 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2F0000-2FFFFF |
| SA48 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 300000-30FFFF |
| SA49 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 310000-31FFFF |
| SA50 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 320000-32FFFF |
| SA51 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 330000-33FFFF |
| SA52 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 340000-34FFFF |
| SA53 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 350000-35FFFF |
| SA54 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 360000-36FFFF |
| SA55 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 370000-37FFFF |
| SA56 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 380000-38FFFF |
| SA57 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 390000-39FFFF |
| SA58 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A0000-3AFFFF |
| SA59 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3B0000-3BFFFF |
| SA60 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C0000-3CFFFF |
| SA61 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3D0000-3DFFFF |
| SA62 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E0000-3EFFFF |
| SA63 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3F0000-3FFFFF |
| SA64 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 400000-40FFFF |
| SA65 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 410000-41FFFF |
| SA66 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 420000-42FFFF |
| SA67 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 430000-43FFFF |
| SA68 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 440000-44FFFF |
| SA69 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 450000-45FFFF |
| SA70 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 460000-46FFFF |
| SA71 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 470000-47FFFF |
| SA72 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 480000-48FFFF |
| SA73 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 490000-49FFFF |
| SA74 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 4A0000-4AFFFF |
| SA75 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 4B0000-4BFFFF |
| SA76 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4C0000-4CFFFF |
| SA77 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 4D0000-4DFFFF |

| Sector | A22 | A21 | A20 | A19 | A18 | A17 | A16 | 8-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|
| SA78 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4E0000-4EFFFF |
| SA79 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F0000-4FFFFF |
| SA80 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 500000-50FFFF |
| SA81 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 510000-51FFFF |
| SA82 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 520000-52FFFF |
| SA83 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 530000-53FFFF |
| SA84 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 540000-54FFFF |
| SA85 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 550000-55FFFF |
| SA86 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 560000-56FFFF |
| SA87 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 570000-57FFFF |
| SA88 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 580000-58FFFF |
| SA89 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 590000-59FFFF |
| SA90 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A0000-5AFFFF |
| SA91 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B0000-5BFFFF |
| SA92 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C0000-5CFFFF |
| SA93 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D0000-5DFFFF |
| SA94 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E0000-5EFFFF |
| SA95 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F0000-5FFFFF |
| SA96 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 600000-60FFFF |
| SA97 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 610000-60FFFF |
| SA98 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 620000-62FFFF |
| SA99 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 630000-63FFFF |
| SA100 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 640000-64FFFF |
| SA101 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 650000-65FFFF |
| SA102 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 660000-66FFFF |
| SA103 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 670000-67FFFF |
| SA104 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 680000-68FFFF |
| SA105 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 690000-69FFFF |
| SA106 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 6A0000-6AFFFF |
| SA107 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 6B0000-6BFFFF |
| SA108 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6C0000-6CFFFF |
| SA109 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 6D8000-6DFFFF |
| SA110 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 6E0000-6EFFFF |
| SA111 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 6F8000-6FFFFF |
| SA112 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 700000-70FFFF |
| SA113 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 710000-71FFFF |
| SA114 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 720000-72FFFF |
| SA115 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 730000-73FFFF |
| SA116 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 740000-74FFFF |
| SA117 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 750000-75FFFF |

| Sectpr | A21 | A20 | A19 | A18 | A17 | A16 | A15 | 8-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|
| SA118 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 760000-76FFFF |
| SA119 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 770000-77FFFF |
| SA120 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 780000-78FFFF |
| SA121 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 790000-79FFFF |
| SA122 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A0000-7AFFFF |
| SA123 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B0000-7BFFFF |
| SA124 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C0000-7CFFFF |
| SA125 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7D0000-7DFFFF |
| SA126 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E0000-7EFFFF |
| SA127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F0000-7FFFFF |

Note: All sector groups are 64K bytes in size.

## Sector Group Protection/Unprotected Address Table

| Sector Group | A21-A17 |
|---|---|
| SA0-SA3 | 00000 |
| SA4-SA7 | 00001 |
| SA8-SA11 | 00010 |
| SA12-SA15 | 00011 |
| SA16-SA19 | 00100 |
| SA20-SA23 | 00101 |
| SA24-SA27 | 00110 |
| SA28-SA31 | 00111 |
| SA32-SA35 | 01000 |
| SA36-SA39 | 01001 |
| SA40-SA43 | 01010 |
| SA44-SA47 | 01011 |
| SA48-SA51 | 01100 |
| SA52-SA55 | 01101 |
| SA56-SA59 | 01110 |
| SA60-SA63 | 01111 |
| SA64-SA67 | 10000 |
| SA68-SA71 | 10001 |
| SA72-SA75 | 10010 |
| SA76-SA79 | 10011 |
| SA80-SA83 | 10100 |
| SA84-SA87 | 10101 |
| SA88-SA91 | 10110 |
| SA92-SA95 | 10111 |
| SA96-SA99 | 11000 |
| SA100-SA103 | 11001 |
| SA104-SA107 | 11010 |
| SA108-SA111 | 11011 |
| SA112-SA115 | 11100 |
| SA116-SA119 | 11101 |
| SA120-SA123 | 11110 |
| SA124-SA127 | 11111 |

Note: All sector groups are 256K bytes in size.

## Table 1. BUS OPERATION (1)

| Operation | CE# | OE# | WE# | RESET# | ACC | Address (Note 1) | Q15~Q0 |
|---|---|---|---|---|---|---|---|
| Read | L | L | H | H | X | $A_{IN}$ | $D_{OUT}$ |
| Write (Program/Erase) | L | H | L | H | X | $A_{IN}$ | (Note 2) |
| Accelerated Program | L | H | L | H | $V_{HH}$ | $A_{IN}$ | (Note 2) |
| Standby | VCC±0.3V | X | X | VCC±0.3V | H | X | High-Z |
| Output Disable | L | H | H | H | X | X | High-Z |
| Reset | X | X | X | L | X | X | High-Z |
| Sector Group Protect (Note 1) | L | H | L | $V_{ID}$ | X | Sector Addresses, A6=L, A1=H, A0=L | (Note 2) |
| Sector Group Unprotected (Note 1) | L | H | L | $V_{ID}$ | X | Sector Addresses, A6=H, A1=H, A0=L | (Note 2) |
| Temporary Sector Group Unprotected | X | X | X | $V_{ID}$ | X | $A_{IN}$ | (Note 2) |

Legend:

L=Logic LOW=$V_{IL}$,H=Logic High=$V_{IH}$,$V_{ID}$=12.0±0.5V, X=Don't Care, $A_{IN}$=Address IN, $D_{IN}$=Data IN, $D_{OUT}$=Data OUT

Notes:

1. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotect" section.
2. $D_{IN}$ or $D_{OUT}$ as required by command sequence, Data# Polling or sector protect algorithm (see Figure 14).

**Table 2. AUTO-SELECT CODES (High Voltage Method)**

| Operation | CE# | OE# | WE# | A0 | A1 | A5 to A2 | A6 | A8 to A7 | A9 | A15 to A10 | A16 to A22 | Q0~Q7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Silicon ID Manufactures Code | L | L | H | L | L | X | L | X | $V_{ID}$ | X | X | C2H |
| Read Silicon ID Device Code | L | L | H | H | L | X | L | X | $V_{ID}$ | X | X | 93H |
| Sector Protect Verify | L | L | H | L | H | X | X | X | $V_{ID}$ | X | SA | Code(1) |
| Secured Silicon Sector Indicator Bit(Q7) | L | L | H | H | H | X | L | X | $V_{ID}$ | X | X | 90h (factory locked) |
| | | | | | | | | | | | | 10h (non-factory locked) |

Note :
1. code=00h means unprotected, or code=01h means protected, SA=Sector Address, X=Don't care.

## REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

## WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE# and CE# to VIL, and OE# to VIH.

An erase operation can erase one sector, multiple sectors , or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data". Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Auto-select Mode and Auto-select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

## ACCELERATED PROGRAM OPERATION

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned accelerated program mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. Removing VHH from the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

## STANDBY MODE

MX29LV065B can be set into Standby mode with two different approaches. One is using both CE# and RESET# pins and the other one is using RESET# pin only.

When using both pins of CE# and RESET#, a CMOS Standby mode is achieved with both pins held at Vcc ± 0.3V. Under this condition, the current consumed is less than 0.2uA (typ.). If both of the CE# and RESET# are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, Vcc active current (Icc2) is required even CE# = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes.

When using only RESET#, a CMOS standby mode is achieved with RESET# input held at Vss ± 0.3V, Under this condition the current is consumed less than 1uA (typ.). Once the RESET# pin is taken high, the device is back to active without recovery delay.

In the standby mode the outputs are in the high impedance state, independent of the OE# input.

MX29LV065B is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29LV065B automatically switch themselves to low power mode when MX29LV065B addresses remain stable during access time of tACC+30ns.

It is not necessary to control CE#, WE#, and OE# on the mode. Under the mode, the current consumed is typically 0.2uA (CMOS level).

## AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when address remain stable for tACC+30ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC4 in the DC Characteristics table represents the automatic sleep mode current specification.

## OUTPUT DISABLE

With the OE# input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

## RESET# OPERATION

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the RESET# pulse. When RESET# is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If RESET# is held at VIL but not within VSS±0.3V, the standby current will be greater.

The RESET# pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY. The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is completed within a time of tREADY . The system can read data tRH after the RESET# pin returns to VIH.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 3 for the timing diagram.

## SECTOR GROUP PROTECT OPERATION

The MX29LV065B features hardware sector group protection. This feature will disable both program and erase operations for these sector group protected. In this device, a sector group consists of four adjacent sectors which are protected or unprotected at the same time. To activate this mode, the programming equipment must force VID on address pin A9 and control pin OE#, (suggest VID = 12V) A6 = VIL and CE# = VIL. (see Table 2) Programming of the protection circuitry begins on the falling edge of the WE# pulse and is terminated on the rising edge. Please refer to sector group protect algorithm and waveform.

MX29LV065B also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 ( with CE# and OE# at VIL and WE# at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

## CHIP UNPROTECTED OPERATION

The MX29LV065B also features the chip unprotected mode, so that all sectors are unprotected after chip

unprotected is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotected mode.

To activate this mode, the programming equipment must force VID on control pin OE# and address pin A9. The CE# pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotected algorithm and waveform for the chip unprotected algorithm. The unprotected mechanism begins on the falling edge of the WE# pulse and is terminated on the rising edge.

MX29LV065B also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotected algorithm is completed.

## TEMPORARY SECTOR GROUP UNPROTECTED OPERATION

This feature allows temporary unprotected of previously protected sector to change data in-system. The Temporary Sector Unprotected mode is activated by setting the RESET# pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as unprotected sector. Once VID is remove from the RESET# pin, all the previously protected sectors are protected again.

## SILICON ID READ OPERATION

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX29LV065B provides hardware method to access the silicon ID read operation. Which method requires VID on A9 pin, VIL on CE#, OE#, A6, and A1 pins. Which apply VIL on A0 pin, the device will output MXIC's manufacture code of C2H. Which apply VIH on A0 pin, the device will output MX29LV065B device code of 93H.

## VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV065B provides hardware method for sector group protect status verify. Which method requires VID on A9 pin, VIH on WE# and A1 pins, VIL on CE#, OE#, A6, and A0 pins, and sector address on A16 to A21 pins. Which the identified sector is protected, the device will output 01H. Which the identified sector is not protect, the device will output 00H.

## DATA PROTECTION

The MX29LV065B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

## SECURED SILICON SECTOR

The MX29LV065B features a Flash memory region where the system may access through a command sequence to create a permanent part identification as so called Electronic Serial Number (ESN) in the device. Once this region is programmed, any further modification on the region is impossible. The secured silicon sector is a 128 bytes in length, and uses a Secured Silicon Sector Indicator Bit (Q7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevent duplication of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The MX29LV065B offers the device with Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory , and has the Secured Silicon Sector Indicator Bit permanently set to a "1". The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customs to utilize that sector in any form they prefer. The customer-lockable version has the secured sector Indicator Bit permanently set to a "0". Therefore, the Secured Silicon Sector Indicator Bit permanently set to a "0". Therefore, the Second Silicon Sector Indicator Bit prevents customer, lockable device from being used to replace devices that are factory locked.

The system access the Secured Silicon Sector through a command sequence (refer to "Enter Secured Silicon/ Exit Secured Silicon Sector command Sequence). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the address normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending command to sector SA0.

## LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

## WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on CE# or WE# will not initiate a write cycle.

## LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

## POWER-UP SEQUENCE

The MX29LV065B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

## POWER-UP WRITE INHIBIT

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

## POWER SUPPLY DE COUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

## FACTORY LOCKED:Secured Silicon Sector Programmed and Protected At the Factory

In device with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. A factory locked device has an 16-byte random ESN at address 000000h-00000Fh.

## CUSTOMER LOCKABLE:Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the Secured Silicon Sector at address 000010h-00008Fh. Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotected the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 14, except that RESET# may be at either VIH or VID. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that method is only applicable to the Secured Silicon Sector.

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then alternate method of sector protection described in the :Sector Group Protection and Unprotected" section.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

## SOFTWARE COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data are latched on rising edge of WE# or CE#, whichever happens first.

**TABLE 3. MX29LV065B COMMAND DEFINITIONS**

| Command | Bus Cycle | First Bus Cycle | | Second Bus Cycle | | Third Bus Cycle | | Fourth Bus Cycle | | Fifth Bus Cycle | | Sixth Bus Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read(Note 5) | 1 | RA | RD | | | | | | | | | | |
| Reset(Note 6) | 1 | XXX | F0 | | | | | | | | | | |
| Auto-select(Note 7) | | | | | | | | | | | | | |
| Manufacturer ID | 4 | XXX | AA | XXX | 55 | XXX | 90 | X00 | C2 | | | | |
| Device ID | 4 | XXX | AA | XXX | 55 | XXX | 90 | X01 | 93 | | | | |
| Secured Sector Factory Protect (Note 8) | 4 | XXX | AA | XXX | 55 | XXX | 90 | X03 | 90/10 | | | | |
| Sector Group Protect | 4 | XXX | AA | XXX | 55 | XXX | 90 | SA | xx00 | | | | |
| Verify (Note 9) | 4 | XXX | AA | XXX | 55 | XXX | 90 | X02 | xx01 | | | | |
| Enter Secured Silicon Sector | 3 | XXX | AA | XXX | 55 | XXX | 88 | | | | | | |
| Exit Secured Silicon Sector | 4 | XXX | AA | XXX | 55 | XXX | 90 | xxx | 00 | | | | |
| Program | 4 | XXX | AA | XXX | 55 | XXX | A0 | PA | PD | | | | |
| Chip Erase | 6 | XXX | AA | XXX | 55 | XXX | 80 | XXX | AA | XXX | 55 | XXX | 10 |
| Sector Erase | 6 | XXX | AA | XXX | 55 | XXX | 80 | XXX | AA | XXX | 55 | SA | 30 |
| Erase Suspend(Note 10) | 1 | BA | B0 | | | | | | | | | | |
| Erase Resume(Note 11) | 1 | BA | 30 | | | | | | | | | | |
| CFI Query (Note 12) | 1 | XX | 98 | | | | | | | | | | |

Legend:
X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse.
PD=Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.
SA=Address of the sector to be erased or verified. Address bits A22-A16 uniquely select any sector.

Notes:
1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except for the read cycle and fourth cycle of the auto-select command sequence, all bus cycles are write cycles.
4. Unless otherwise noted, address bits A22-A12 are don't cares.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the auto-select mode or if Q5 goes high (while the device is providing status information).
7. The fourth cycle of the auto-select command sequence is a read cycle. See the Auto-select Command Sequence section for more information.
8. The data is 80h for factory locked and 00h for not factory locked.
9. The data is 00h for an unprotected sector group and 01h for a protected sector group.
10. The system may read and program functions in non-erasing sectors, or enter the auto-select mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
11. The Erase Resume command is valid only during the Erase Suspend mode.
12. Command is valid when device is ready to read array data or when device is in auto-select mode.

## READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See rase Suspend/Erase Resume Commands" for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the auto-select mode. See the "Reset Command" section, next.

## RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

## SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 3 shows the address and data requirements.

This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires $V_{ID}$ on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the auto-select mode and return to reading array data.

## BYTE PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 3 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using
Q7, Q6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

## SETUP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H, or the sector erase command 30H.

The MX29LV065B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 93H for MX29LV065B.

## AUTOMATIC CHIP/SECTOR ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically preprogram and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 2 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6, Q2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 16 for timing diagrams.

## SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later , while the command(data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 50us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

## ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is issued during the sector erase operation, the device requires a maximum 20us to suspend the sector erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Erase Resume, program data to, or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

## ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

## QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV065B is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 3.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

**Table 4-1. CFI mode: Identification Data Values**
(All values in these tables are in hexadecimal)

| Description | Address h | Data h |
|---|---|---|
| Query-unique ASCII string "QRY" | 10 | 0051 |
| | 11 | 0052 |
| | 12 | 0059 |
| Primary vendor command set and control interface ID code | 13 | 0002 |
| | 14 | 0000 |
| Address for primary algorithm extended query table | 15 | 0040 |
| | 16 | 0000 |
| Alternate vendor command set and control interface ID code (none) | 17 | 0000 |
| | 18 | 0000 |
| Address for secondary algorithm extended query table (none) | 19 | 0000 |
| | 1A | 0000 |

**Table 4-2. CFI Mode: System Interface Data Values**

| Description | Address h | Data h |
|---|---|---|
| VCC supply, minimum (2.7V) | 1B | 27 |
| VCC supply, maximum (3.6V) | 1C | 36 |
| VPP supply, minimum (none) | 1D | 00 |
| VPP supply, maximum (none) | 1E | 00 |
| Typical timeout for single byte write ($2^N$ us) | 1F | 04 |
| Typical timeout for maximum size buffer write ($2^N$ us) | 20 | 00 |
| Typical timeout for individual block erase ($2^N$ ms) | 21 | 0A |
| Typical timeout for full chip erase ($2^N$ ms) | 22 | 00 |
| Maximum timeout for single byte write times ($2^N$ X Typ) | 23 | 05 |
| Maximum timeout for maximum size buffer write times ($2^N$ X Typ) | 24 | 00 |
| Maximum timeout for individual block erase times ($2^N$ X Typ) | 25 | 04 |
| Maximum timeout for full chip erase times (not supported) | 26 | 00 |

**Table 4-3. CFI Mode: Device Geometry Data Values**

| Description | Address h | Data h |
|---|---|---|
| Device size ($2^n$ bytes) | 27 | 17 |
| Flash device interface code (02=asynchronous x8/x16) | 28 | 00 |
| | 29 | 00 |
| Maximum number of bytes in multi-byte write (not supported) | 2A | 00 |
| | 2B | 00 |
| Number of erase block regions | 2C | 01 |
| Erase block region 1 information | 2D | 7F |
| [2E,2D] = # of blocks in region -1 | 2E | 00 |
| [30, 2F] = size in multiples of 256-bytes | 2F | 00 |
| | 30 | 01 |
| | 31 | 00 |
| Erase Block Region 2 Information (refer to CFI publication 100) | 32 | 00 |
| | 33 | 00 |
| | 34 | 00 |
| | 35 | 00 |
| Erase Block Region 3 Information (refer to CFI publication 100) | 36 | 00 |
| | 37 | 00 |
| | 38 | 00 |
| | 39 | 00 |
| Erase Block Region 4 Information (refer to CFI publication 100) | 3A | 00 |
| | 3B | 00 |
| | 3C | 00 |

**Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values**

| Description | Address h | Data h |
|---|---|---|
| Query-unique ASCII string "PRI" | 40 | 50 |
| | 41 | 52 |
| | 42 | 49 |
| Major version number, ASCII | 43 | 31 |
| Minor version number, ASCII | 44 | 31 |
| Address sensitive unlock (0=required, 1= not required) | 45 | 01 |
| Erase suspend (2= to read and write) | 46 | 02 |
| Sector protect (N= # of sectors/group) | 47 | 04 |
| Temporary sector unprotect (1=supported) | 48 | 01 |
| Sector protect/unprotect scheme (04=29LV800 mode) | 49 | 04 |
| Simultaneous R/W operation (0=not supported) | 4A | 00 |
| Burst mode type (0=not supported) | 4B | 00 |
| Page mode type (0=not supported) | 4C | 00 |
| ACC (Acceleration) Supply Minimum<br>00h=Not Supported, D7-D4: Volt, D3-D0:100mV | 4D | B5 |
| ACC (Acceleration) Supply Maximum<br>00h=Not Supported, D7-D4: Volt, D3-D0:100mV | 4E | C5 |
| Top/Bottom Boot Sector Flag<br>02h=Bottom Boot Device, 03h=Top BootnDevice | 4F | 00 |

## WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY#. Table 5 and the following subsections describe the functions of these bits. Q7, RY/BY#, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

### Table 5. Write Operation Status

| | Status | | Q7 Note1 | Q6 | Q5 Note2 | Q3 | Q2 | RY/BY# |
|---|---|---|---|---|---|---|---|---|
| In Progress | Byte Program in Auto Program Algorithm | | Q7# | Toggle | 0 | N/A | No Toggle | 0 |
| | Auto Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle | 0 |
| | Erase Suspended Mode | Erase Suspend Read (Erase Suspended Sector) | 1 | No Toggle | 0 | N/A | Toggle | 1 |
| | | Erase Suspend Read (Non-Erase Suspended Sector) | Data | Data | Data | Data | Data | 1 |
| | | Erase Suspend Program | Q7# | Toggle | 0 | N/A | N/A | 0 |
| Exceeded Time Limits | Byte Program in Auto Program Algorithm | | Q7# | Toggle | 1 | N/A | No Toggle | 0 |
| | Auto Erase Algorithm | | 0 | Toggle | 1 | 1 | Toggle | 0 |
| | Erase Suspend Program | | Q7# | Toggle | 1 | N/A | N/A | 0 |

Notes:
1. Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2. Performing successive read operations from any address will cause Q6 to toggle.
3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit.
   However, successive reads from the erase-suspended sector will cause Q2 to toggle.

### Q7: Data# Polling

The Data# Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data# Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data# Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE#) is asserted low.

### Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles for 100us and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

### Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read

cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 5 to compare outputs for Q2 and Q6.

### Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

### Q5:Program/Erase Timing

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1". Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, Q5 produces a "1".

### Q3:Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is

still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

If the time between additional erase commands from the system can be less than 50us, the system need not to monitor Q3.

## RY/BY# : READY/BUSY# OUTPUT

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to VCC .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . . ..... -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . .... -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, OE#, ACC and

RESET# (Note 2) . . . . . ....-0.5 V to +12.5 V

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9, OE# and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

## OPERATING RATINGS

**Commercial (C) Devices**

Ambient Temperature ($T_A$). . . . . 0° C to +70° C

**Industrial (I) Devices**

Ambient Temperature ($T_A$). . . . . -40° C to +85° C

**VCC Supply Voltages**

VCC for full voltage range. . . . . +2.7 V to 3.6 V

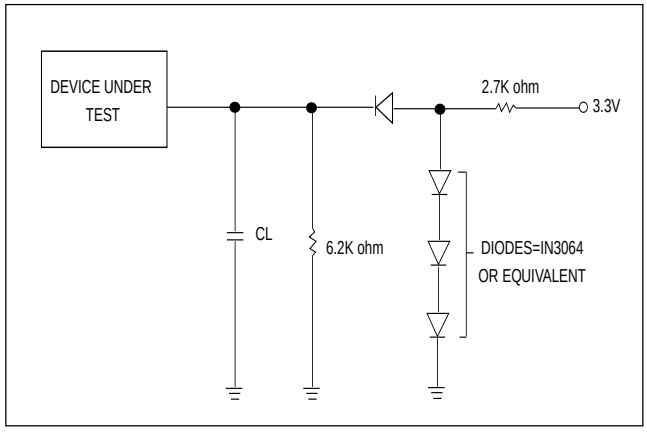
Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS TA=-40° C to 85° C, VCC=2.7V~3.6V

| Para-meter | Description | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| I LI | Input Load Current (Note 1) | VIN = VSS to VCC , VCC = VCC max | | | | ±1.0 | uA |
| I LIT | A9 Input Load Current | VCC=VCC max; A9 = 12.5V | | | | 35 | uA |
| I LO | Output Leakage Current | VOUT = VSS to VCC , VCC= VCC max | | | | ±1.0 | uA |
| ICC1 | VCC Active Read Current | CE# = VIL, | 5 MHz | | 9 | 16 | mA |
| | (Notes 2,3) | OE# = VIH | 1 MHz | | 2 | 4 | mA |
| ICC2 | VCC Active Write Current (Notes 2,4) | CE#= VIL , OE# = VIH | | | 26 | 30 | mA |
| ICC3 | VCC Standby Current (Note 2) | CE#, RESET#=VCC ±0.3V | | | 0.2 | 15 | uA |
| ICC4 | VCC Reset Current (Note 2) | RESET#=VSS ±0.3V | | | 0.2 | 15 | uA |
| ICC5 | Automatic Sleep Mode (Note 2) | VIL = VSS ±0.3 V, VIH = VCC ±0.3 V | | | 0.2 | 15 | uA |
| IACC | ACC Accelerated Program | CE# = VIL , | ACC pin | | 5 | 10 | mA |
| | Current | OE# = VIH | VCC pin | | 15 | 30 | mA |
| VIL | Input Low Voltage (Note 5) | | | -0.5 | | 0.8 | V |
| VIH | Input High Voltage (Note 5) | | | 0.7xVCC | | VCC+0.3 | V |
| VHH | Voltage for ACC Program Acceleration | VCC = 3.0 V ±10% | | 11.5 | | 12.5 | V |
| VID | Voltage for Auto-select and Temporary Sector Unprotected | VCC = 3.0 V ±10% | | 8.5 | | 12.5 | V |
| VOL | Output Low Voltage | IOL= 4.0mA,VCC=VCC min | | | | 0.45 | V |
| VOH1 | Output High Voltage | IOH=-2.0mA,VCC=VCC min | | 0.85VCC | | | V |
| VOH2 | | IOH=-100uA,VCC=VCC min | | VCC-0.4 | | | V |
| VLKO | Low VCC Lock-Out Voltage (Note 4) | | | 2.3 | | 2.5 | V |

Notes :
1. The ICC current listed is typically less than 2mA/MHz, with OE# at VIH.
2. Maximum ICC specifications are tested with VCC = VCC max.
3. ICC active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t ACC + 30 ns. Typical sleep mode current is 200 nA.
5. Not 100% tested.

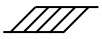
## SWITCHING TEST CIRCUITS



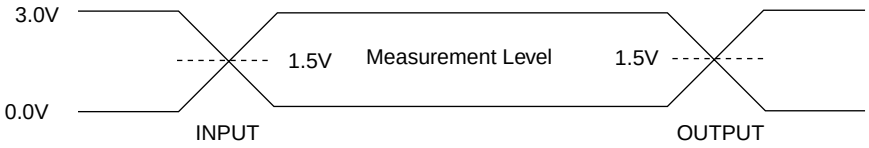

## TEST SPECIFICATIONS

| Test Condition | 90 | 12 | Unit |
|---|---|---|---|
| Output Load | 1 TTL gate | | |
| Output Load Capacitance, CL (including jig capacitance) | 30 | 100 | pF |
| Input Rise and Fall Times | 5 | | ns |
| Input Pulse Levels | 0.0-3.0 | | V |
| Input timing measurement reference levels | 1.5 | | V |
| Output timing measurement reference levels | 1.5 | | V |

## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Steady | |
|  | Changing from H to L | |
|  | Changing from L to H | |
|  | Don't Care, Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High Impedance State(High Z) |

## SWITCHING TEST WAVEFORMS



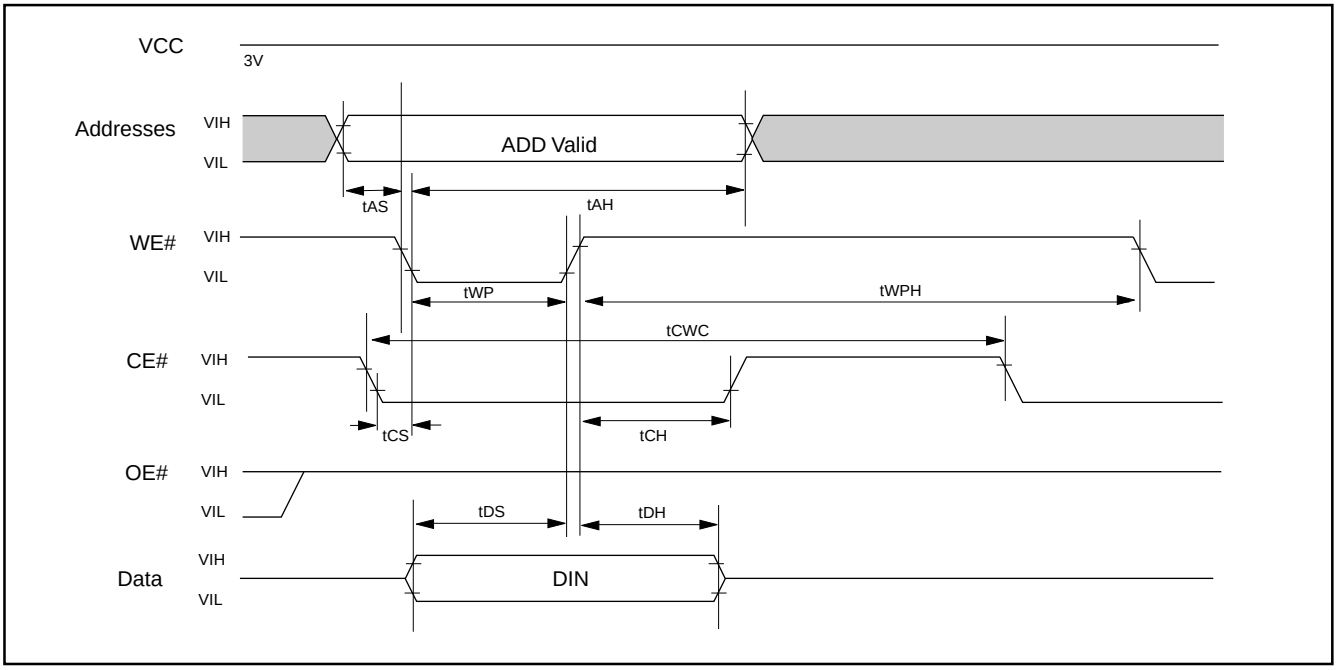
## AC CHARACTERISTICS

### Read-Only Operations TA=-40° C to 85° C, VCC=2.7V~3.6V

| Parameter Std. | Description | | Test Setup | | Speed Options | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | 90 | 12 | |
| tRC | Read Cycle Time (Note 1) | | | Min | 90 | 120 | ns |
| tACC | Address to Output Delay | | CE#, OE#=VIL | Max | 90 | 120 | ns |
| tCE | Chip Enable to Output Delay | | OE#=VIL | Max | 90 | 120 | ns |
| tOE | Output Enable to Output Delay | | | Max | 35 | 50 | ns |
| tDF | Chip Enable to Output High Z (Note 1) | | | Max | 30 | 30 | ns |
| tDF | Output Enable to Output High Z (Note 1) | | | Max | 30 | 30 | ns |
| tOH | Output Hold Time From Address, CE# or OE#, whichever Occurs First | | | Min | 0 | | ns |
| tOEH | Output Enable Hold Time (Note 1) | Read | | Min | 0 | | ns |
| | | Toggle and Data# Polling | | Min | 10 | | ns |

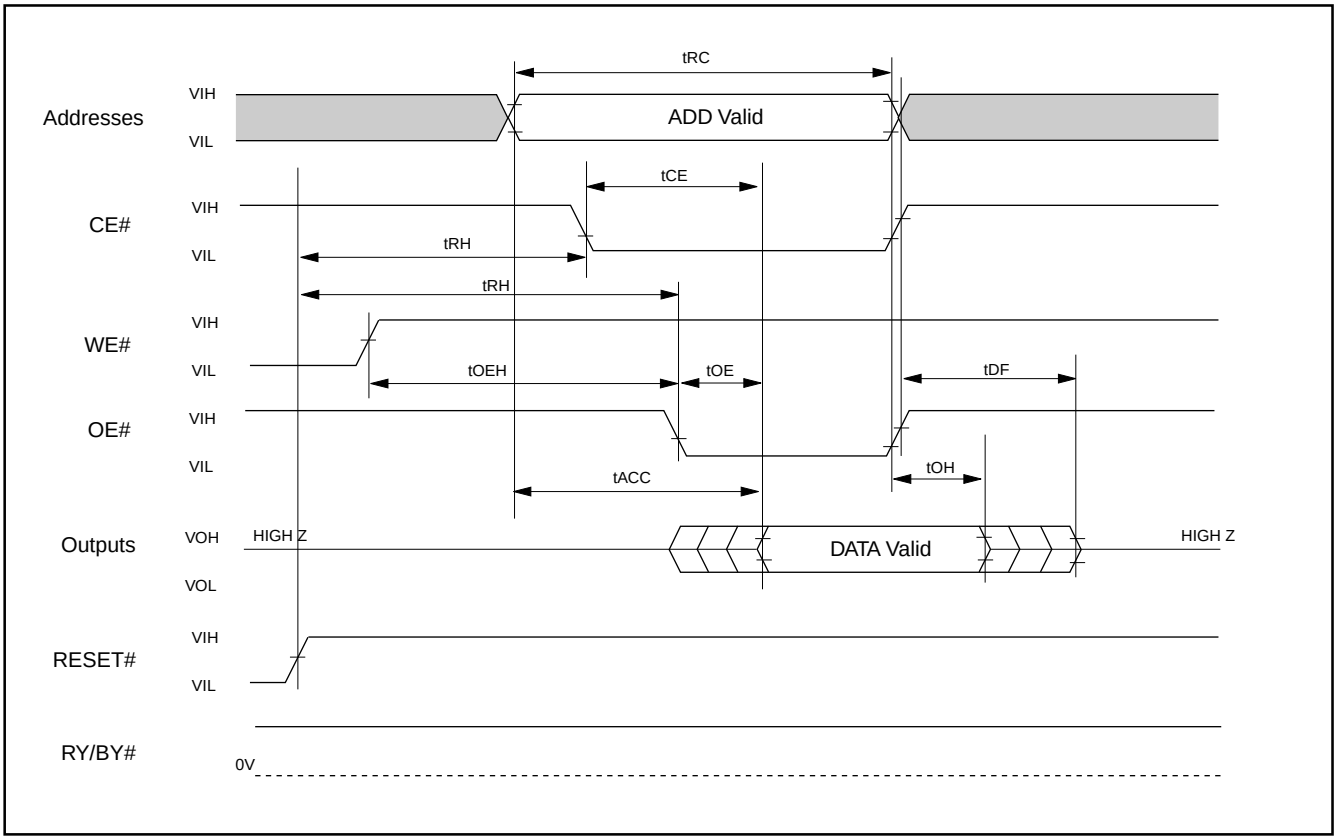
Notes:
1. Not 100% tested.
2. See SWITCHING TEST CIRCUITS and TEST SPECIFICATIONS TABLE for test specifications.

### Figure 1. COMMAND WRITE OPERATION




## READ/RESET# OPERATION

### Figure 2. READ TIMING WAVEFORMS

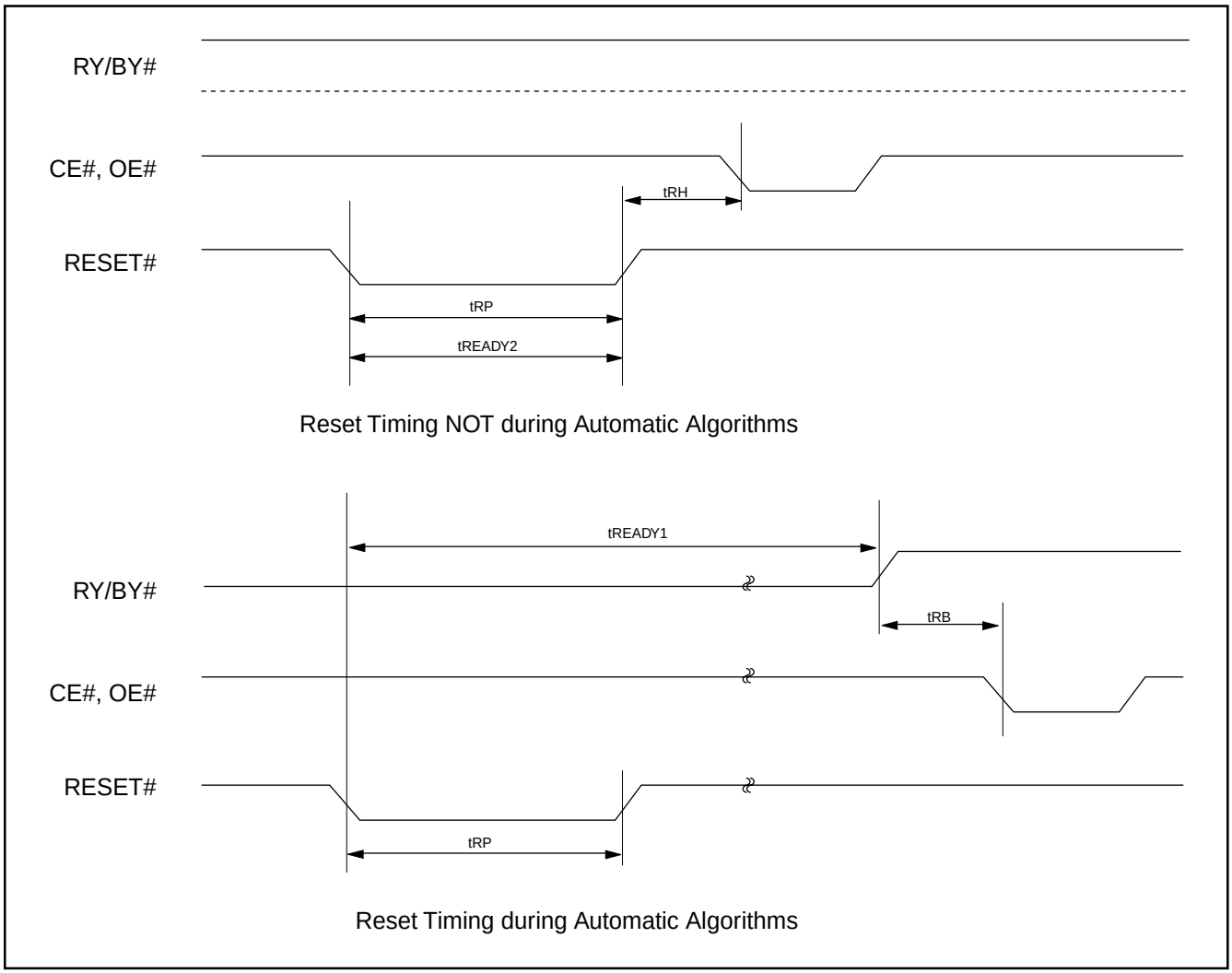


## AC CHARACTERISTICS

| Parameter | Description | Test Setup | All Speed Options | Unit |
|---|---|---|---|---|
| tREADY1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write (See Note) | MAX | 20 | us |
| tREADY2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note) | MAX | 500 | ns |
| tRP | RESET# Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| tRH | RESET# High Time Before Read(See Note) | MIN | 50 | ns |
| tRB | RY/BY# Recovery Time(to CE#, OE# go low) | MIN | 0 | ns |
| tRPD | RESET# Low to Standby Mode | MIN | 20 | us |

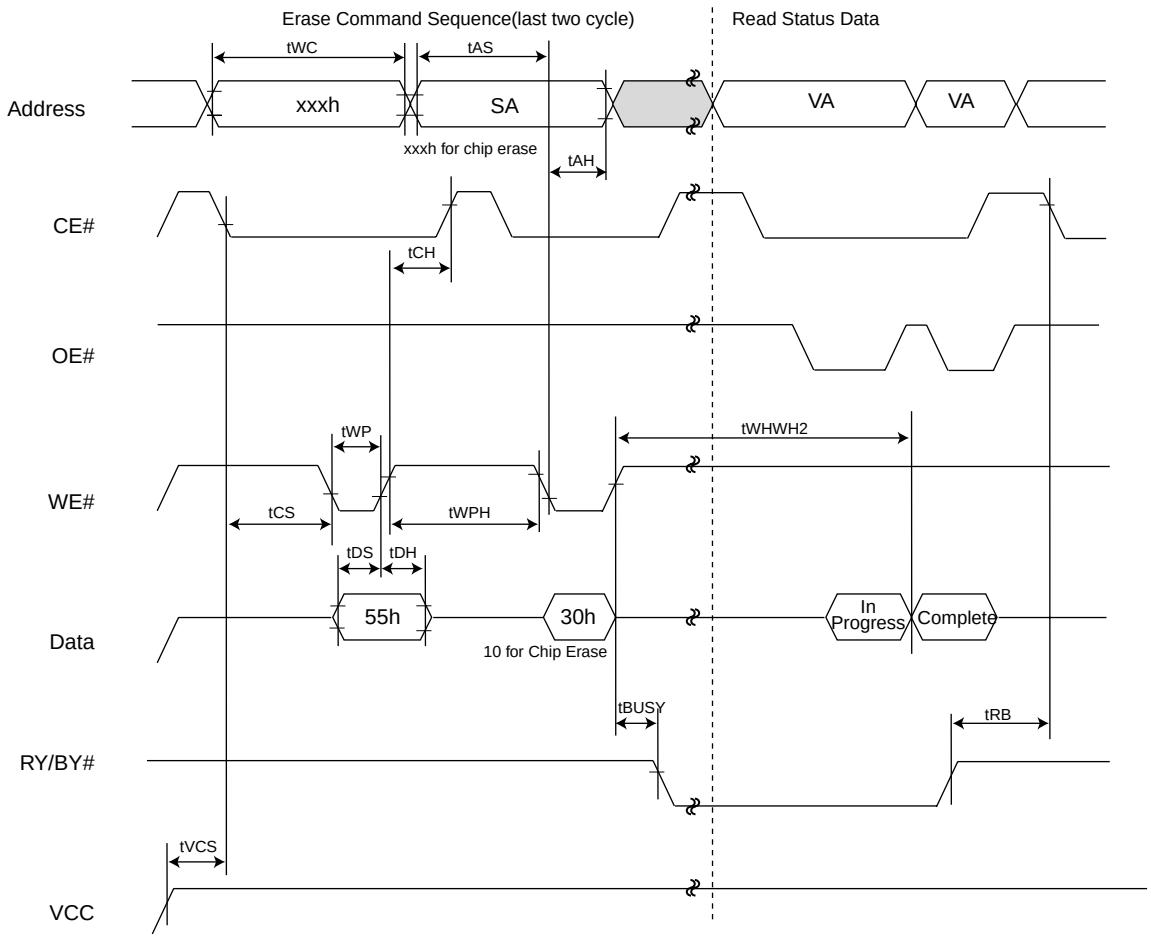
Note : Not 100% tested

**Figure 3. RESET# TIMING WAVEFORM**



## ERASE/PROGRAM OPERATION

### Figure 4. AUTOMATIC CHIP/SECTOR ERASE TIMING WAVEFORM




Note :
1.SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

**Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**

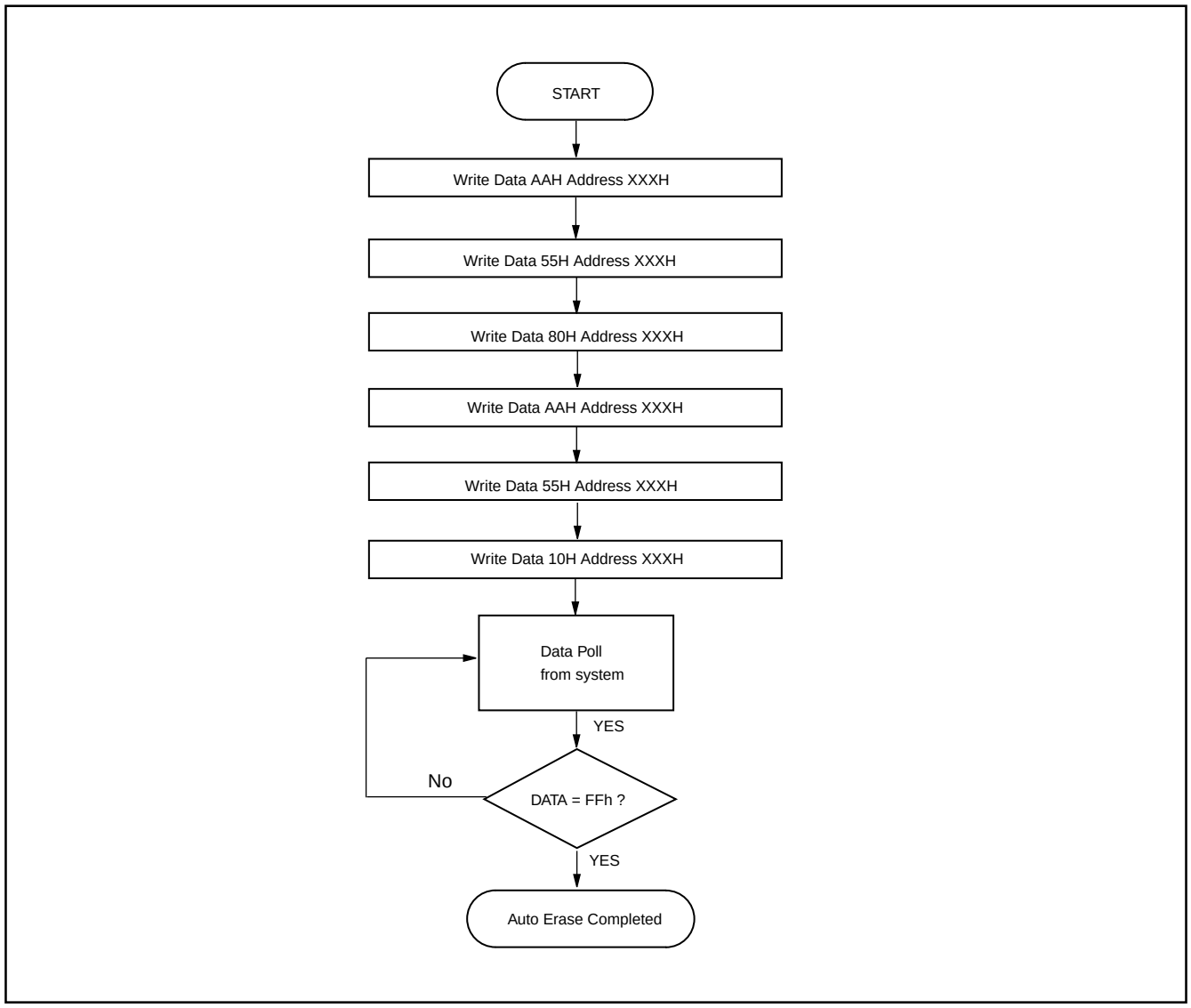


**Figure 6. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**

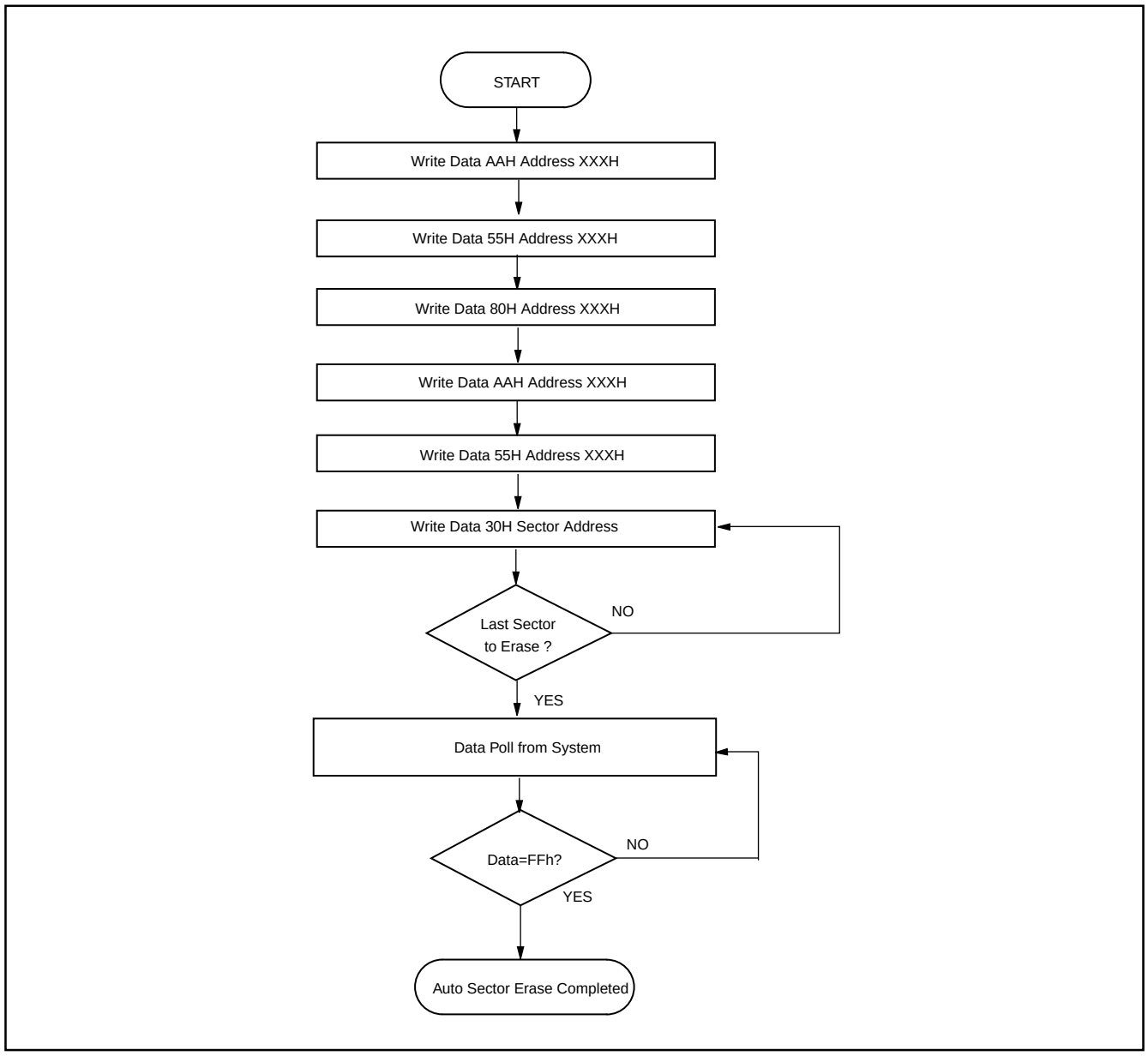


**Figure 7. ERASE SUSPEND/RESUME FLOWCHART**

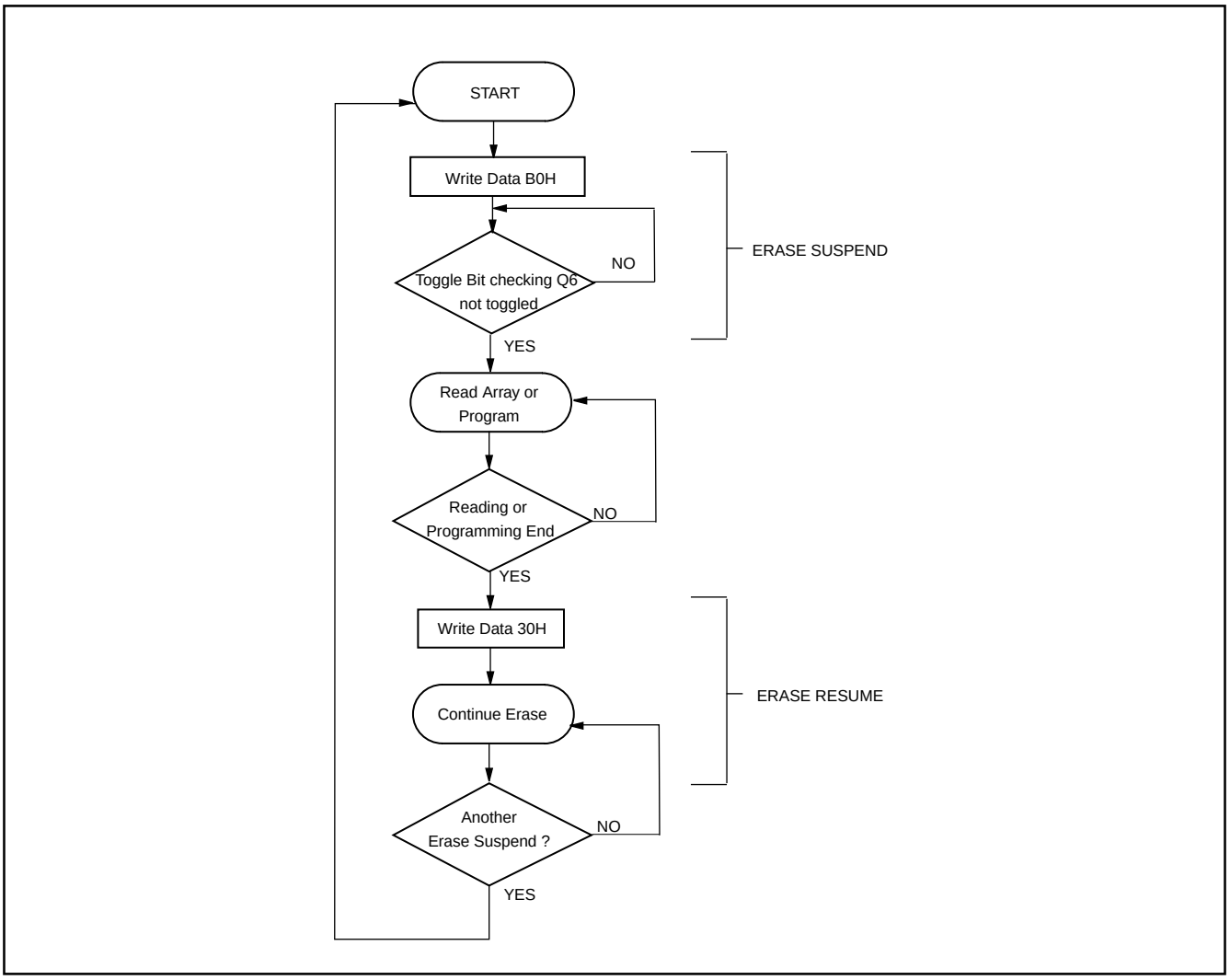
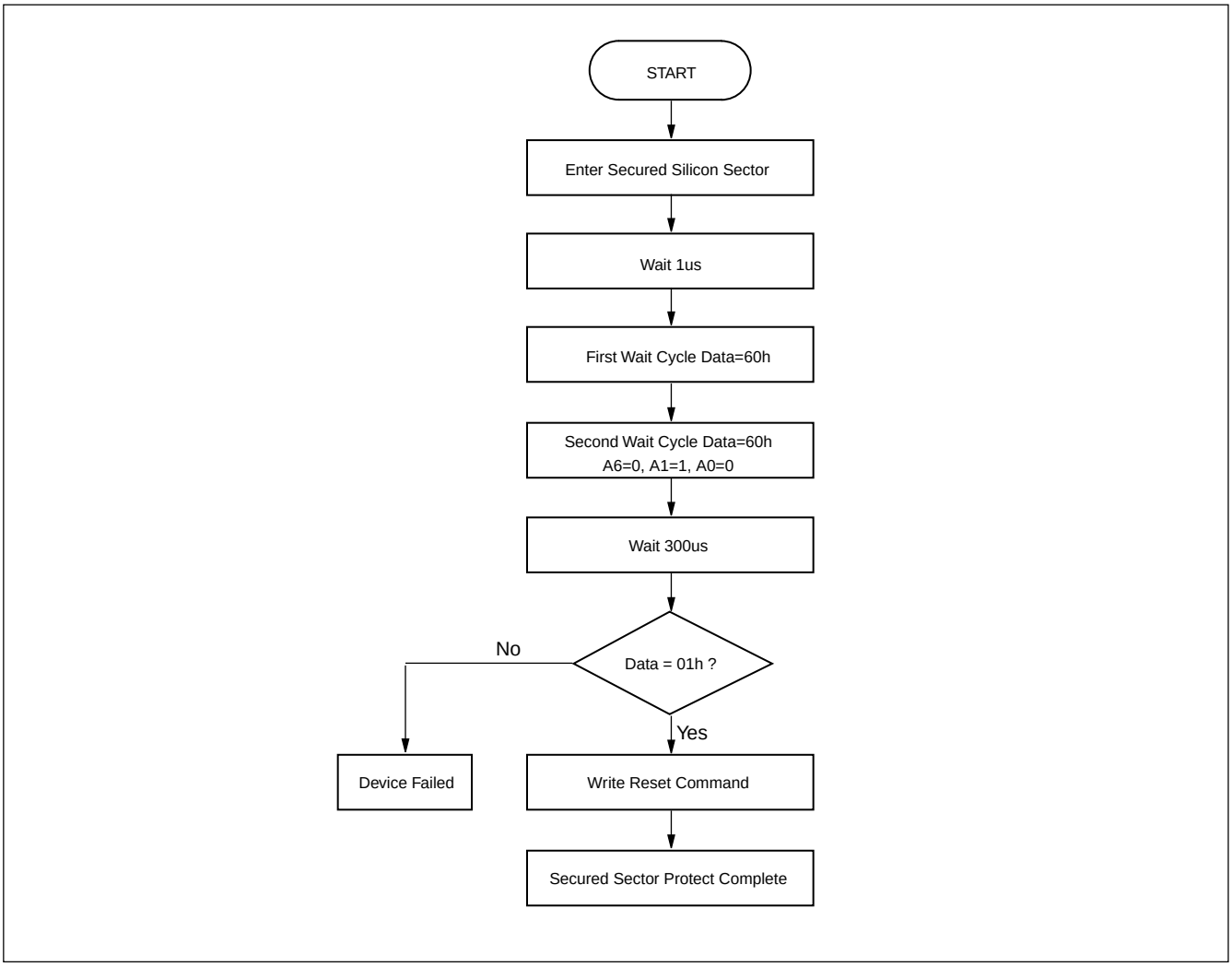


**Figure 8. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART**



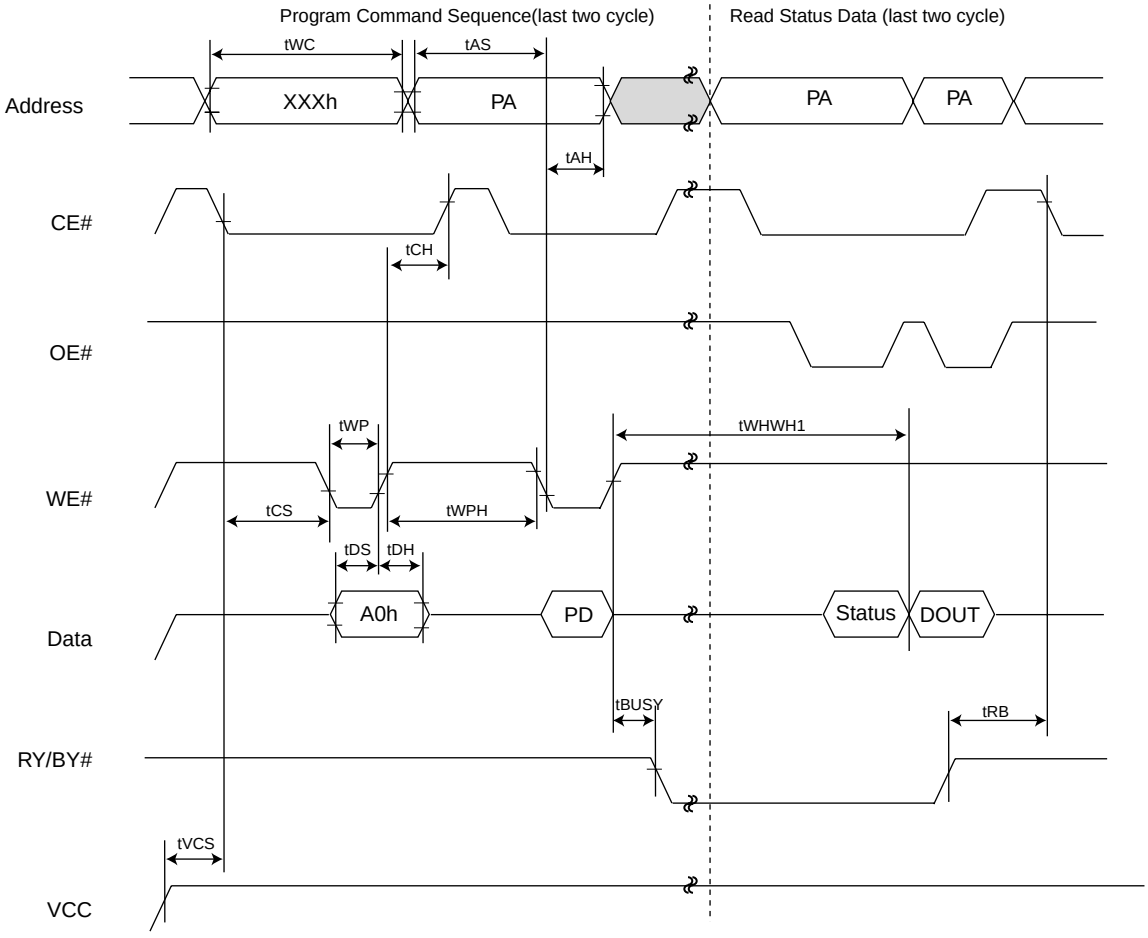
## AC CHARACTERISTICS

### Erase and Program Operations TA=-40° C to 85° C, VCC=2.7V~3.6V

| Parameter Std. | Description | | Speed Options | | Unit |
|---|---|---|---|---|---|
| | | | 90 | 12 | |
| tWC | Write Cycle Time (Note 1) | Min | 90 | 120 | ns |
| tCWC | Command Write Cycle Time (Note 1) | Min | 90 | 120 | ns |
| tAS | Address Setup Time | Min | 0 | | ns |
| tASO | Address Setup Time to OE# low during toggle bit polling | Min | 15 | | ns |
| tAH | Address Hold Time | Min | 45 | 50 | ns |
| tAHT | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0 | | ns |
| tDS | Data Setup Time | Min | 45 | 50 | ns |
| tDH | Data Hold Time | Min | 0 | | ns |
| tOEPH | Output Enable High during toggle bit polling | Min | 20 | | ns |
| tGHWL | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | ns |
| tCS | CE# Setup Time | Min | 0 | | ns |
| tCH | CE# Hold Time | Min | 0 | | ns |
| tWP | Write Pulse Width | Min | 35 | 50 | ns |
| tWPH | Write Pulse Width High | Min | 30 | | ns |
| tWHWH1 | Byte Programming Operation (Note 2) | Typ | 7 | | us |
| tWHWH2 | Sector Erase Operation (Note 2) | Typ | 1.6 | | sec |
| tVHH | VHH Rise and Fall Time (Note 1) | Min | 250 | | ns |
| tVCS | VCC Setup Time (Note 1) | Min | 50 | | us |
| tRB | Write Recovery Time from RY/BY# | Min | 0 | | ns |
| tBUSY | Program/Erase Valid to RY/BY# Delay | Min | 90 | | ns |

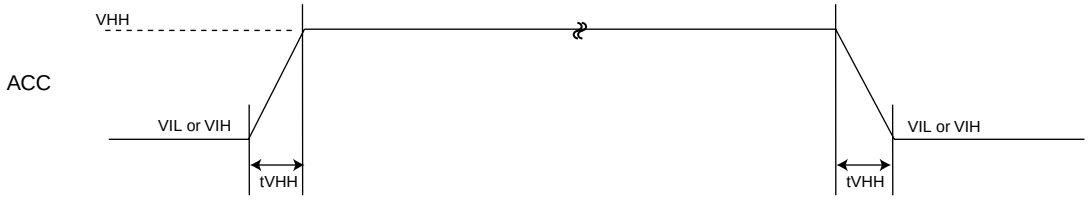
Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.

## Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS




Note :
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

## Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM



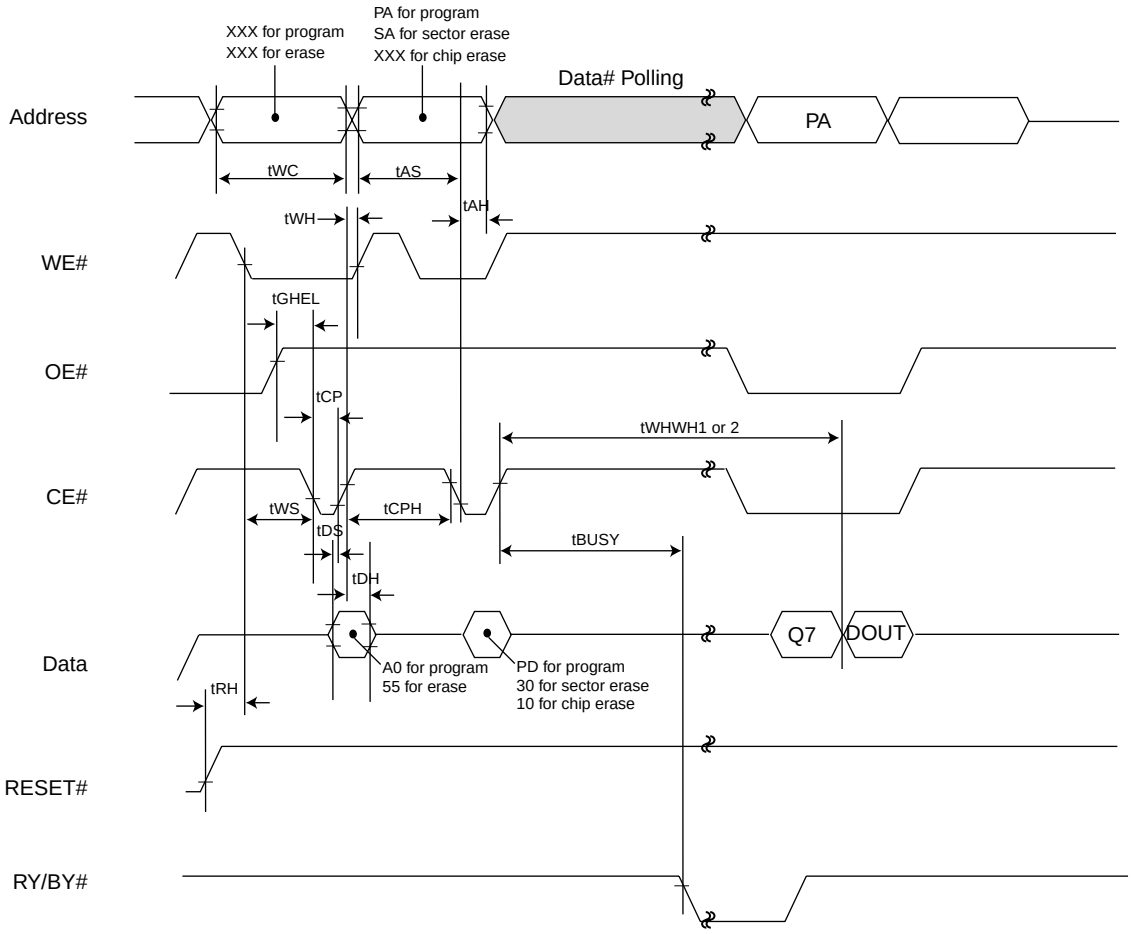
## AC CHARACTERISTICS

### Alternate CE# Controlled Erase and Program Operations

| Parameter Std. | Description | | Speed Options | | Unit |
|---|---|---|---|---|---|
| | | | 90 | 12 | |
| tWC | Write Cycle Time (Note 1) | Min | 90 | 120 | ns |
| tAS | Address Setup Time | Min | 0 | | ns |
| tAH | Address Hold Time | Min | 45 | 50 | ns |
| tDS | Data Setup Time | Min | 45 | 50 | ns |
| tDH | Data Hold Time | Min | 0 | | ns |
| tGHEL | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | ns |
| tWS | WE# Setup Time | Min | 0 | | ns |
| tWH | WE# Hold Time | Min | 0 | | ns |
| tCP | CE# Pulse Width | Min | 45 | 50 | ns |
| tCPH | CE# Pulse Width High | Min | 30 | | ns |
| tWHWH1 | Byte Programming Operation (Note 2) | Typ | 7 | | us |
| tWHWH2 | Sector Erase Operation (Note 2) | Typ | 1.6 | | sec |

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.

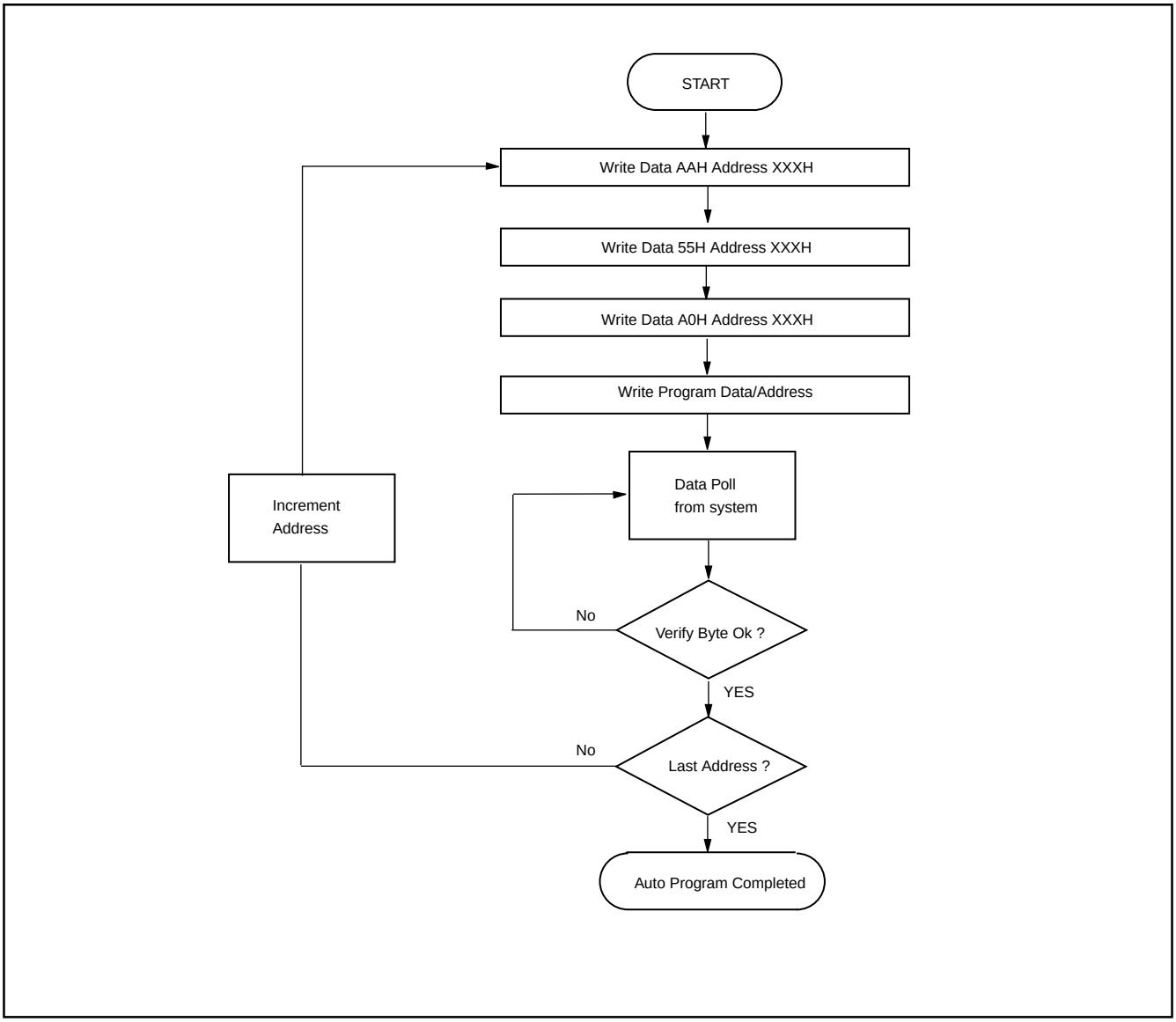
## Figure 11. CE# CONTROLLED PROGRAM TIMING WAVEFORM




Notes :

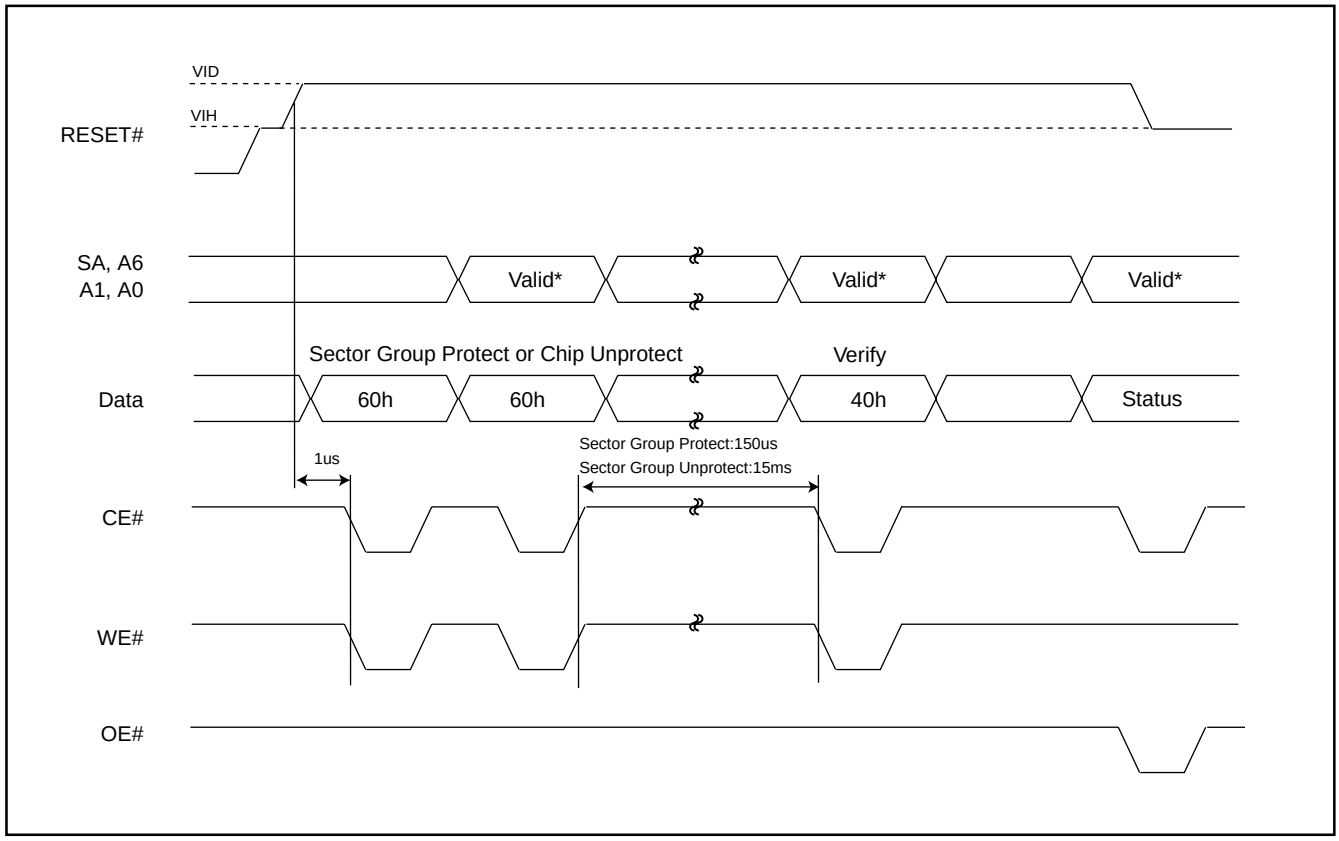
1. PA=Program Address, PD=Program Data, DOUT=Data Out, Q7=complement of data written to device.
2. Figure indicates the last two bus cycles of the command sequence.

**Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**



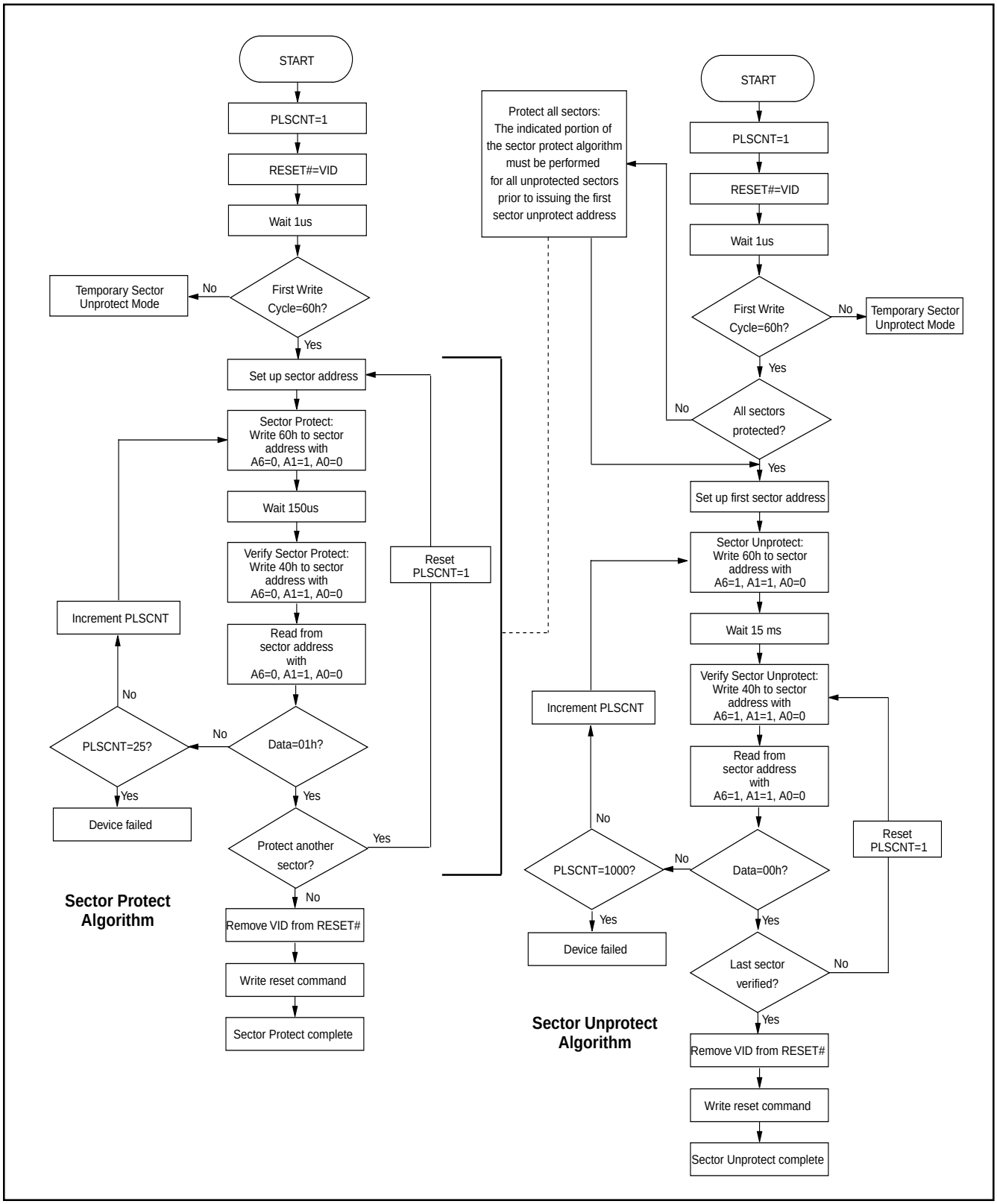
## SECTOR GROUP PROTECT/CHIP UNPROTECTED

**Figure 13. Sector Group Protect / Protect and Unprotected Waveform (RESET# Control)**




Note: For sector group protect A6=0, A1=1, A0=0. For sector group unprotected A6=1, A1=1, A0=0

**Figure 14. IN-SYSTEM SECTOR GROUP PROTECT/CHIP UNPROTECTED ALGORITHMS WITH RESET#=VID**



## AC CHARACTERISTICS

| Parameter | Description | Test Setup | All Speed Options | Unit |
|---|---|---|---|---|
| tVLHT | Voltage transition time | Min. | 4 | us |
| tWPP1 | Write pulse width for sector group protect | Min. | 100 | ns |
| tWPP2 | Write pulse width for chip unprotect | Min. | 100 | ns |
| tOESP | OE# setup time to WE# active | Min. | 4 | us |

**Figure 15. SECTOR GROUP PROTECT TIMING WAVEFORM (A9, OE# Control)**

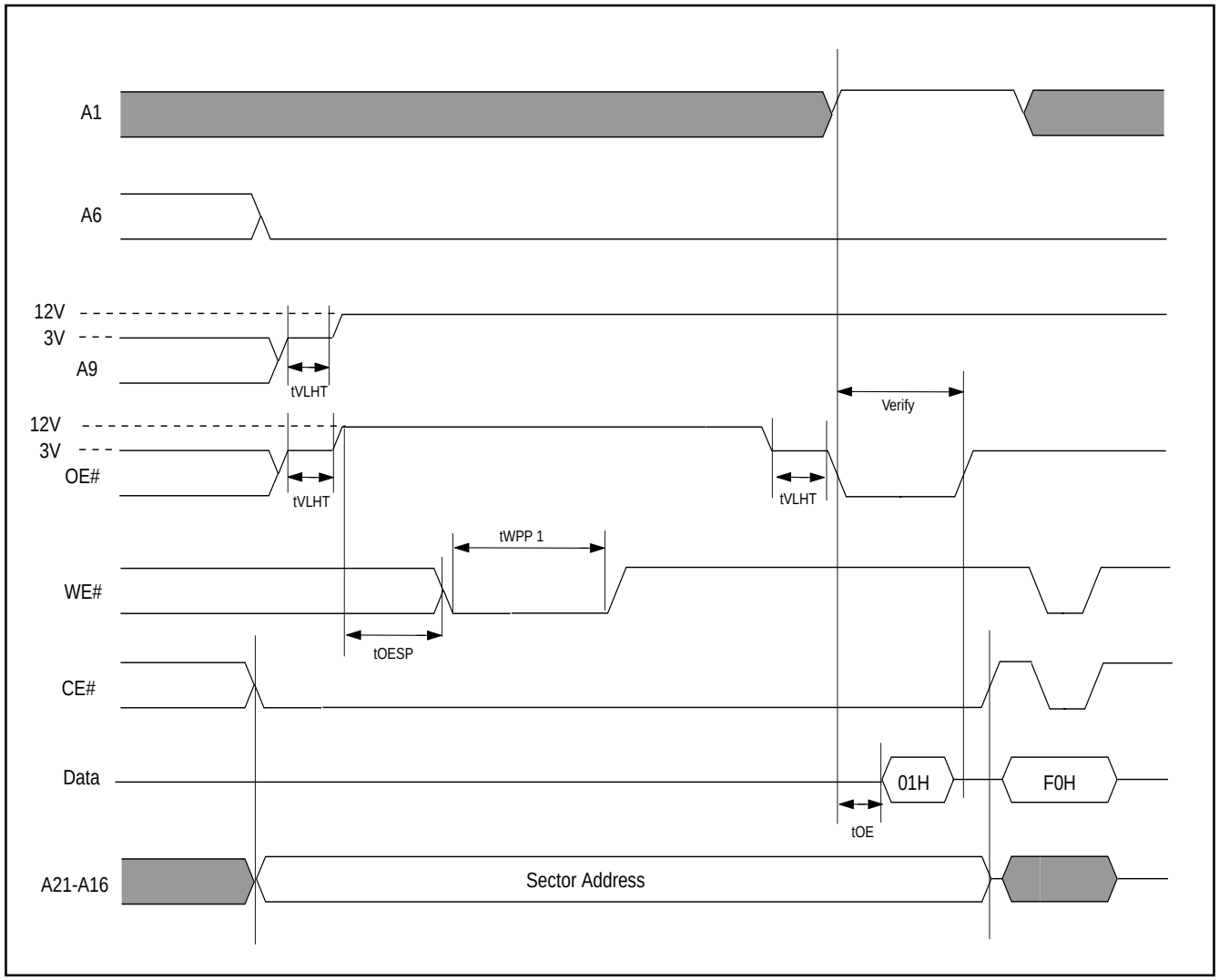


**Figure 16. SECTOR GROUP PROTECTION ALGORITHM (A9, OE# Control)**

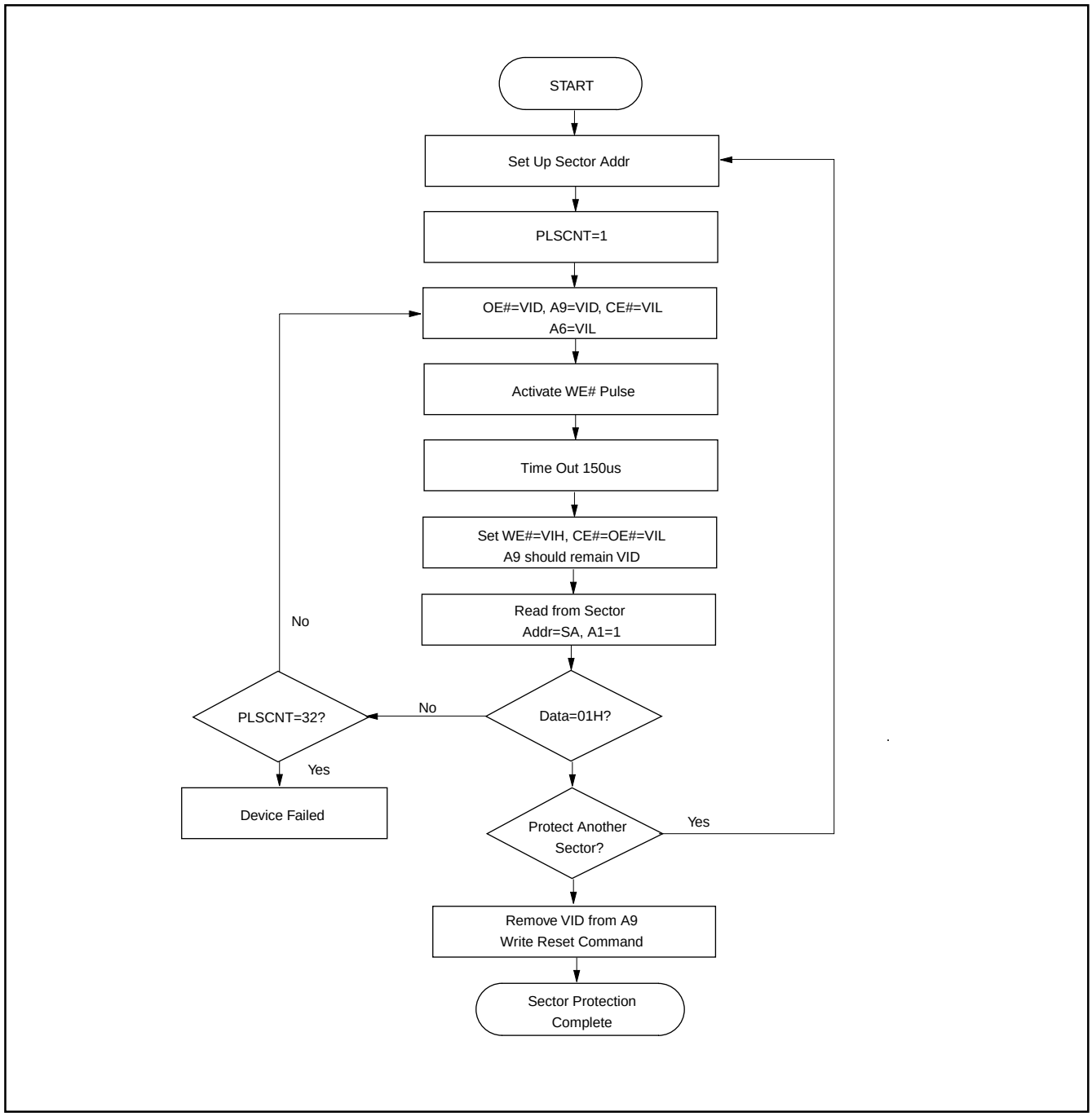


**Figure 17. CHIP UNPROTECTED TIMING WAVEFORM (A9, OE# Control)**

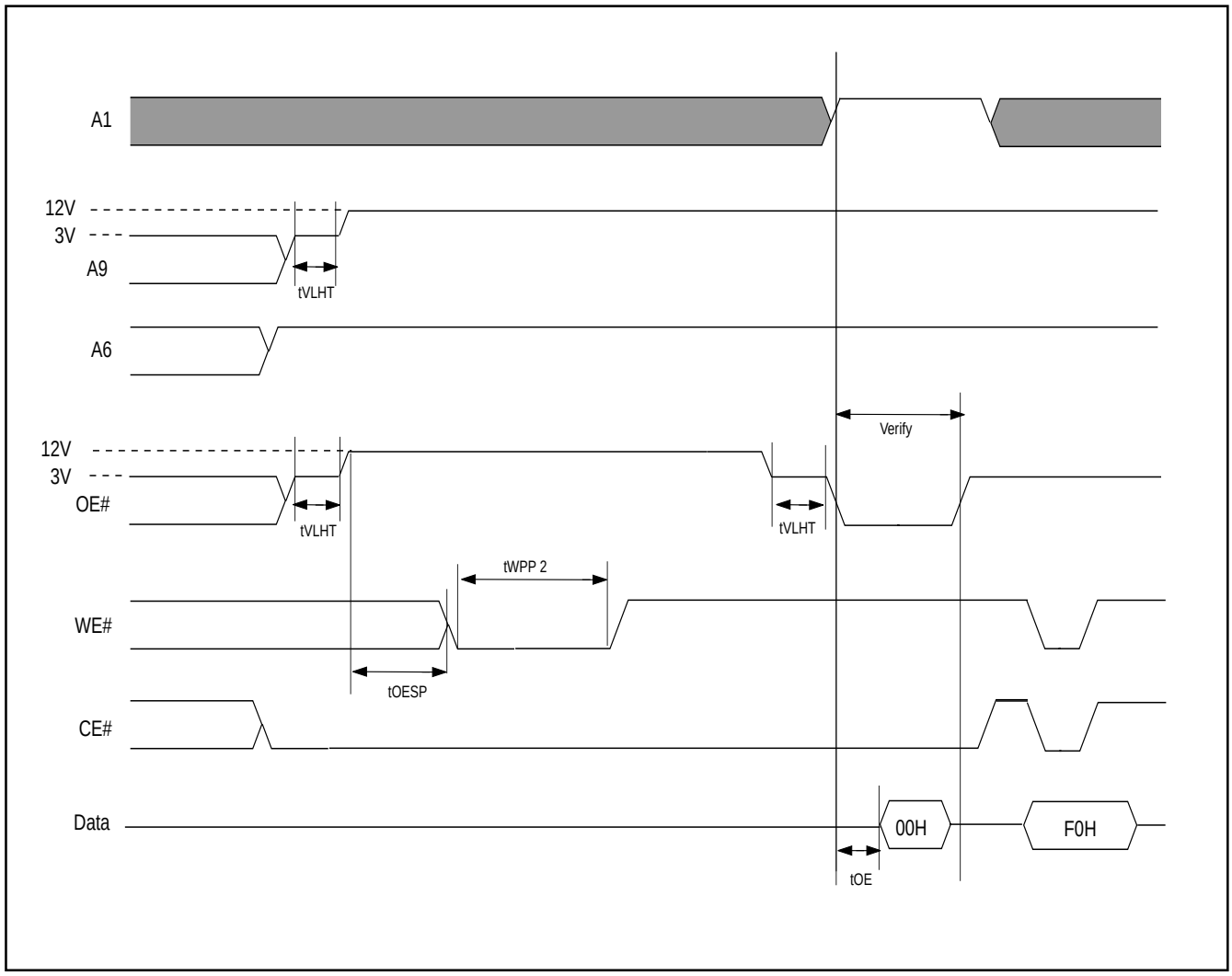
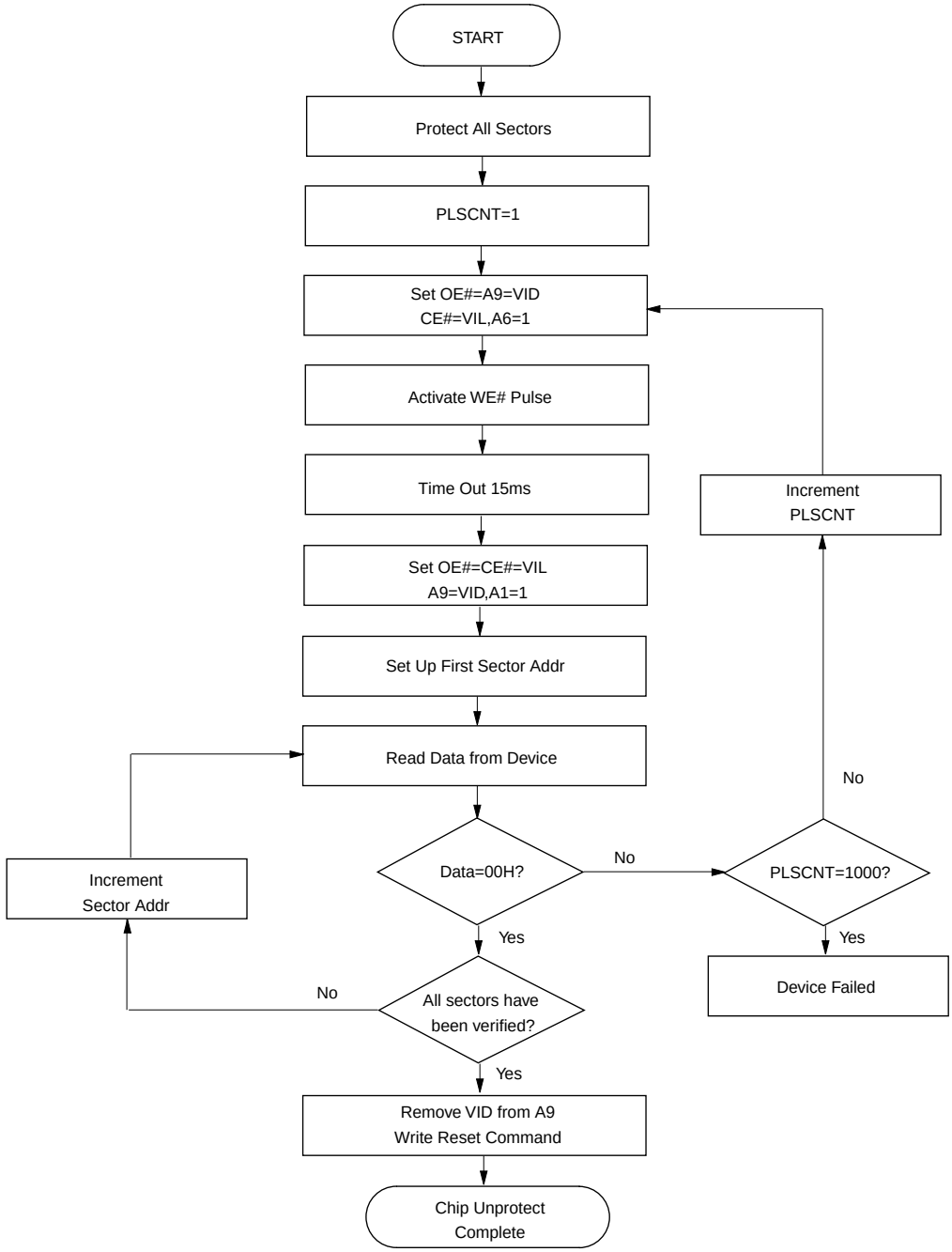


**Figure 18. CHIP UNPROTECTED FLOWCHART (A9, OE# Control)**




* It is recommended before unprotect whole chip, all sectors should be protected in advance.

## AC CHARACTERISTICS

| Parameter | Description | Test Setup | All Speed Options | Unit |
|---|---|---|---|---|
| tVIDR | VID Rise and Fall Time (see Note) | Min | 500 | ns |
| tRSP | RESET# Setup Time for Temporary Sector Unprotected | Min | 4 | us |
| tRRB | RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotected | Min | 4 | us |

**Figure 19. TEMPORARY SECTOR GROUP UNPROTECTED WAVEFORMS**

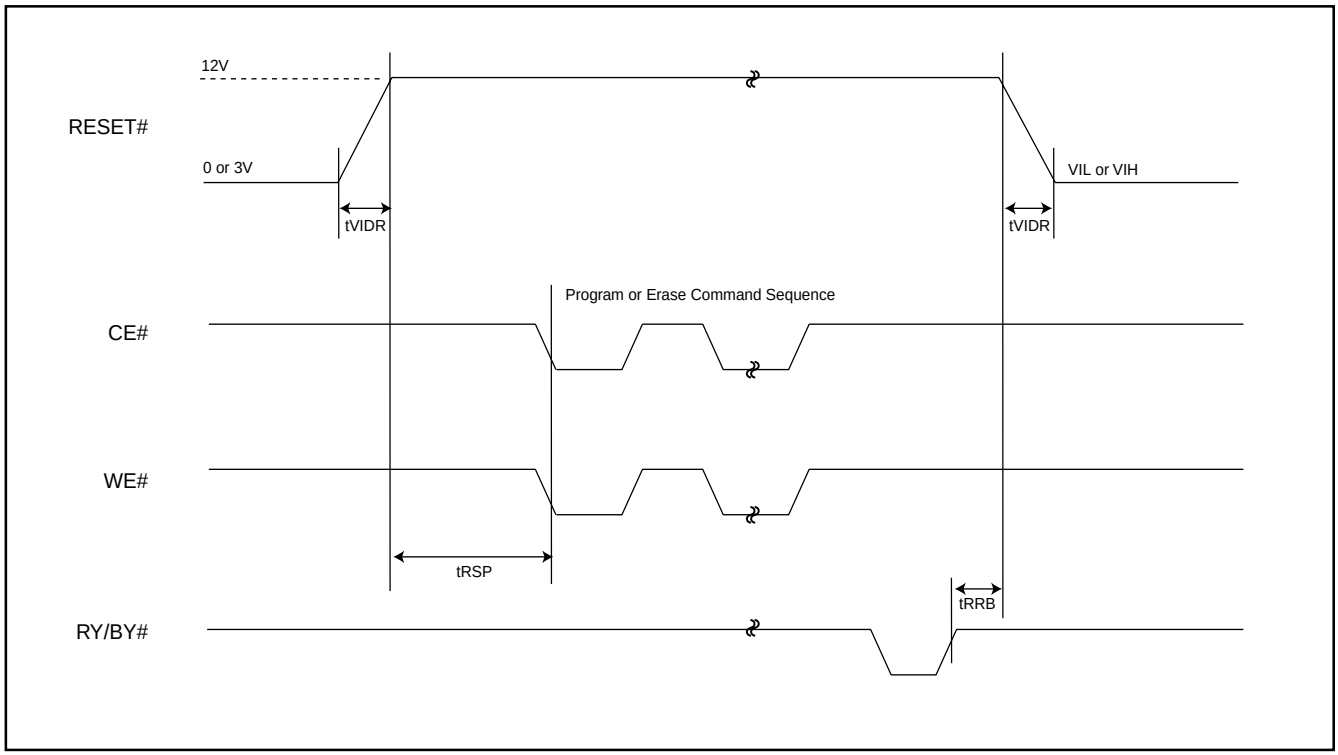
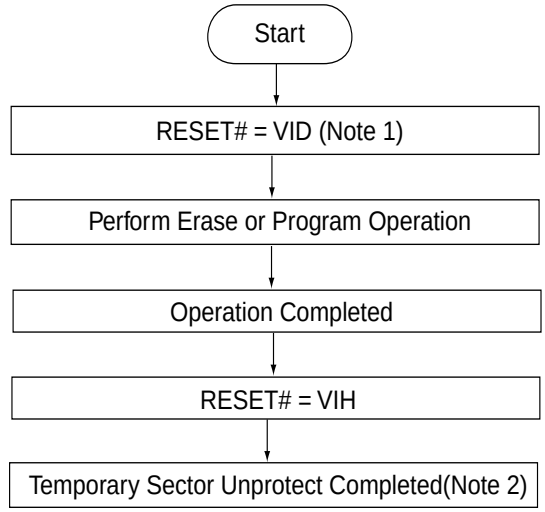


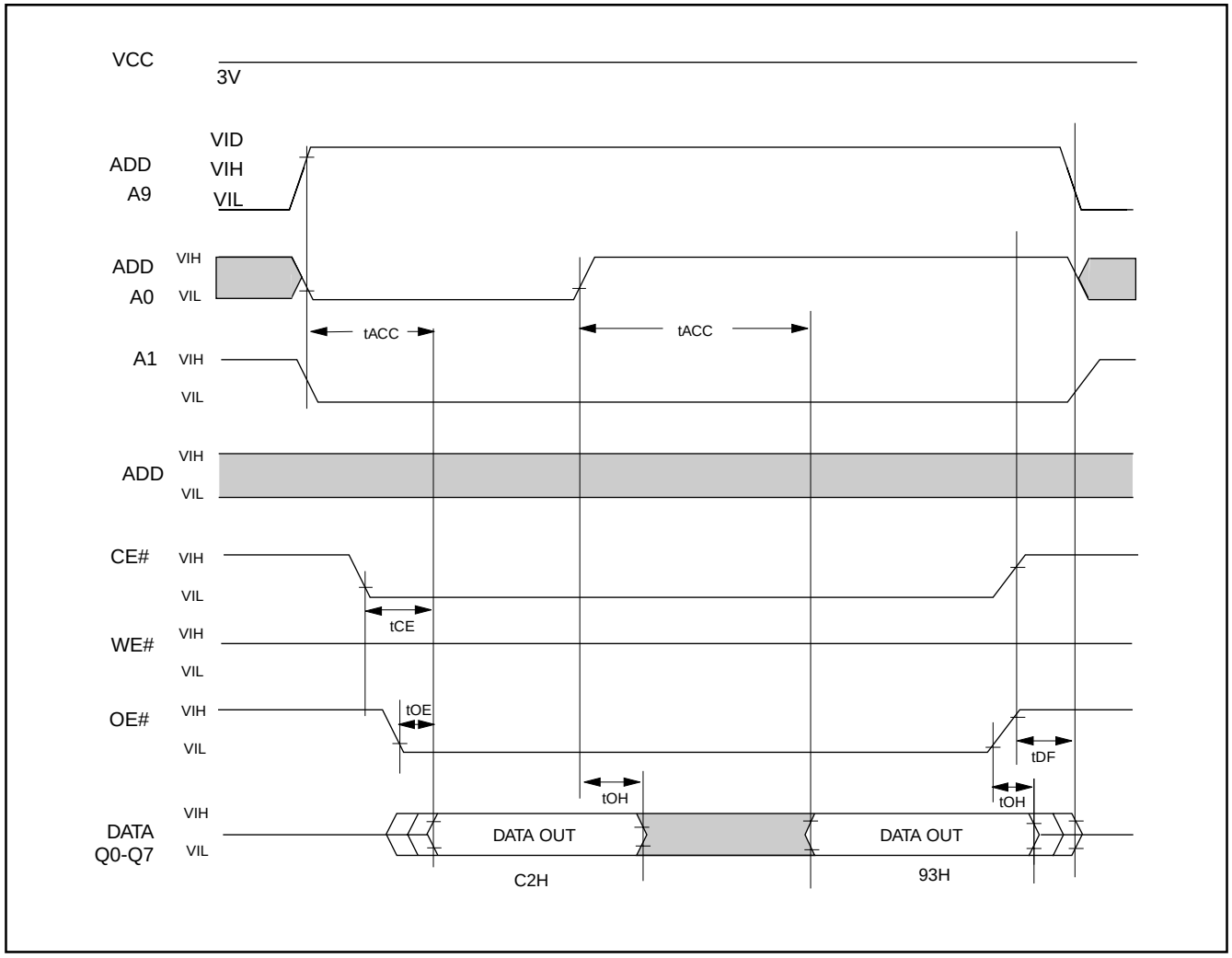
**Figure 20. TEMPORARY SECTOR GROUP UNPROTECTED FLOWCHART**




Notes : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

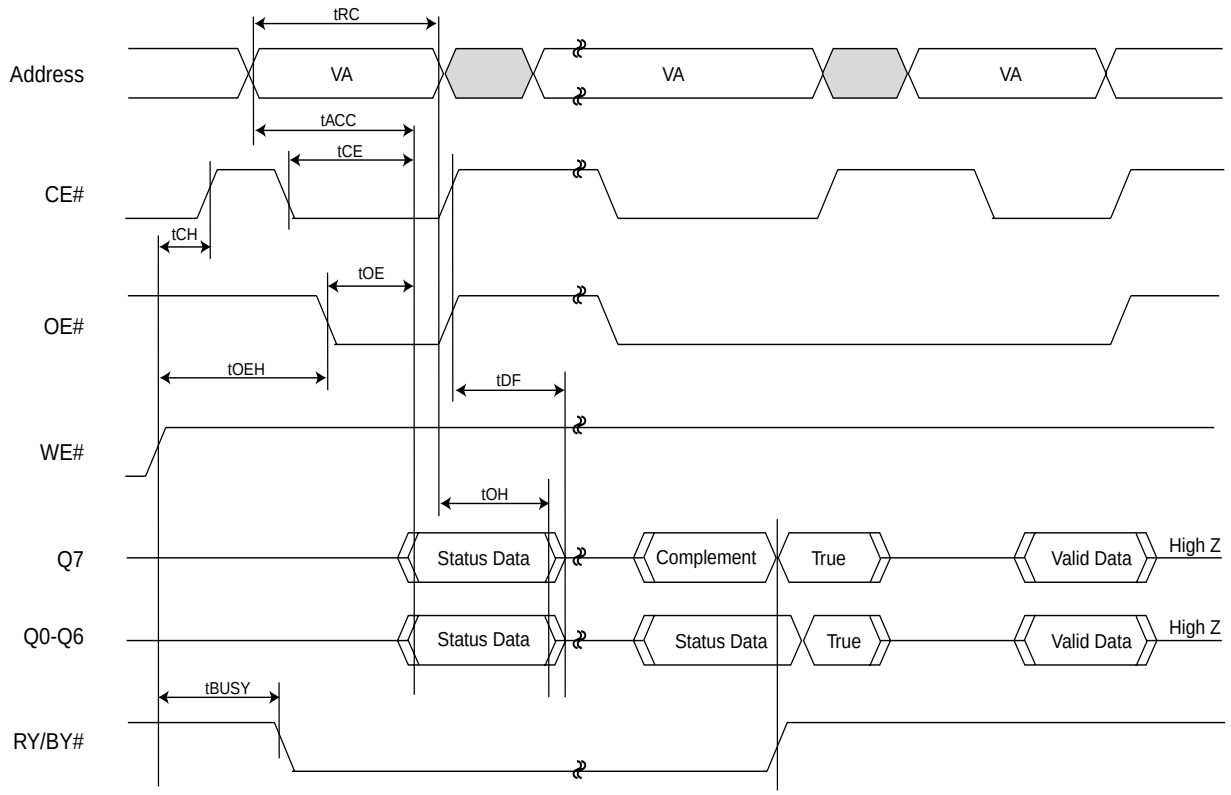
2. All previously protected sectors are protected again.

**Figure 21. SILICON ID READ TIMING WAVEFORM**



## WRITE OPERATION STATUS

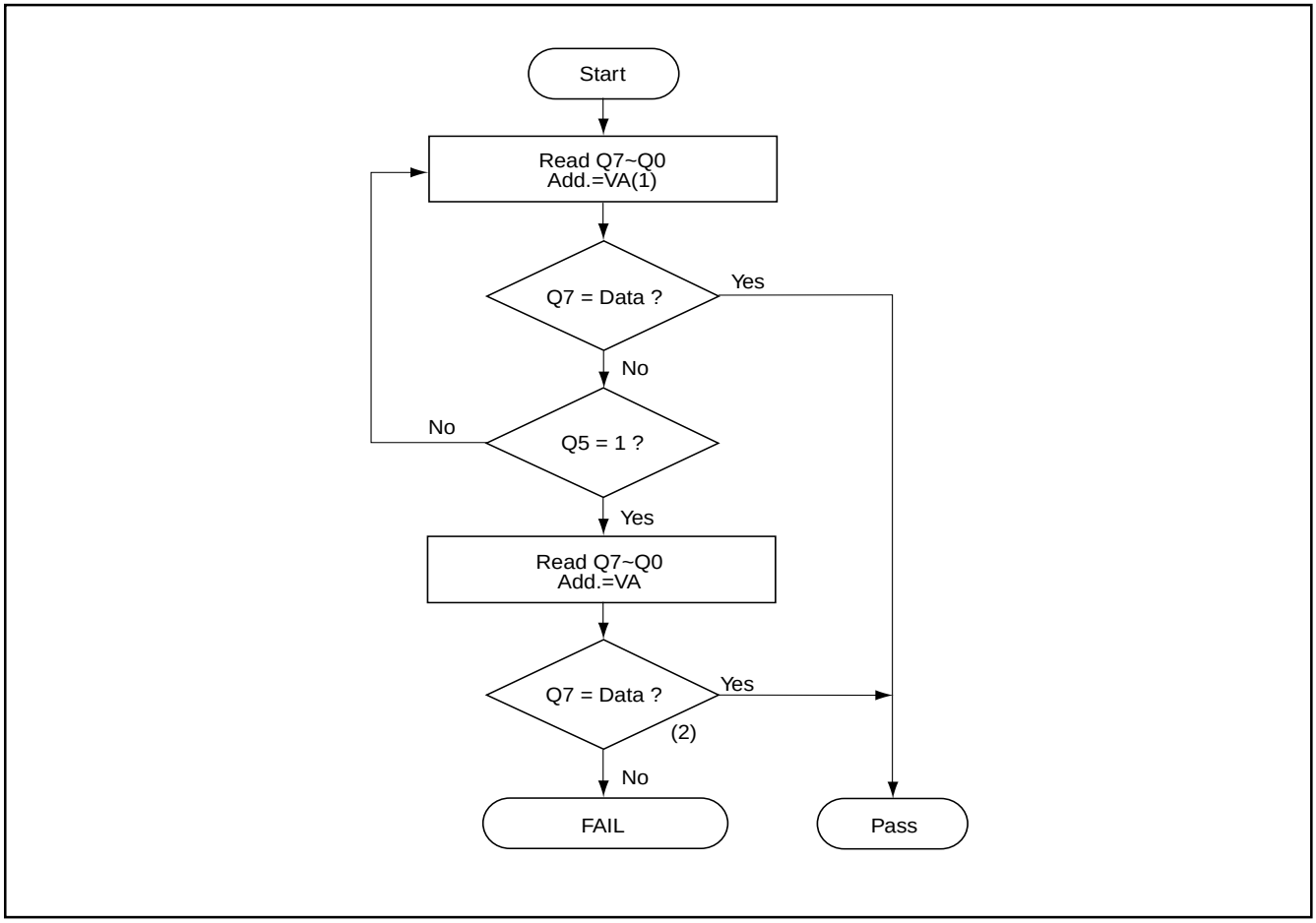
### Figure 22. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)




Note :

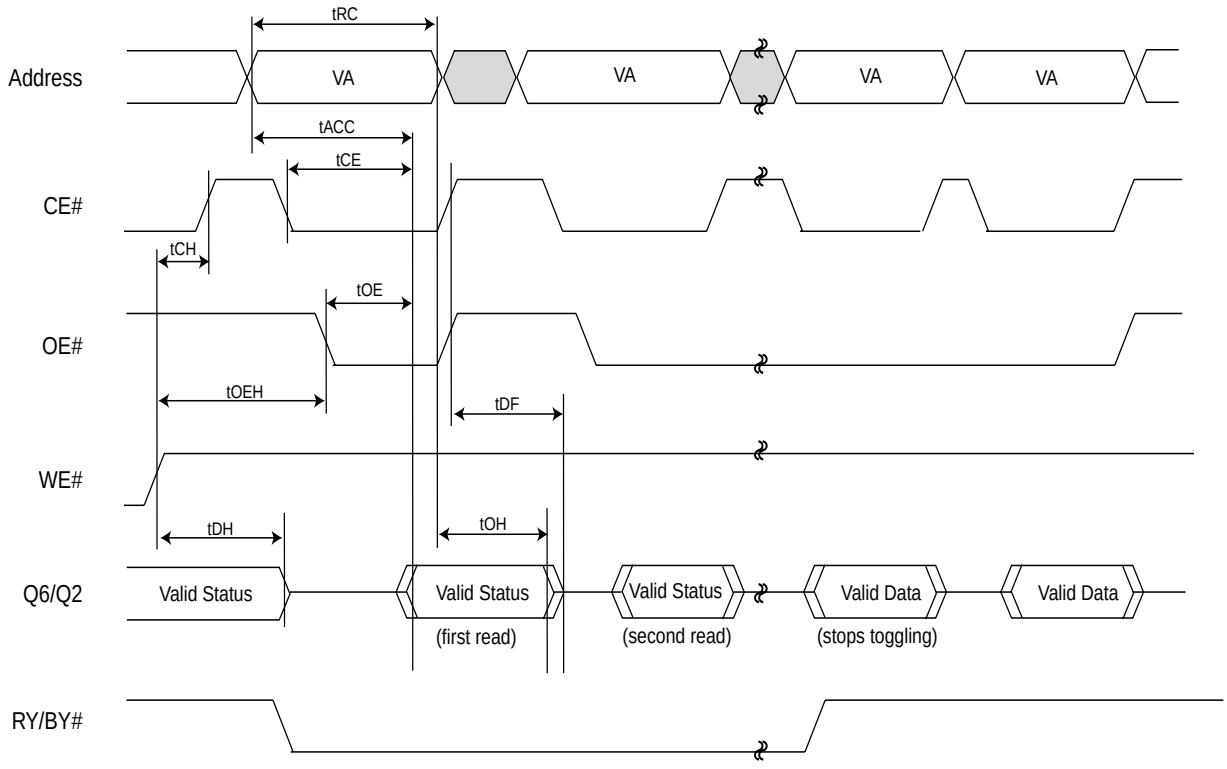
VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

**Figure 23. Data# Polling Algorithm**




Notes:
1.VA=valid address for programming.
2.Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

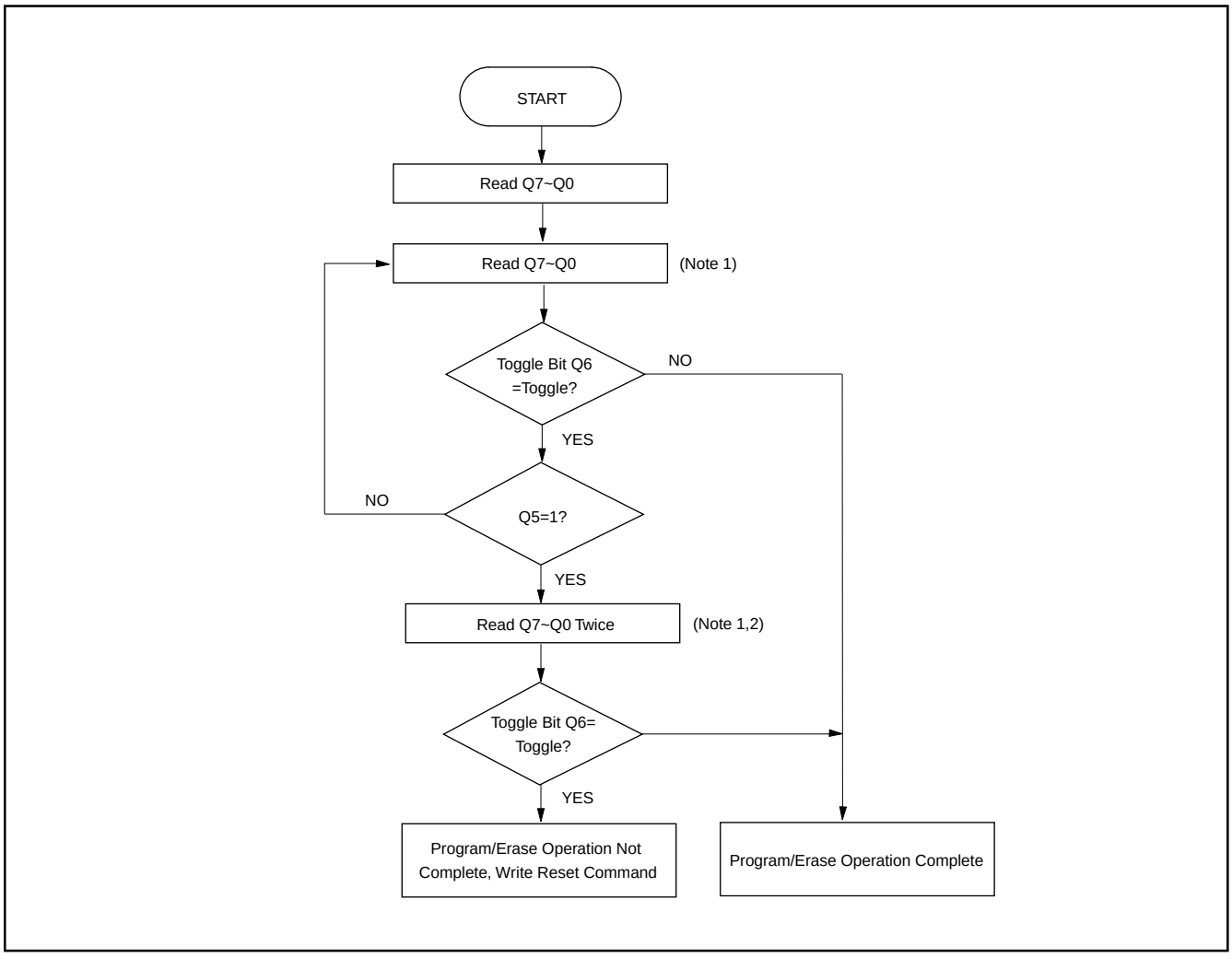
**Figure 24. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**




Note :

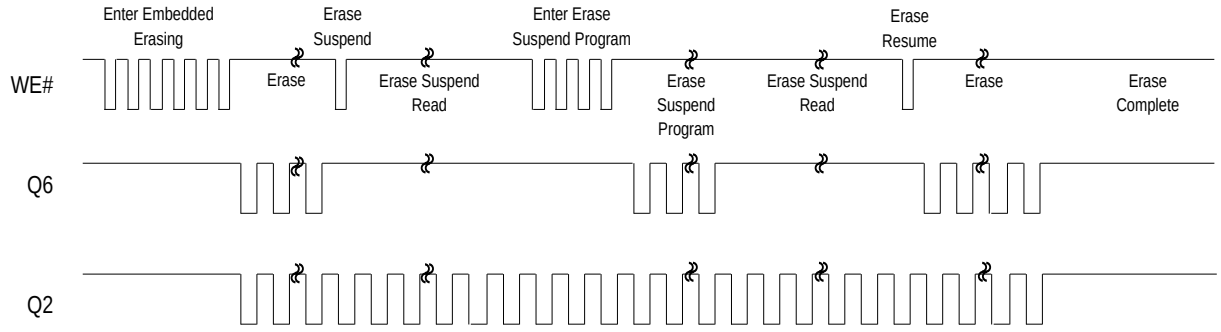
VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

**Figure 25. Toggle Bit Algorithm**




Notes :
1.Read toggle bit twice to determine whether or not it is toggling.
2.Recheck toggle bit because it may stop toggling as Q5 changes to "1".

**Figure 26. Q6 versus Q2**




Note :

The system can use OE# or CE# to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

## ERASE AND PROGRAMMING PERFORMANCE (1)

| PARAMETER | LIMITS | | | UNITS |
|---|---|---|---|---|
| | MIN. | TYP.(2) | MAX. | |
| Sector Erase Time | | 0.9 | 15 | sec |
| Chip Erase Time | | 45 | 65 | sec |
| Byte Programming Time | | 7 | 150 | us |
| Accelerated Byte Program Time | | 4 | 120 | us |
| Chip Programming Time | | 42 | 126 | sec |
| Erase/Program Cycles | 100,000 | | | Cycles |

Note: 1. Not 100% Tested, Excludes external system level over head.
2. Typical program and erase times assume the following condition= 25° C,3.0V VCC. Additionally, programming typical assume checkerboard pattern.

## LATCH-UP CHARACTERISTICS

| | MIN. | MAX. |
|---|---|---|
| Input Voltage with respect to GND on all pins except I/O pins | -1.0V | 13.5V |
| Input Voltage with respect to GND on all I/O pins | -1.0V | VCC + 1.0V |
| Current | -100mA | +100mA |
| Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time. | | |

## TSOP PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Set | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CIN | Input Capacitance | VIN=0 | 6 | 7.5 | pF |
| COUT | Output Capacitance | VOUT=0 | 8.5 | 12 | pF |
| CIN2 | Control Pin Capacitance | VIN=0 | 7.5 | 9 | pF |

**Notes:**
1. Sampled, not 100% tested.
2. Test conditions TA=25° C, f=1.0MHz

## DATA RETENTION

| Parameter | Test Conditions | Min | Unit |
|---|---|---|---|
| Minimum Pattern Data Retention Time | 150° C | 10 | Years |
| | 125° C | 20 | Years |

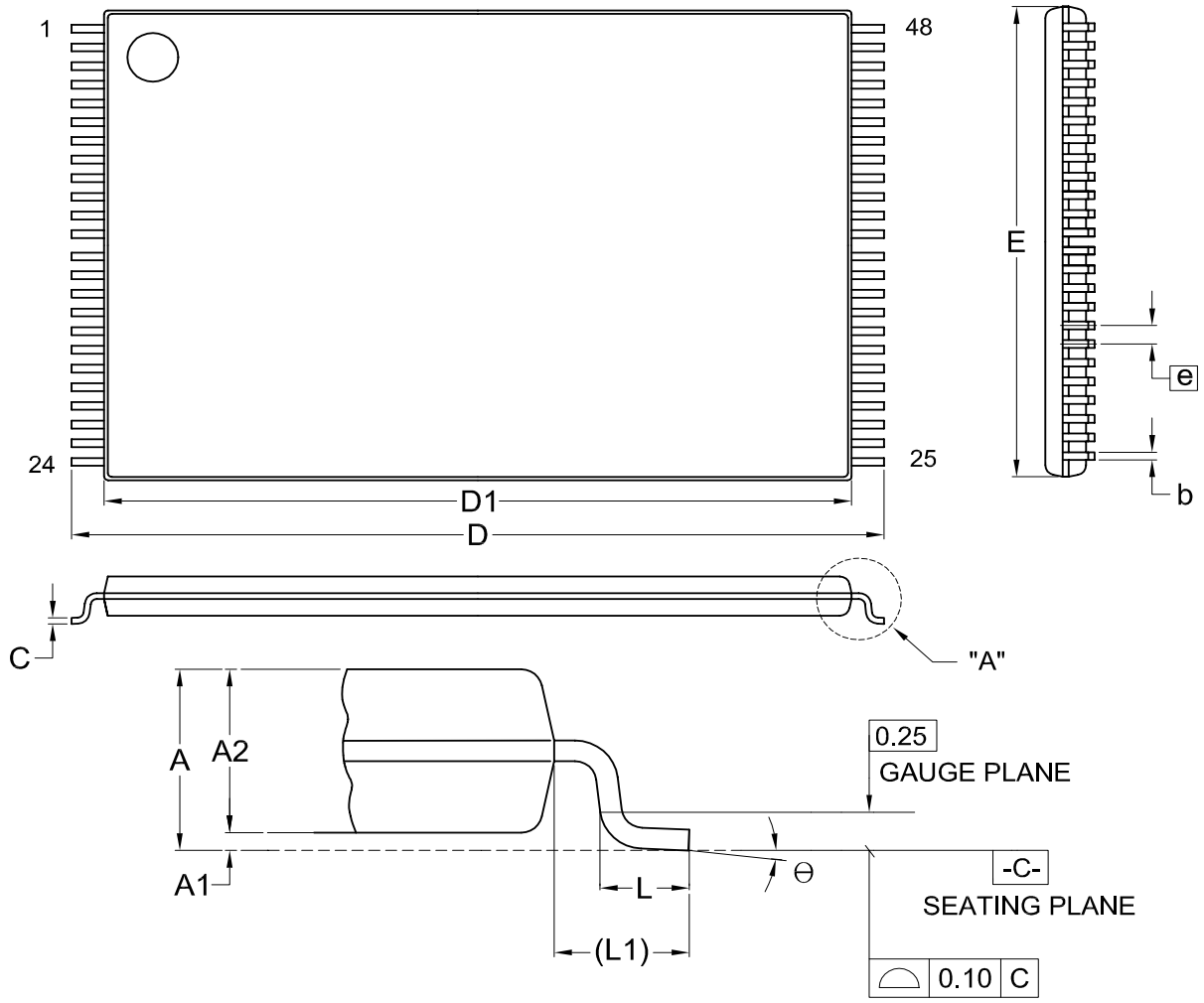
## ORDERING INFORMATION

### PLASTIC PACKAGE

| PART NO. | ACCESS TIME (ns) | Ball Pitch/ Ball size | PACKAGE | Remark |
|---|---|---|---|---|
| MX29LV065BTC-90 | 90 | | 48 Pin TSOP (Normal Type) | Commercial grade |
| MX29LV065BTC-12 | 120 | | 48 Pin TSOP (Normal Type) | Commercial grade |
| MX29LV065BTI-90 | 90 | | 48 Pin TSOP (Normal Type) | Industrial grade |
| MX29LV065BTI-12 | 120 | | 48 Pin TSOP (Normal Type) | Industrial grade |
| MX29LV065BTC-90G | 90 | | 48 Pin TSOP (Normal Type) | Commercial grade Pb-free |
| MX29LV065BTC-12G | 120 | | 48 Pin TSOP (Normal Type) | Commercial grade Pb-free |
| MX29LV065BTI-90G | 90 | | 48 Pin TSOP (Normal Type) | Industrial grade Pb-free |
| MX29LV065BTI-12G | 120 | | 48 Pin TSOP (Normal Type) | Industrial grade Pb-free |

## PACKAGE INFORMATION

**Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**




DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 11.90 | | 0.50 | 0.70 | 0 |
| | Nom. | --- | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 12.00 | 0.50 | 0.60 | 0.80 | 5 |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 12.10 | | 0.70 | 0.90 | 8 |
| Inch | Min. | --- | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.469 | | 0.020 | 0.028 | 0 |
| | Nom. | --- | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.472 | 0.020 | 0.024 | 0.031 | 5 |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.476 | | 0.028 | 0.035 | 8 |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-1607 | 7 | MO-142 | | | 12-01-'03 |

## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1. Removed "Preliminary" | P1 | MAR/08/2005 |
| 1.1 | 1. Removed 63-CSP package information | All | JAN/09/2006 |

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