MX25U12873G

1.8V, 128M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Protocol Support - Single I/O, Dual I/O and Quad I/O*
- *Supports DTR (Double Transfer Rate) Mode*
- *Supports clock frequencies up to 133MHz*
- *Quad Peripheral Interface (QPI) Read / Program Mode*
- *Quad I/O mode is permanently enabled*

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1.8V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 1.65 to 2.0 volts for read, erase, and program operations
- 134,217,728 x 1 bit structure
  or 67,108,864 x 2 bits (two I/O mode) structure
  or 33,554,432 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V
- Fast read for SPI mode
  - Supports clock frequencies up to 133MHz
  - Supports Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Supports DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Supports Performance Enhance Mode - XIP (execute-in-place)
- Quad Peripheral Interface (QPI) available
- Default Quad I/O enable (QE bit=1), and can not be changed
- Equal 4K byte sectors, or Equal Blocks with 32K bytes or 64K bytes each
  - Any Block can be erased individually
- Programming:
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Individual Block Protection when OTP WPSEL=1
- Additional 4K bit Secure OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Supports Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SIO2
  - Serial Data Input/Output for 4 x I/O read mode
- SIO3
  - Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (200mil)
  - 8-land WSON (6x5mm)

  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25U12873G is 128Mb bits Serial NOR Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4. MX25U12873G features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output.

The MX25U12873G MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please refer to the security features section for more details.

When the device is not in operation and CS# is high, it will remain in standby mode.

The MX25U12873G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

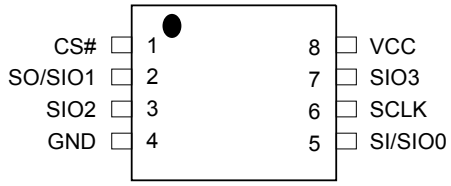
Table 1. Read performance Comparison

Numbers of Dummy Cycles	SPI						QPI	
	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual I/O Fast Read (MHz)	Quad I/O Fast Read (MHz)	Quad I/O DT Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	84*	66	-	66	-
6	-	-	-	-	84*	54*	84*	54*
8	133*	133*	133*	133	104	66	104	66
10	-	-	-	-	133	84	133	84

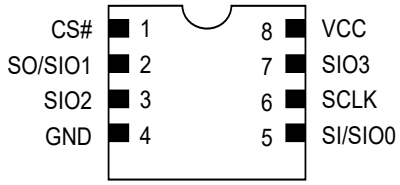
Notes: * Default status.

3. PIN CONFIGURATIONS

8-PIN SOP (200mil)



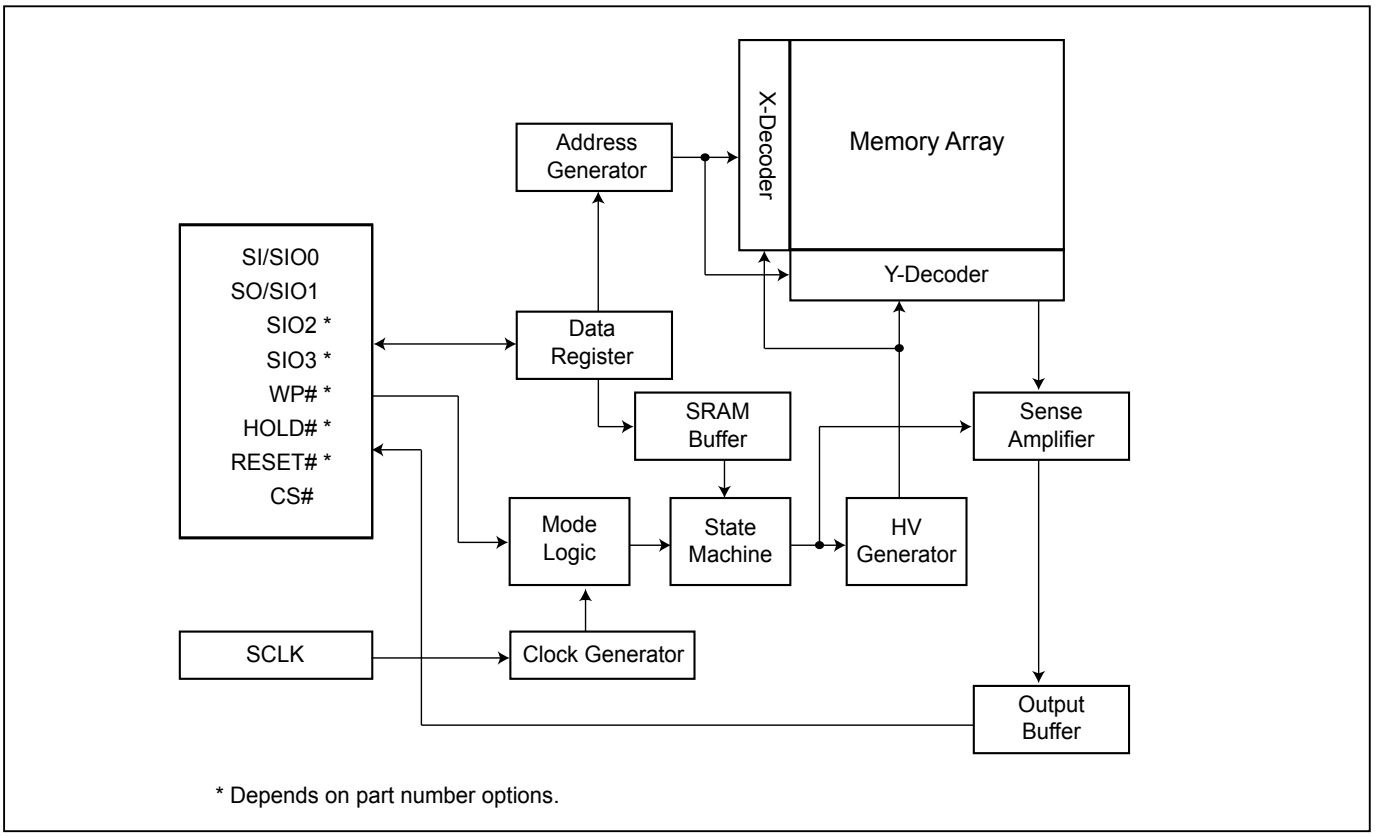
8-WSON (6x5mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
SIO2	Serial Data Input & Output (for 4xI/O read mode)
SIO3	Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground
NC	No Connection

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 of Status Register and T/B of Configuration Register) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 255th)
0	0	1	0	2 (2 blocks, block 254th-255th)
0	0	1	1	3 (4 blocks, block 252nd-255th)
0	1	0	0	4 (8 blocks, block 248th-255th)
0	1	0	1	5 (16 blocks, block 240th-255th)
0	1	1	0	6 (32 blocks, block 224th-255th)
0	1	1	1	7 (64 blocks, block 192nd-255th)
1	0	0	0	8 (128 blocks, block 128th-255th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th-1st)
0	0	1	1	3 (4 blocks, protected block 0th-3rd)
0	1	0	0	4 (8 blocks, protected block 0th-7th)
0	1	0	1	5 (16 blocks, protected block 0th-15th)
0	1	1	0	6 (32 blocks, protected block 0th-31st)
0	1	1	1	7 (64 blocks, protected block 0th-63rd)
1	0	0	0	8 (128 blocks, protected block 0th-127th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

II. Additional 4K-bit secured OTP for an unique identifier to provide an 4K-bit one-time program area for setting a device unique serial number. This may be accomplished in the factory or by an end systems customer.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- The 4K-bit secured OTP area is programmed by entering secured OTP mode (with the Enter Security OTP command), and going through a normal program procedure. Exiting secured OTP mode is done by issuing the Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 12. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx1FF	4096-bit	Determined by Factory	Determined by Customer

7. Memory Organization

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
255	511	4095	FFF000h	FFFFFFh
		⋮		
		4088	FF8000h	FF8FFFh
	510	4087	FF7000h	FF7FFFh
		⋮		
		4080	FF0000h	FF0FFFh
254	509	4079	FEF000h	FEFFFFh
		⋮		
		4072	FE8000h	FE8FFFh
	508	4071	FE7000h	FE7FFFh
		⋮		
		4064	FE0000h	FE0FFFh
253	507	4063	FDF000h	FDFFFFh
		⋮		
		4056	FD8000h	FD8FFFh
	506	4055	FD7000h	FD7FFFh
		⋮		
		4048	FD0000h	FD0FFFh
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When an incorrect command is written to this device, it enters standby mode and stays in the standby mode until the next CS# falling edge. In standby mode, the device's SO pin should be High-Z.

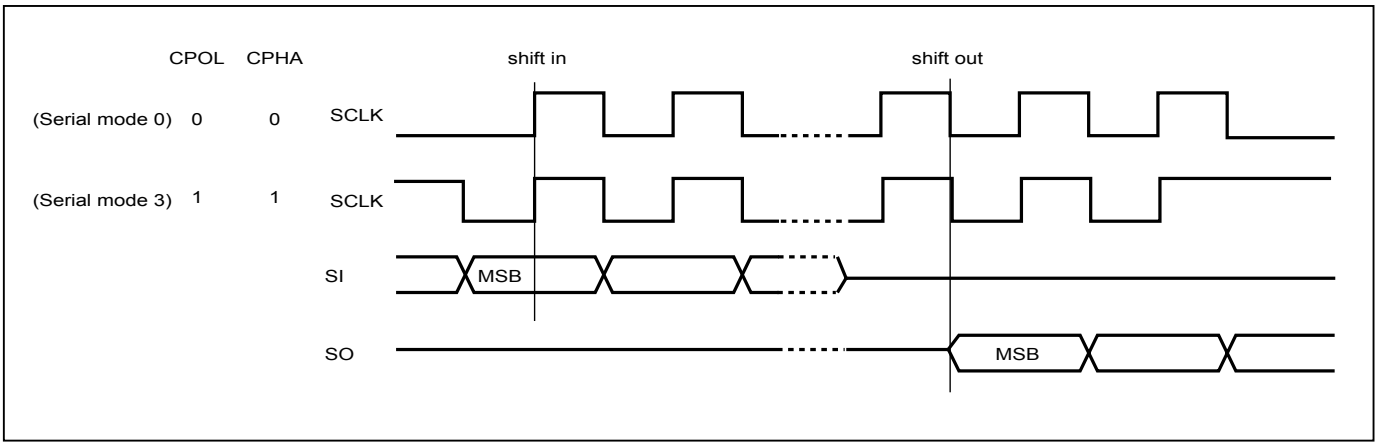
3. When an correct command is written to this device, it enters active mode and stays in the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, W4READ, QREAD, RDSFDP, RES, REMS, QPIID, RDBLOCK, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing (STR mode)

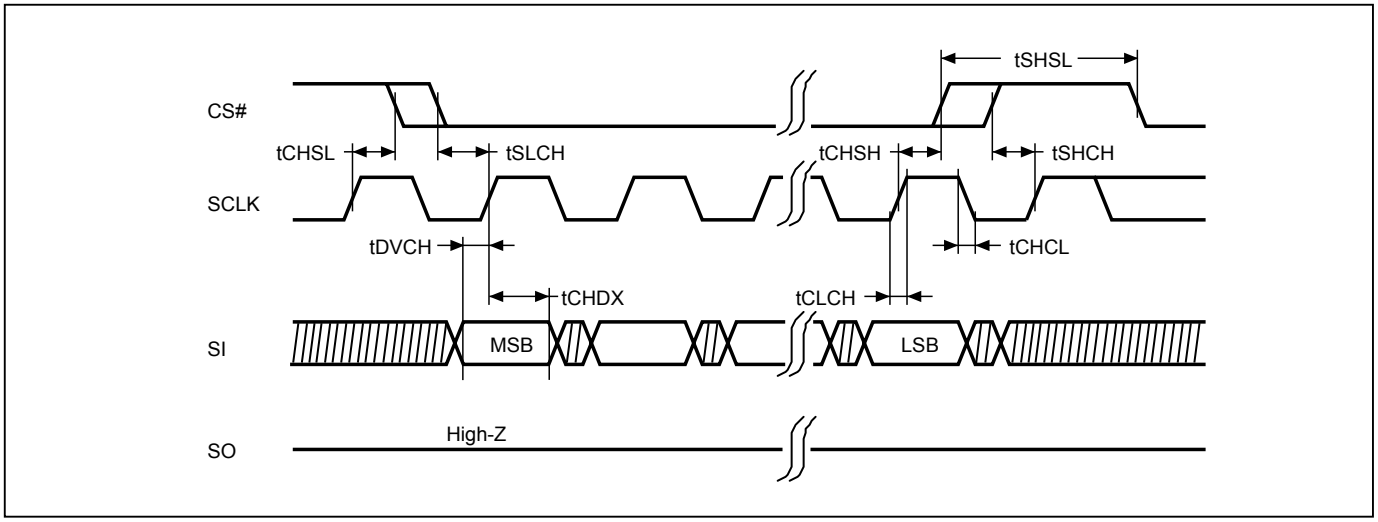


Figure 3. Serial Input Timing (DTR mode)

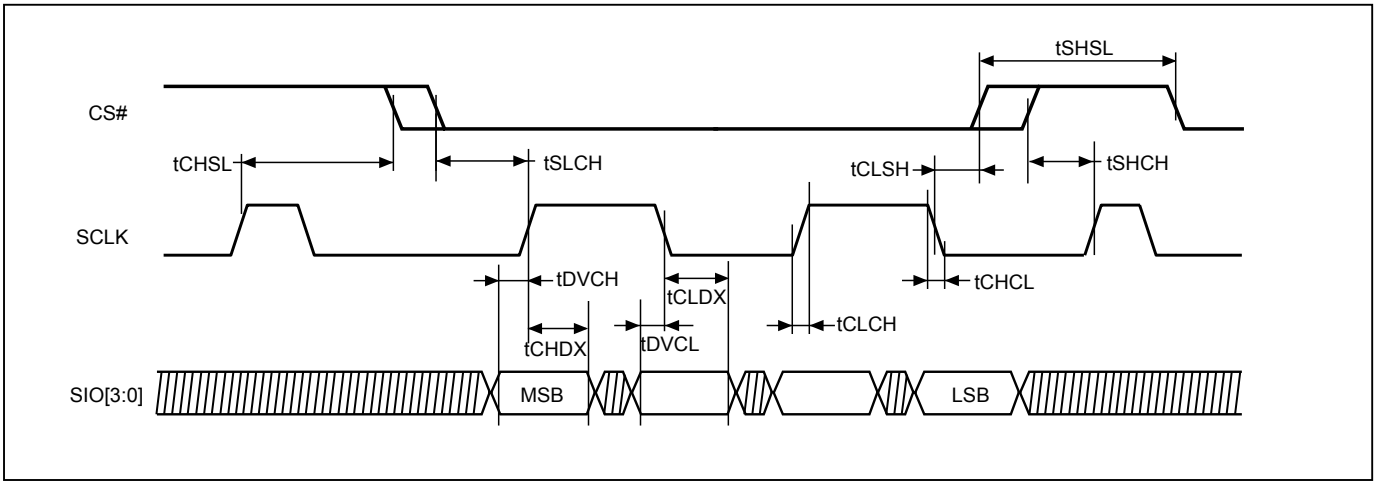


Figure 4. Output Timing (STR mode)

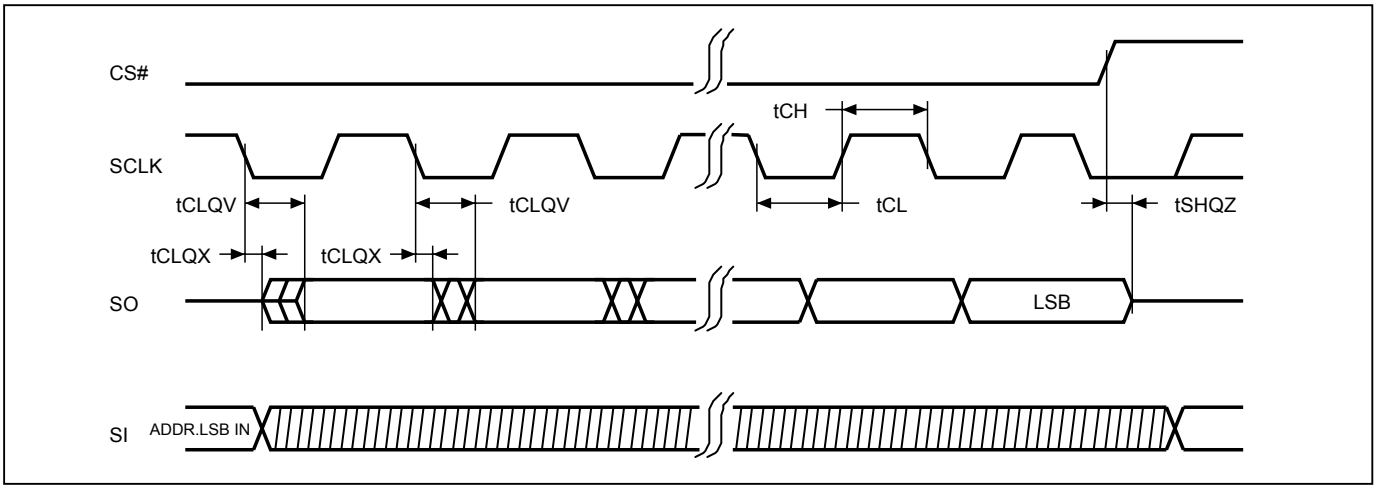
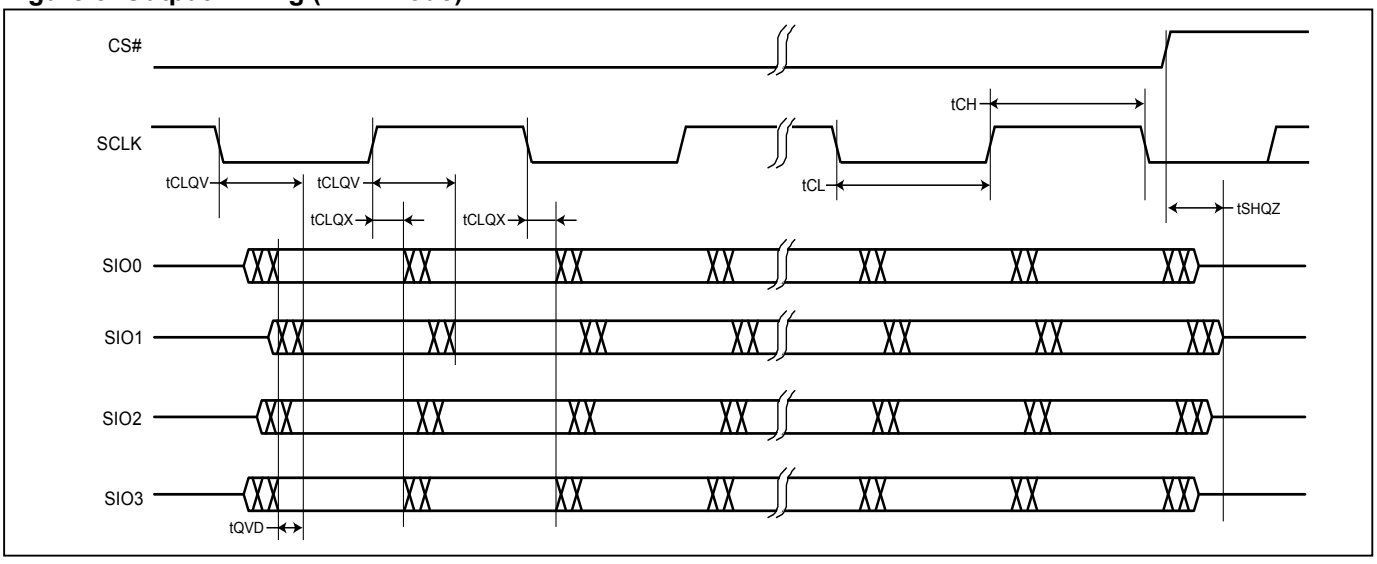


Figure 5. Output Timing (DTR mode)



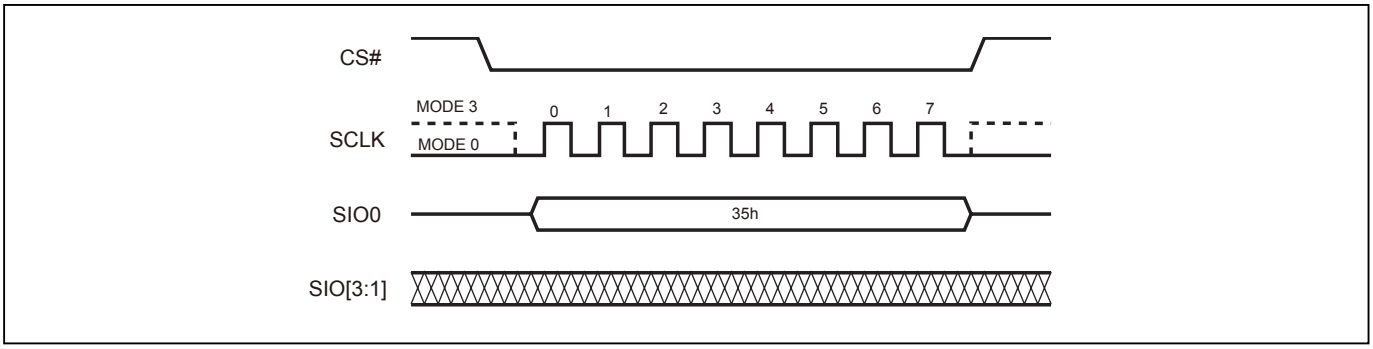
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing EQIO(35h) command, the QPI mode is enabled. After QPI mode is enabled, the device enters quad mode (4-4-4).

Figure 6. Enable QPI Sequence

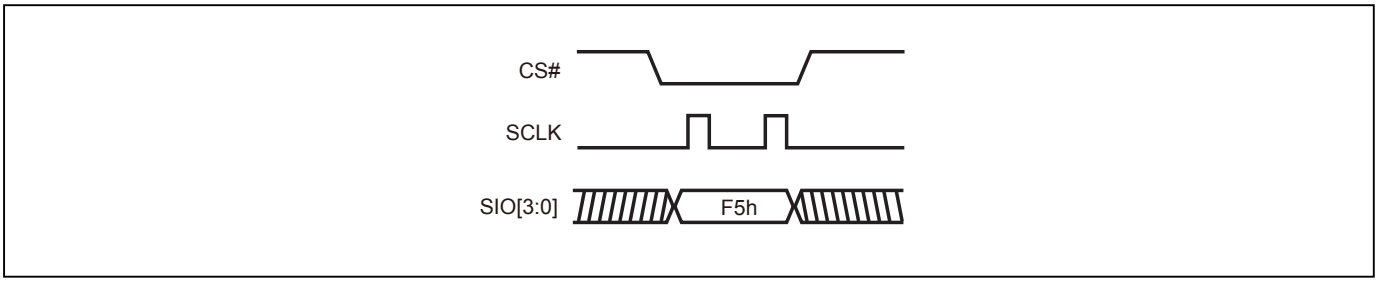


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register" specification of tSHSL (as defined by *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"*) for next instruction.

Figure 7. Reset QPI Mode



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)(Note 1)	DREAD (1I 2O read)	4READ (4 x I/O read command)(Note 5)	W4READ	QREAD (1I 4O read)
Mode	SPI	SPI/QPI	SPI	SPI	SPI/QPI	SPI/QPI	SPI
Address Bytes	3	3	3	3	3	3	3
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	E7 (hex)	6B (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy(8)/(4) (Note 6)	Dummy(8)/(4)	Dummy(8)	Dummy(10)/ (8)/(6)/(4)	Dummy(4)	Dummy(8)
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	Quad I/O read for with 4 dummy cycles	n bytes read out by Quad output until CS# goes high

Command (byte)	4DTRD (Quad I/O DT Read)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3	3	3	3	3	3	0
1st byte	ED (hex)	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte	ADD1		ADD1	ADD1	ADD1	ADD1	
3rd byte	ADD2		ADD2	ADD2	ADD2	ADD2	
4th byte	ADD3		ADD3	ADD3	ADD3	ADD3	
5th byte	Dummy(10)/ (8)/(6)						
Data Cycles		1-256	1-256				
Action	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	FMEN (factory mode enable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	WPSEL (Write Protect Selection)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	06 (hex)	04 (hex)	41 (hex)	05 (hex)	15 (hex)	01 (hex)	68 (hex)
2nd byte						Values	
3rd byte						Values	
4th byte							
5th byte							
Data Cycles						1-2	
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	enable factory mode	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register	to enter and enable individual block protect mode

Command (byte)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)
Mode	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	35 (hex)	F5 (hex)	75 or B0 (hex)	7A or 30 (hex)	B9 (hex)	AB (hex)	C0 (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles							
Action	Entering the QPI mode	Exiting the QPI mode			enters deep power down mode	release from deep power down mode	to set Burst length

ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy(8)(Note 5)		
Data Cycles							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID(Note 2)	ID in QPI interface	Read SFDP mode	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	SBLK (single block lock	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	3	3	3	0	0
1st byte	2B (hex)	2F (hex)	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)
2nd byte			ADD1	ADD1	ADD1		
3rd byte			ADD2	ADD2	ADD2		
4th byte			ADD3	ADD3	ADD3		
5th byte							
Data Cycles							
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)(Note 4)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.
Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 4: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.
Note 5: The number in parentheses after "Dummy" stands for how many clock cycles it has. Dummy cycle number will be different, depending on the bit7 (DC) setting of Configuration Register. Please refer to *"Table 8. Configuration Register"*.
Note 6: The fast read command (0Bh) when under QPI mode, the dummy cycle is 4 clocks.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit. Instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR that are intended to change the device content, should be preceded by the WREN instruction.

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 8. Write Enable (WREN) Sequence (SPI Mode)

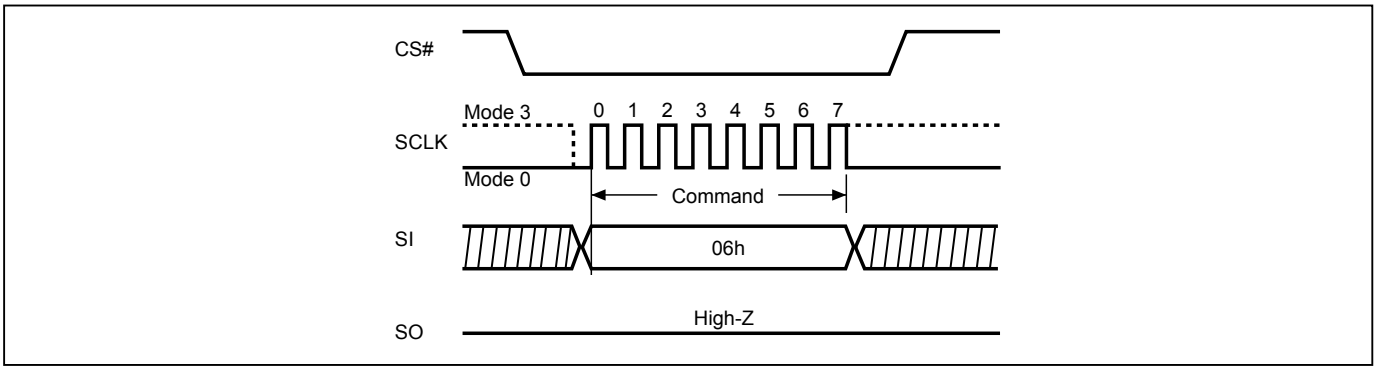
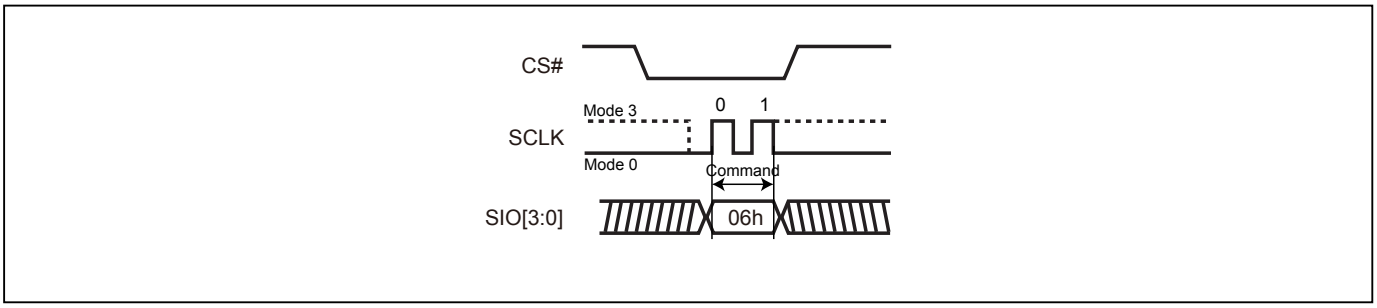


Figure 9. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset in the following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion

Figure 10. Write Disable (WRDI) Sequence (SPI Mode)

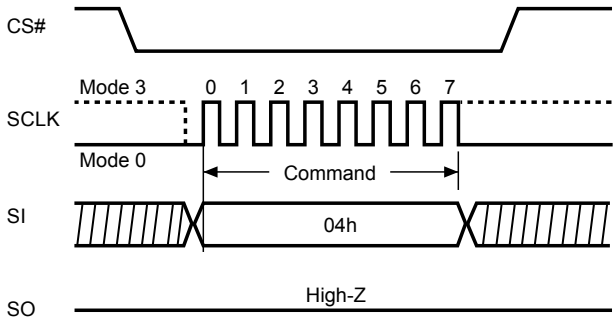
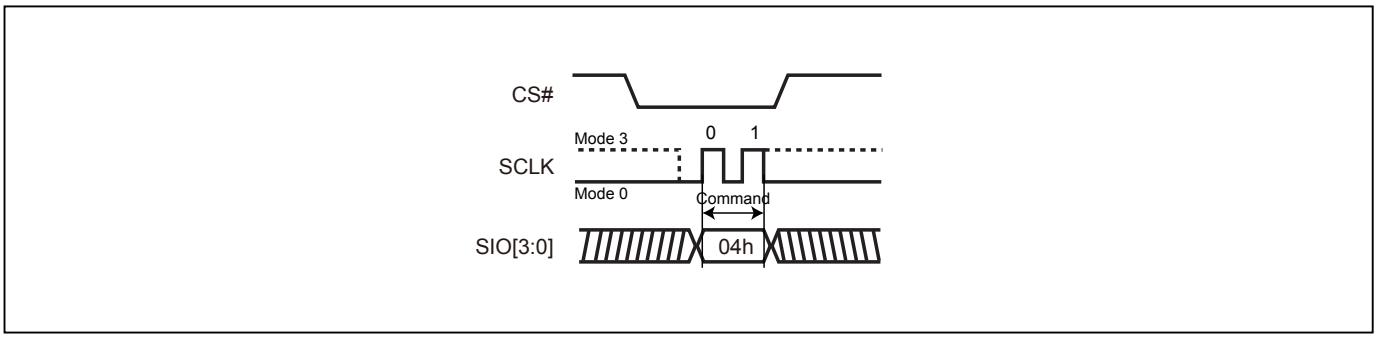


Figure 11. Write Disable (WRDI) Sequence (QPI Mode)



9-3. Factory Mode Enable (FMEN)

The Factory Mode Enable (FMEN) instruction enhances Program and Erase performance to increase factory production throughput. The FMEN instruction needs to combine with the instructions which are intended to change the device content, like PP, 4PP, SE, BE32K, BE, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

Suspend command is not acceptable under factory mode.

The FMEN is reset in the following situations

- Power-up
- Reset# pin driven low
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- Softreset command completion

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 12. Factory Mode Enable (FMEN) Sequence (SPI Mode)

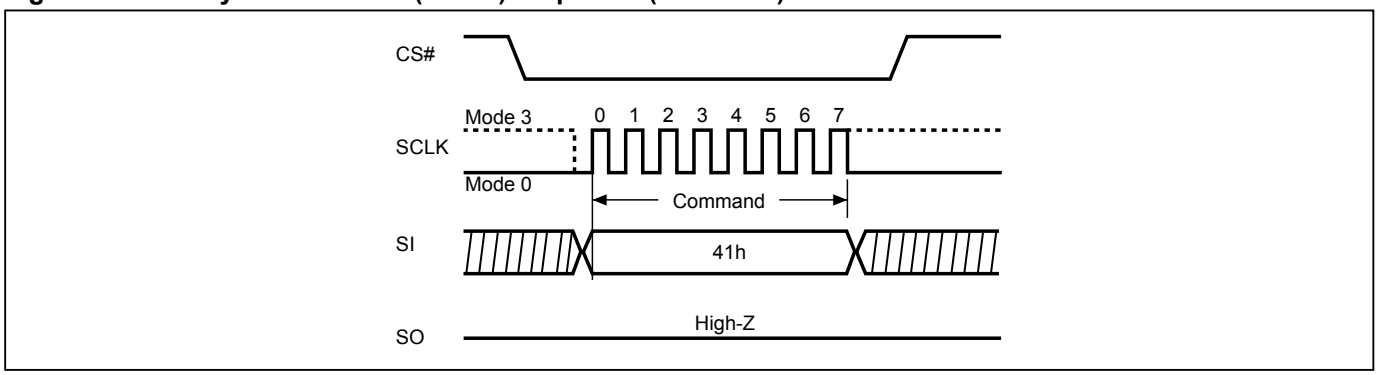
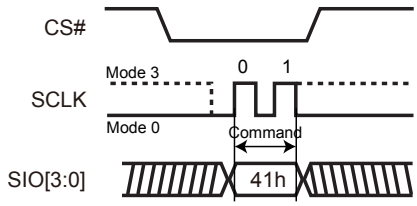


Figure 14. Factory Mode Enable (FMEN) Sequence (QPI Mode)



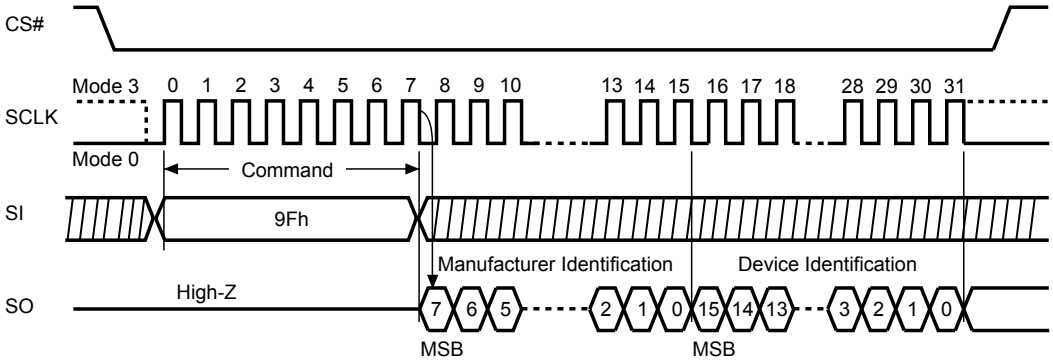
9-4. Read Identification (RDID)

The RDID instruction is for reading the 1-byte manufacturer ID and the 2-byte Device ID that follows. The Macronix Manufacturer ID and Device ID are listed as *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ send RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 13. Read Identification (RDID) Sequence (SPI mode only)



9-5. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature ID, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The RDP and RES are allowed to execute in Deep power-down mode, except if the device is in progress of program/erase/write cycle; In this case, there is no effect on the current program/erase/write cycle that is in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The RES instruction ends when CS# goes high, after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 15. Read Electronic Signature (RES) Sequence (SPI Mode)

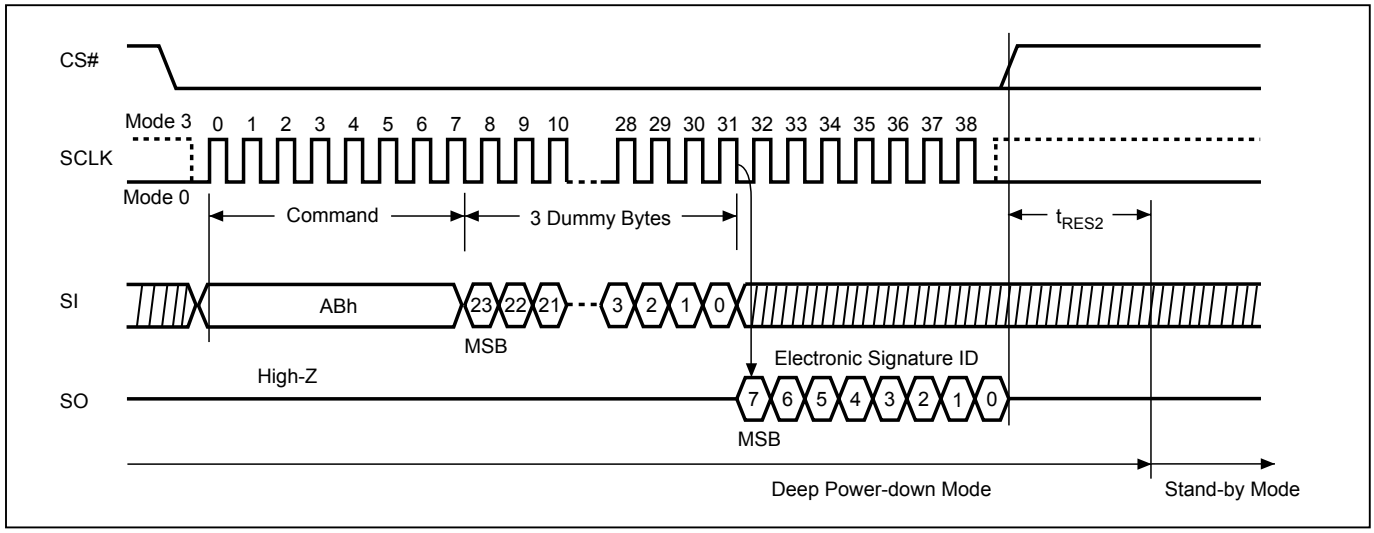


Figure 16. Read Electronic Signature (RES) Sequence (QPI Mode)

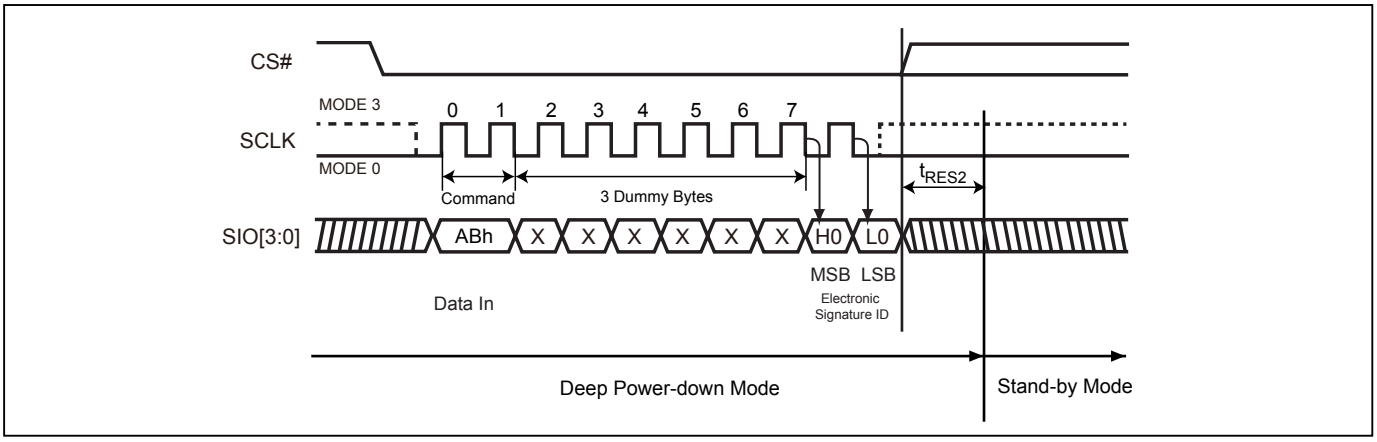


Figure 17. Release from Deep Power-down (RDP) Sequence (SPI Mode)

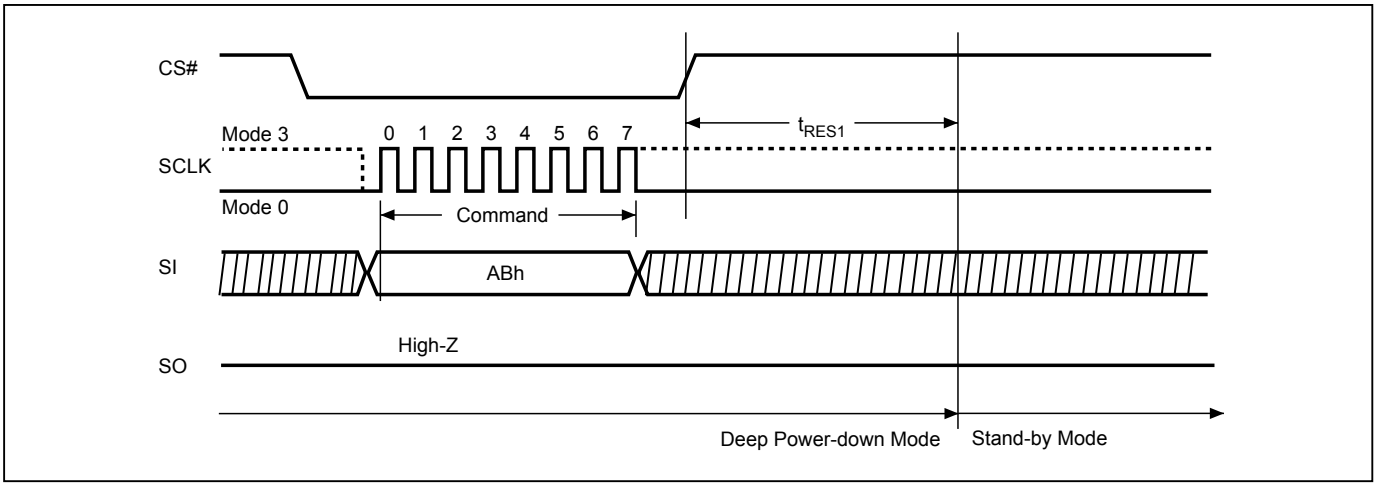
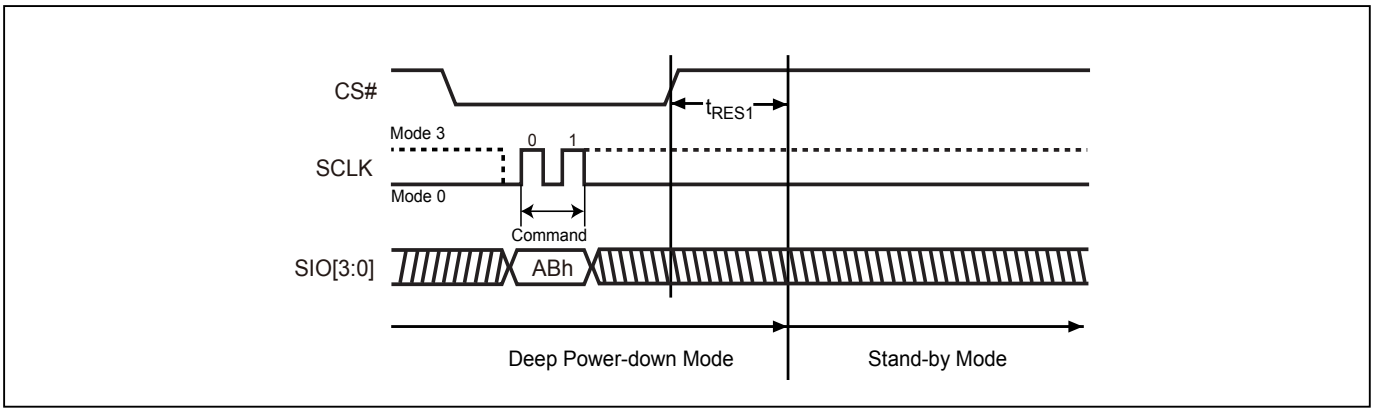


Figure 18. Release from Deep Power-down (RDP) Sequence (QPI Mode)

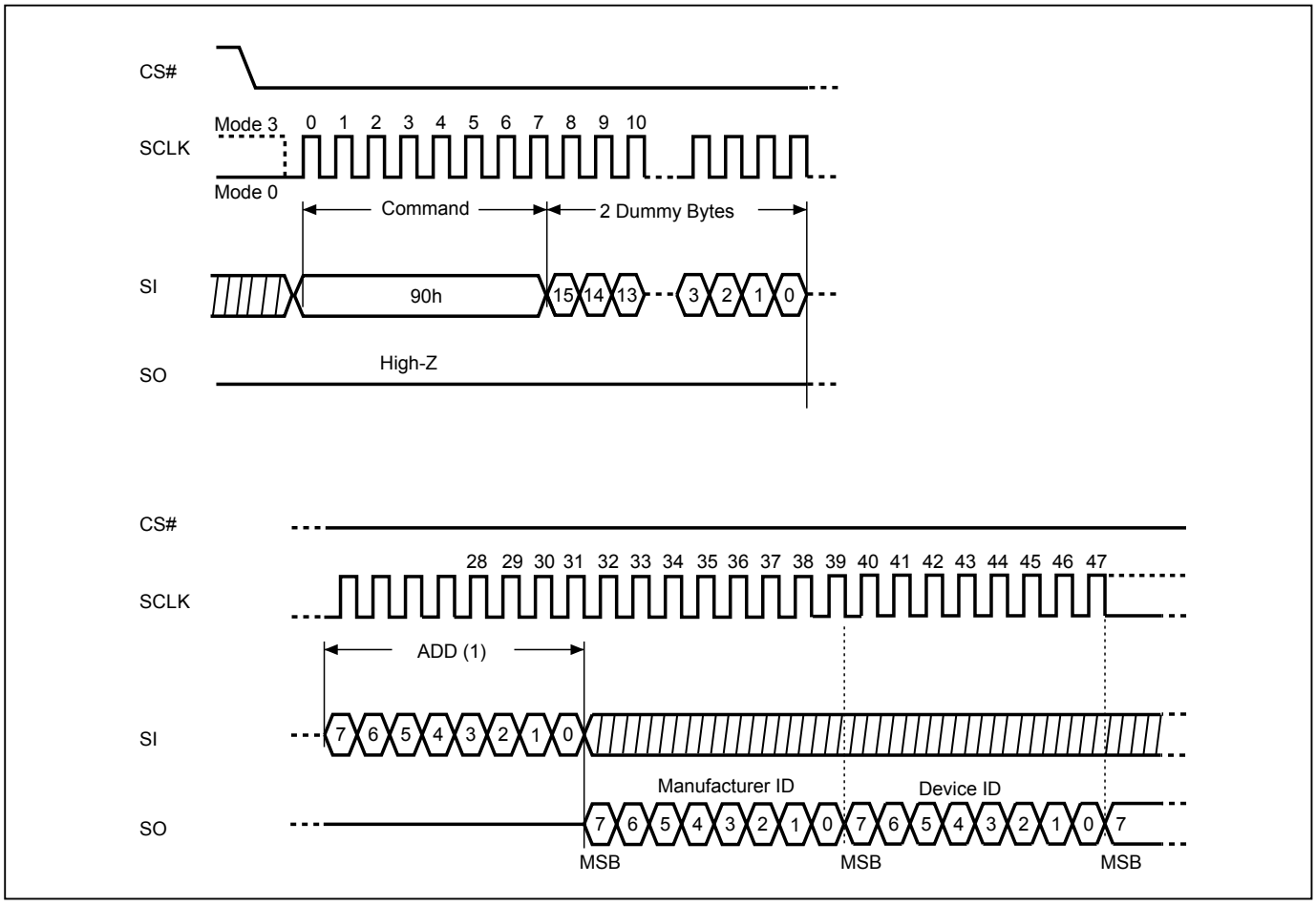


9-6. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 6. ID Definitions"*.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 19. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes: (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

9-7. QPI ID Read (QPIID)

The QPIID Read instruction can be used to identify the Device ID and Manufacturer ID. The sequence of issuing the QPIID instruction is as follows: CS# goes low→send QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and memory density data byte will be output continuously, until the CS# goes high.

Table 6. ID Definitions

Command Type		MX25U12873G		
RDID	9Fh	Manufacturer ID	Memory Type	Memory Density
		C2	25	38
RES	ABh	Electronic Signature ID		
		38		
REMS	90h	Manufacturer ID	Device ID	
		C2	38	
QPIID	AFh	Manufacturer ID	Memory Type	Memory Density
		C2	25	38

9-8. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ send RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 20. Read Status Register (RDSR) Sequence (SPI Mode)

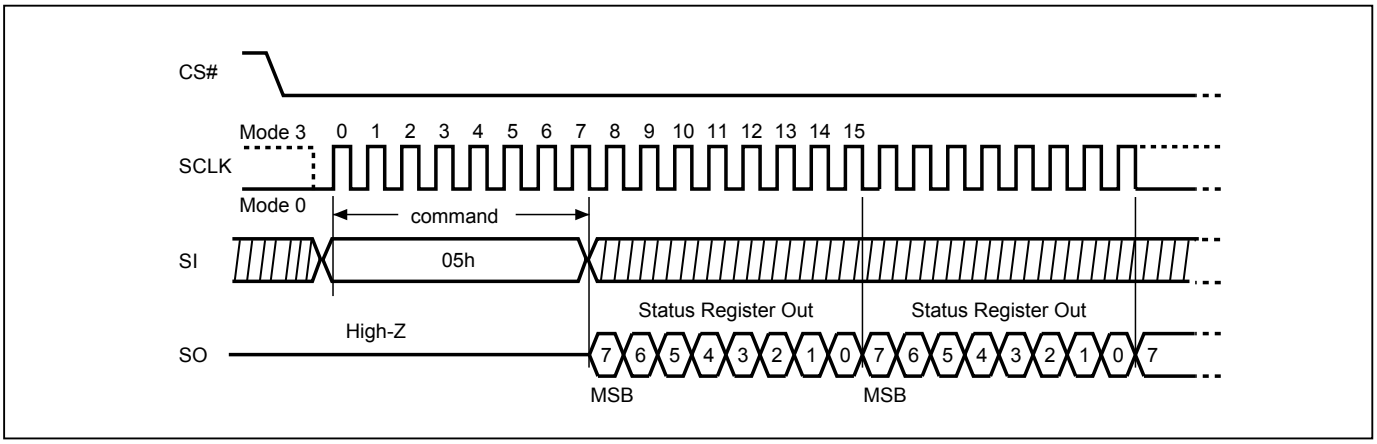
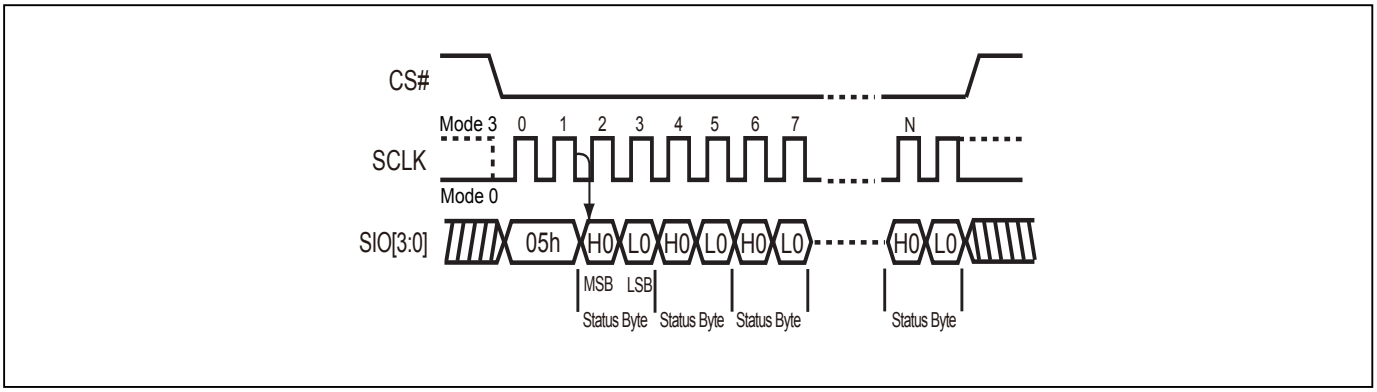


Figure 21. Read Status Register (RDSR) Sequence (QPI Mode)



9-9. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ send RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 22. Read Configuration Register (RDCR) Sequence (SPI Mode)

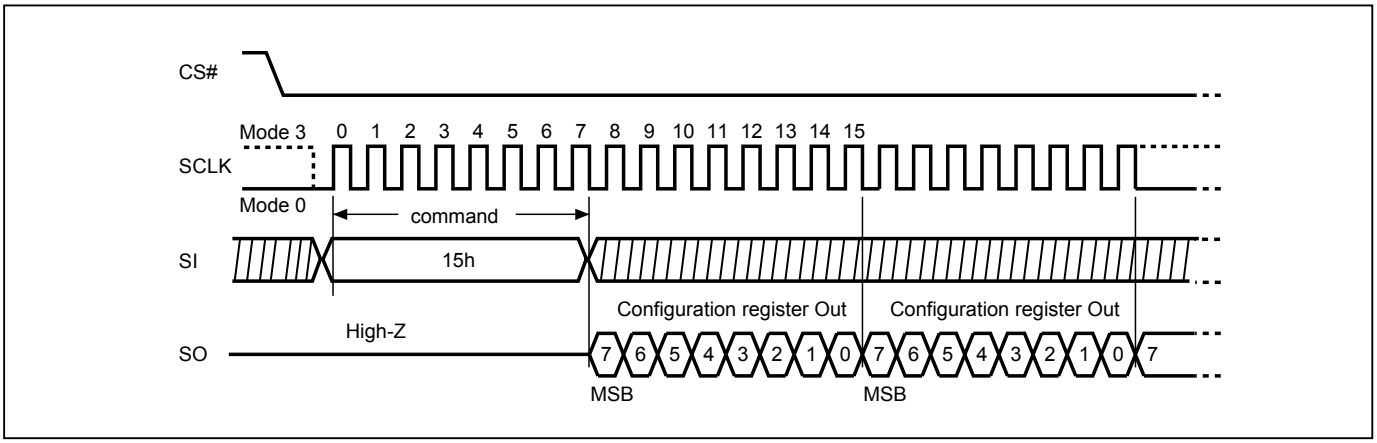
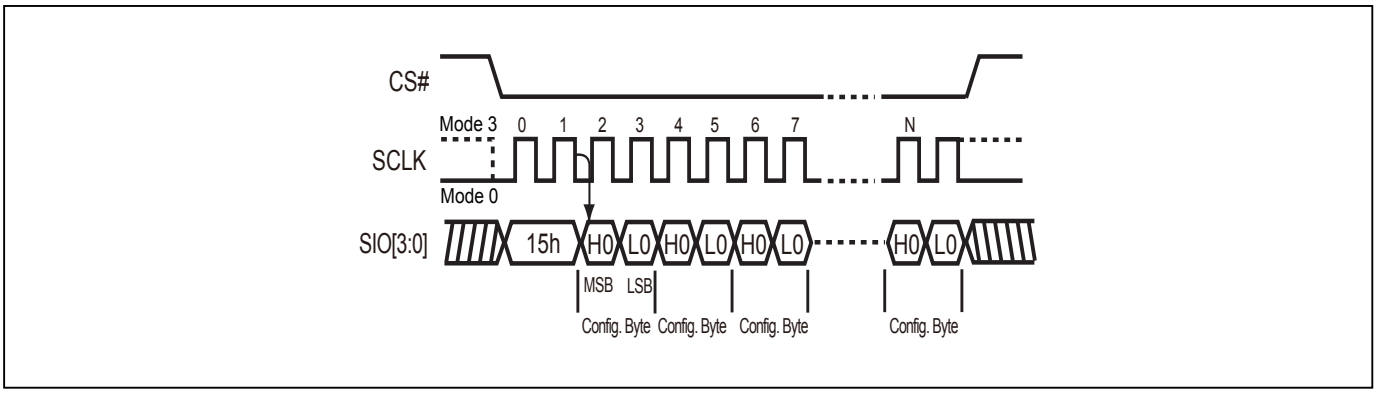


Figure 23. Read Configuration Register (RDCR) Sequence (QPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 24. Program/Erase flow with read array data

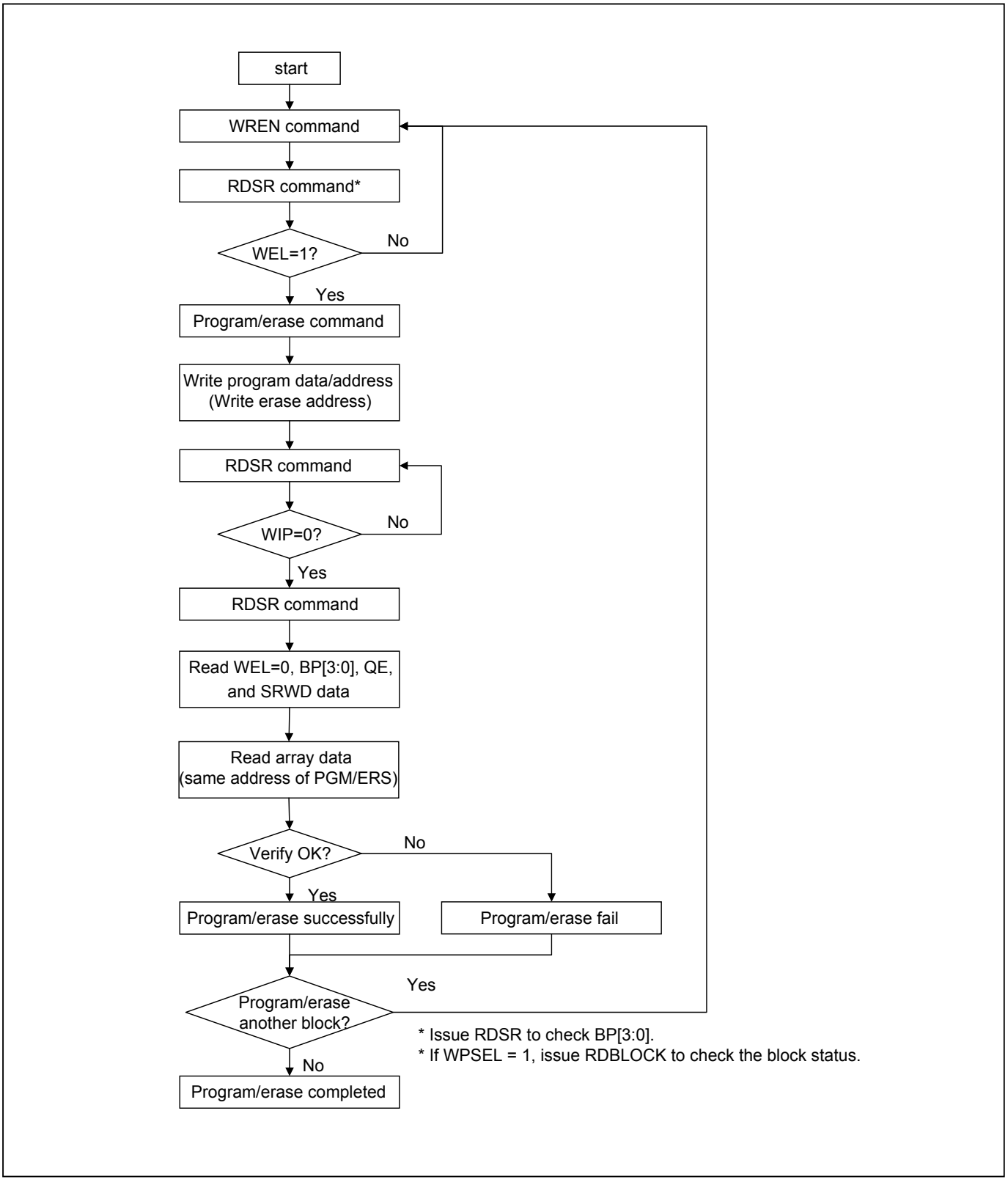
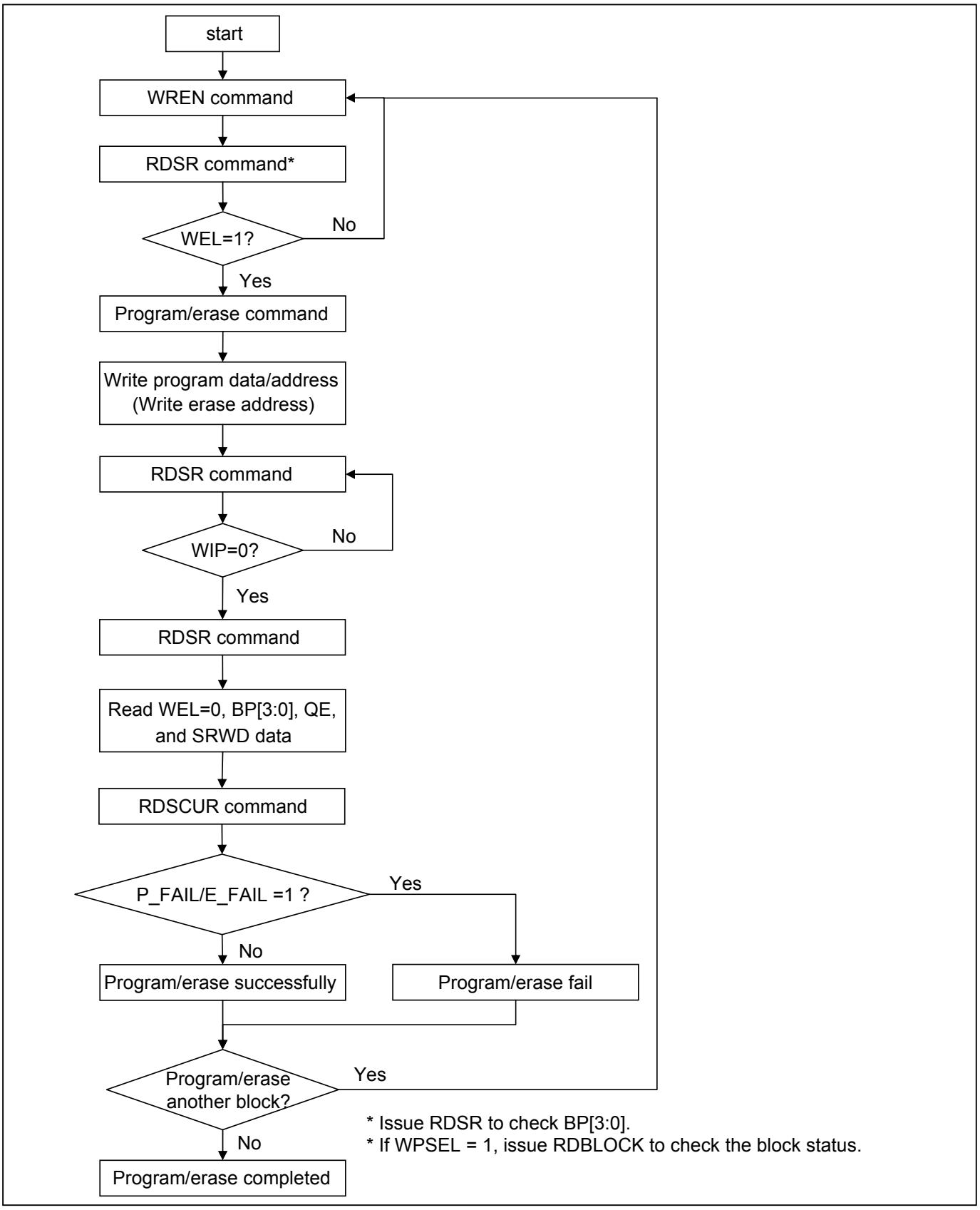


Figure 25. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to “1” by the WREN instruction. WEL needs to be set to “1” before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to “0” when a program or erase operation completes. To ensure that both WIP and WEL are “0” and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be “0” before checking that WEL is also “0”. If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to “0”.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit is permanently set to "1". When QE is "1", Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands.

Table 7. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	QE (Quad Enabled)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
Reserved	1=Quad Enabled	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enabled 0=not write enabled	1=write operation 0=not in write operation
Reserved	Fixed value	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to *"Table 2. Protected Area Sizes"*.

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *"Table 9. Output Driver Strength Table"*) of the device. The Output Driver Strength is defaulted as 30 Ohms when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit
The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. The PBE bit is defaulted as "0", which means preamble bit is disabled. When it is set as "1", the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed.

Table 8. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DC1 (Dummy cycle 1)	DC0 (Dummy cycle 0)	Reserved	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
(Note 2)	*(Note 2)*	x	0=Disabled 1=Enabled	0=Top area protect 1=Bottom area protect (Default=0)	*(Note 1)*	*(Note 1)*	*(Note 1)*
volatile bit	volatile bit	x	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: Please refer to *"Table 9. Output Driver Strength Table"*
Note 2: Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"*

Table 9. Output Driver Strength Table

ODS2	ODS1	ODS0	Resistance (Ohm)	Note
0	0	0	Reserved	Impedance at VCC/2
0	0	1	90 Ohms	
0	1	0	45 Ohms	
0	1	1	45 Ohms	
1	0	0	Reserved	
1	0	1	15 Ohms	
1	1	0	15 Ohms	
1	1	1	30 Ohms (Default)	

Table 10. Dummy Cycle and Frequency Table (MHz)

(STR Mode)

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Dual Output Fast Read	Quad Output Fast Read
Don't care 00 (default)	8	133	133	133

DC[1:0]	Numbers of Dummy clock cycles	Dual IO Fast Read
00 (default)	4	84
01	8	133
10	4	84
11	8	133

DC[1:0]	Numbers of Dummy clock cycles	FAST READ(QPI)
Don't care 00 (default)	4	66

DC[1:0]	Numbers of Dummy clock cycles	Quad IO Fast Read	Quad IO Fast Read (QPI)
00 (default)	6	84	84
01	4	66	66
10	8	104	104
11	10	133	133

(DTR Mode)

DC[1:0]	Numbers of Dummy clock cycles	Quad IO DTR Read
00 (default)	6	54
01	6	54
10	8	66
11	10	84

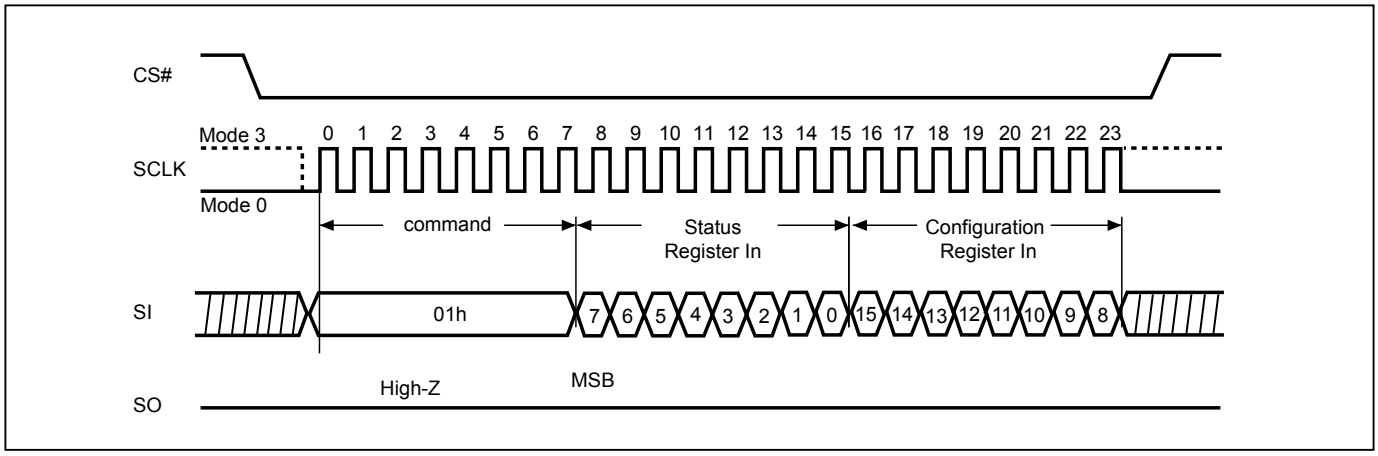
9-10. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*).

The sequence of issuing WRSR instruction is: CS# goes low→ send WRSR instruction code→ Status Register data on SI→Configuration Register data on SI→CS# goes high.

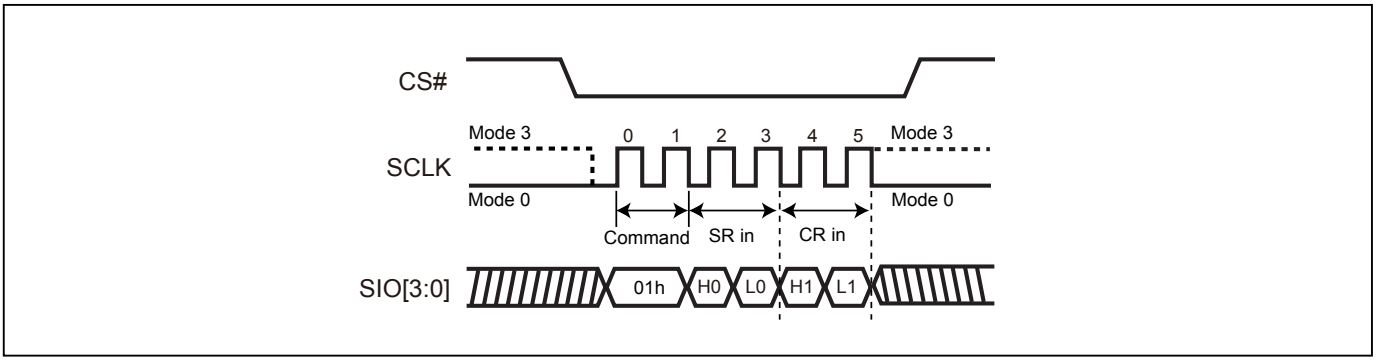
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 26. Write Status Register (WRSR) Sequence (SPI Mode)



Note: The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 27. Write Status Register (WRSR) Sequence (QPI Mode)



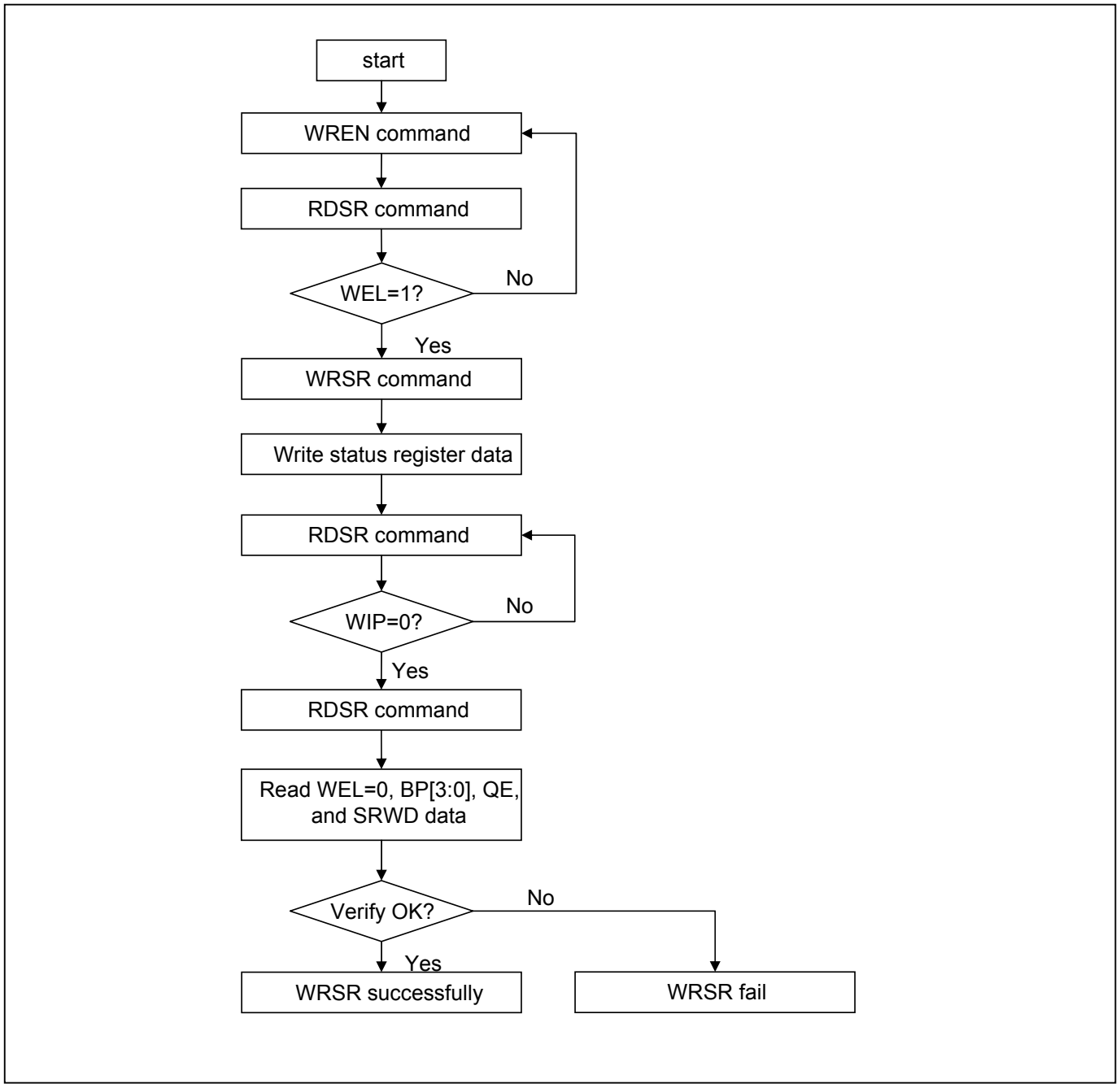
Software Protected Mode (SPM):
The WREN instruction may set the WEL bit and can change the values of BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Table 11. Protection Modes

Mode	Status register condition	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the BP0-BP3 bits can be changed.	The protected area cannot be programmed or erased.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

Figure 28. WRSR flow



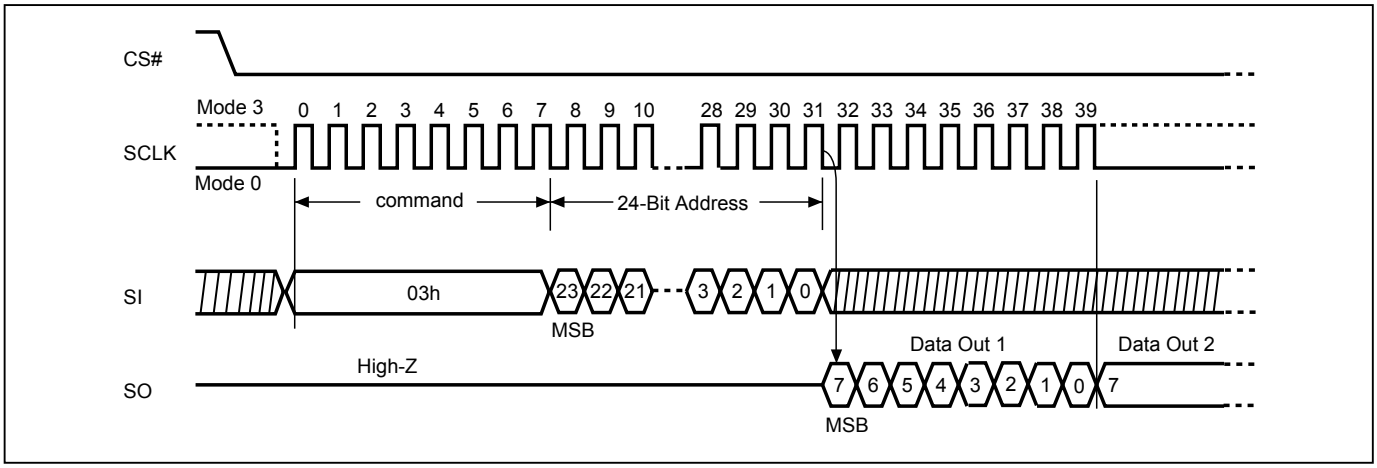
9-11. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→send READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 29. Read Data Bytes (READ) Sequence (SPI Mode only)



9-12. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ send FAST_READ instruction code→ 3-byte address on SI→ 8 dummy cycles → data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

Read on QPI Mode The sequence of issuing FAST_READ instruction in QPI mode is: CS# goes low→ send FAST_READ instruction, 2 cycles→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→4 dummy cycles →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QPI FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 30. Read at Higher Speed (FAST_READ) Sequence (SPI Mode)

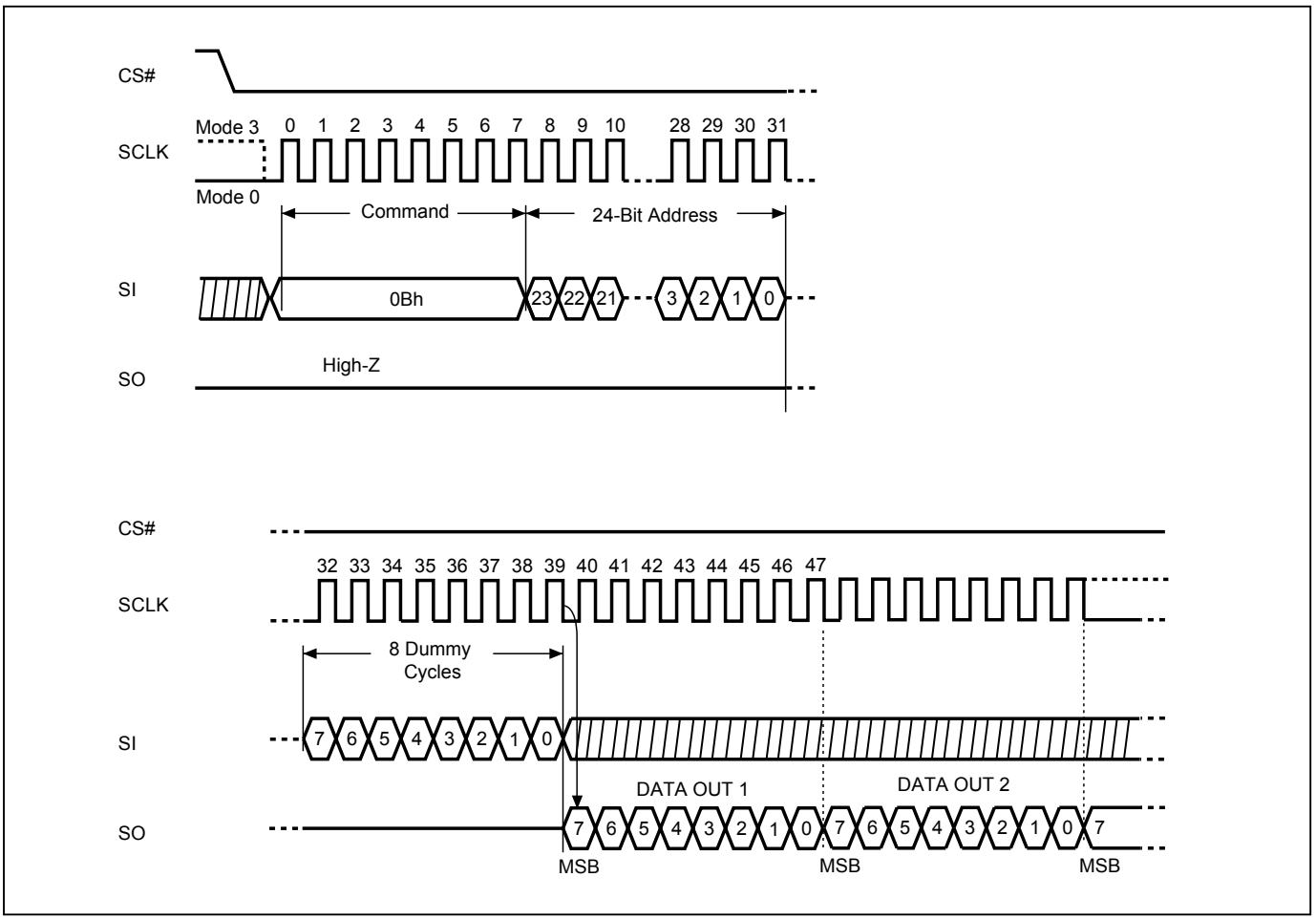
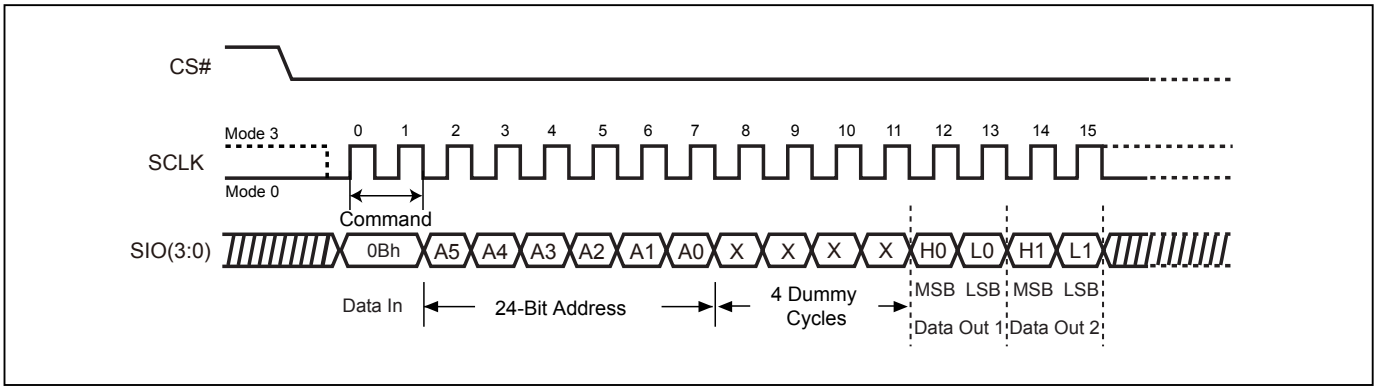


Figure 31. Read at Higher Speed (FAST_READ) Sequence (QPI Mode)



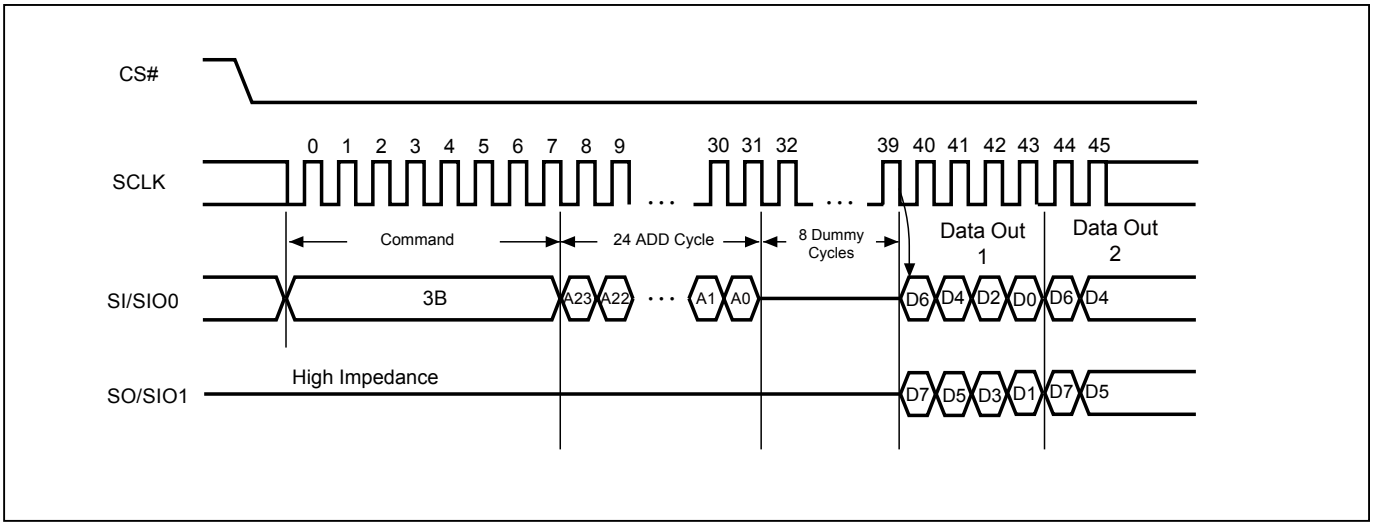
9-13. Dual Output Read Mode (DREAD)

The DREAD instruction enables double throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low→ send DREAD instruction→3-byte address on SIO0→ 8 dummy cycles on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation, use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 32. Dual Read Mode Sequence (SPI Mode only)



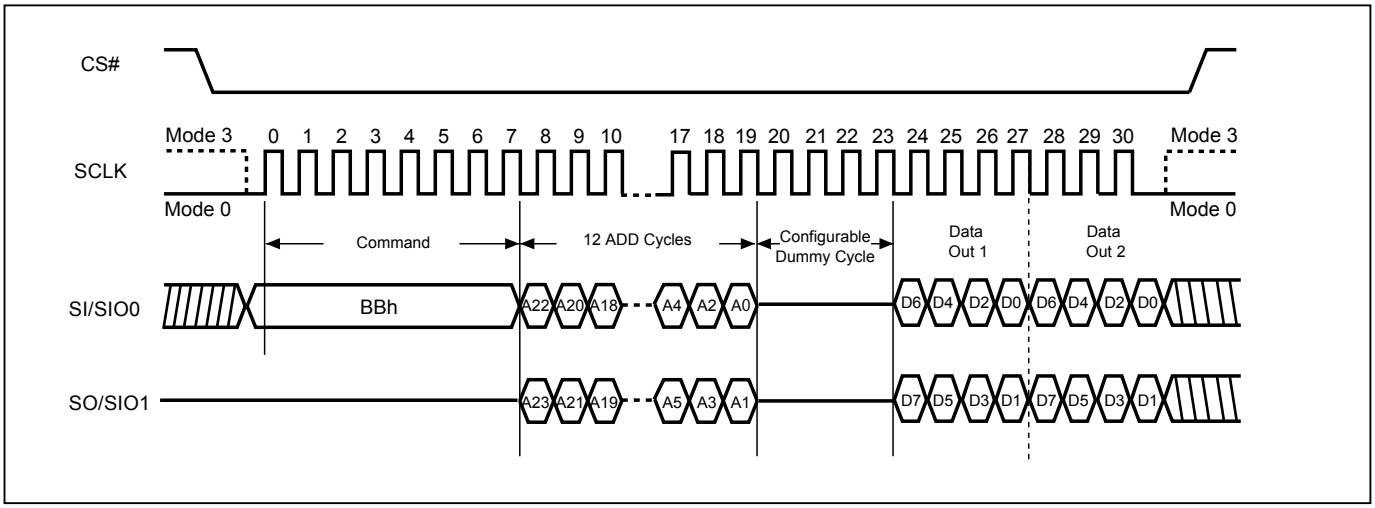
9-14. 2 x I/O Read Mode (2READ)

The 2READ instruction enables double throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ send 2READ instruction→ 3-byte address interleave on SIO1 & SIO0→ 4 dummy cycles (default) on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 33. 2 x I/O Read Mode Sequence (SPI Mode only)



Note: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

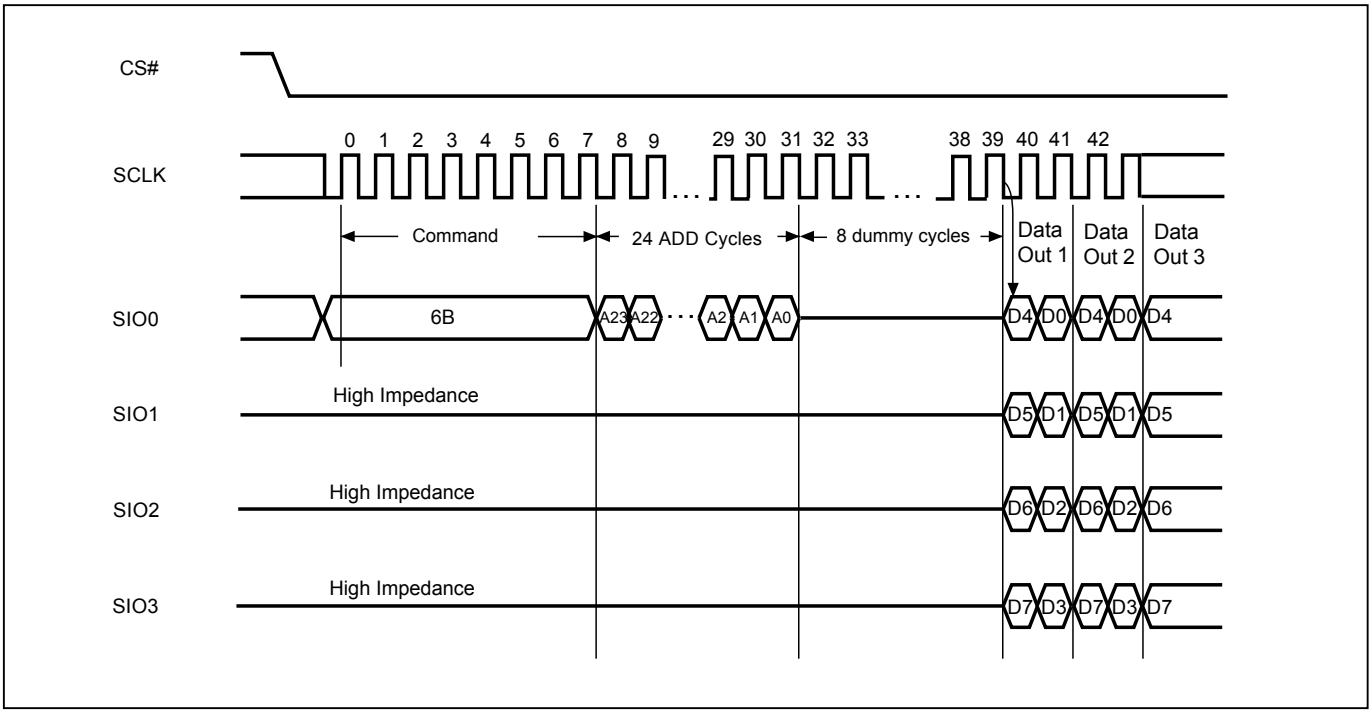
9-15. Quad Read Mode (QREAD)

The QREAD instruction enables quad throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ send QREAD instruction → 3-byte address on SI → 8 dummy cycles → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 34. Quad Read Mode Sequence (SPI Mode only)

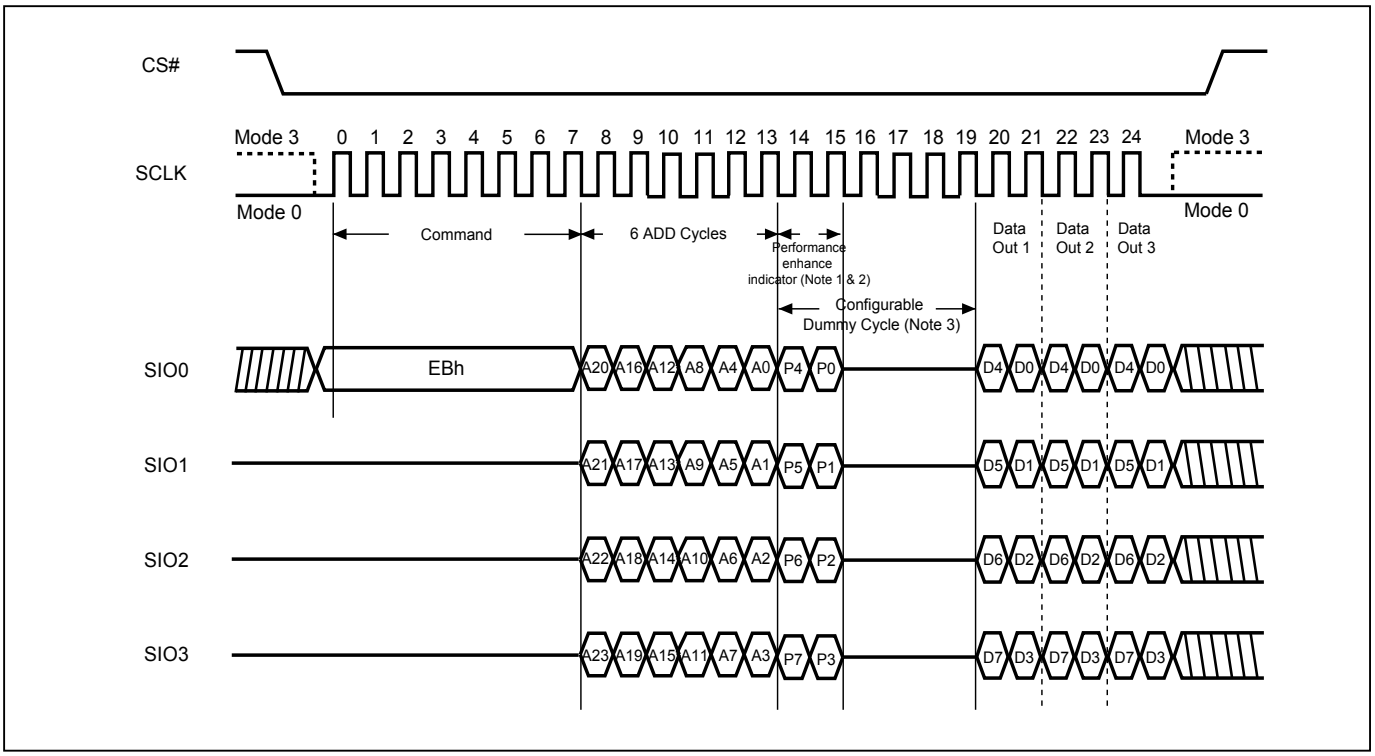


9-16. 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ send 4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation, drive CS# high at any time during data out.

Figure 35. 4 x I/O Read Mode Sequence (SPI Mode)

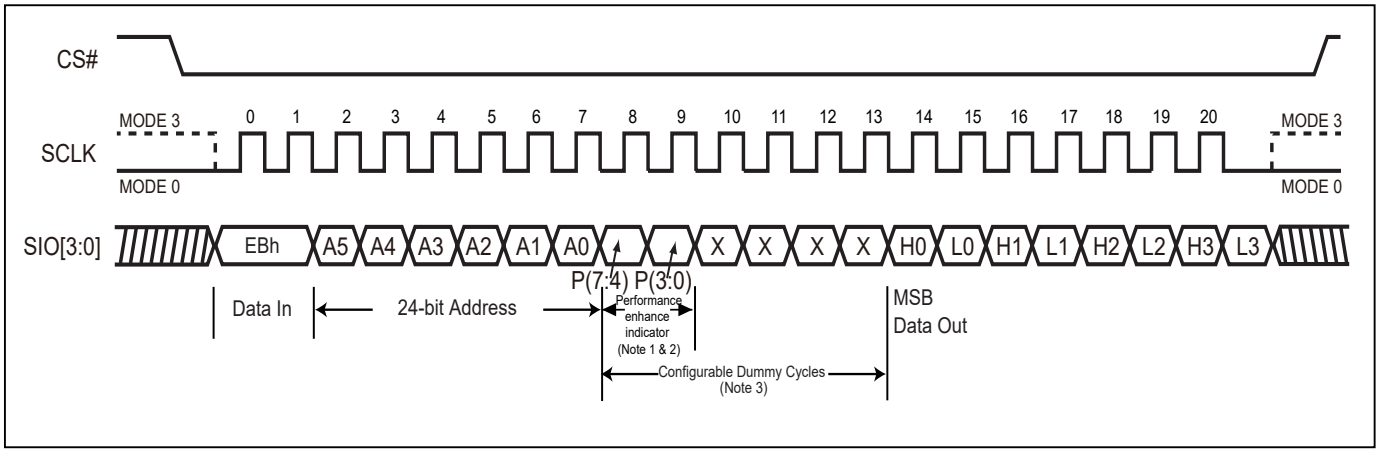


Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ send 4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation, drive CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 36. 4 x I/O Read Mode Sequence (QPI Mode)



Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

W4READ instruction (E7h) is also available for 4 I/O read. Please refer to *"Figure 37. W4READ (Quad Read with 4 dummy cycles) Sequence (SPI Mode)"* and *"Figure 38. W4READ (Quad Read with 4 dummy cycles) Sequence (QPI Mode)"*.

W4READ on SPI Mode

The sequence of issuing W4READ instruction is: CS# goes low→ send W4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 4 dummy cycles →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end W4READ operation, drive CS# high at any time during data out.

W4READ on QPI Mode

The W4READ instruction also supports QPI command mode. The sequence of issuing W4READ instruction QPI mode is: CS# goes low→send W4READ instruction→3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→4 dummy cycles →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end W4READ operation, drive CS# high at any time during data out.

Figure 37. W4READ (Quad Read with 4 dummy cycles) Sequence (SPI Mode)

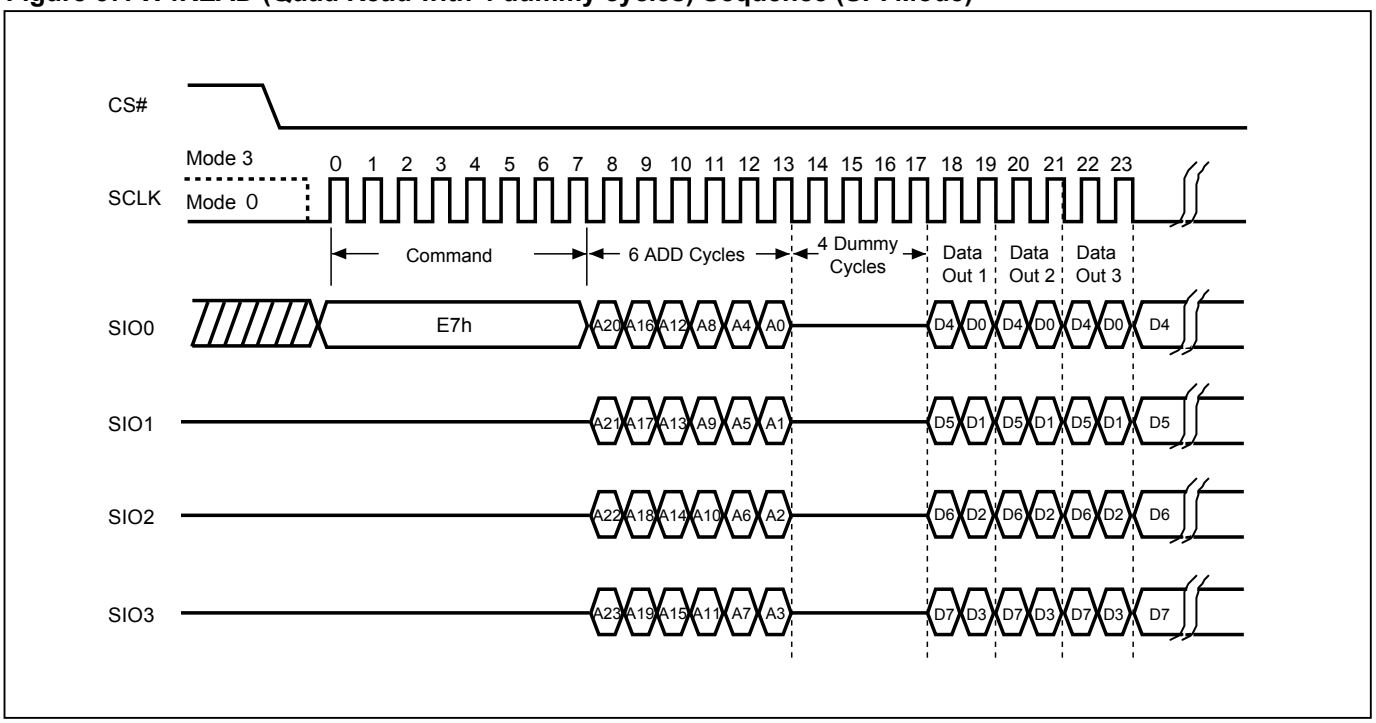
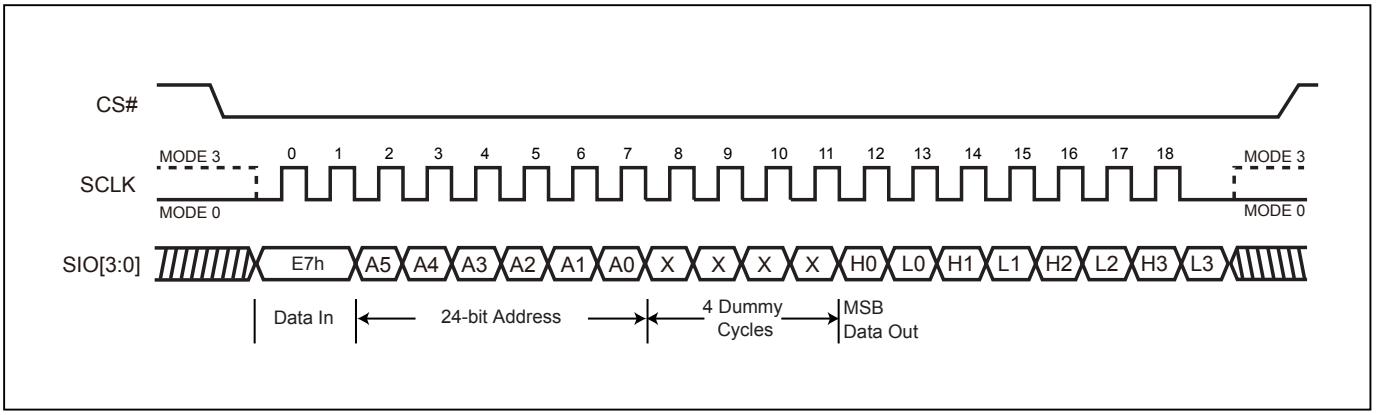


Figure 38. W4READ (Quad Read with 4 dummy cycles) Sequence (QPI Mode)



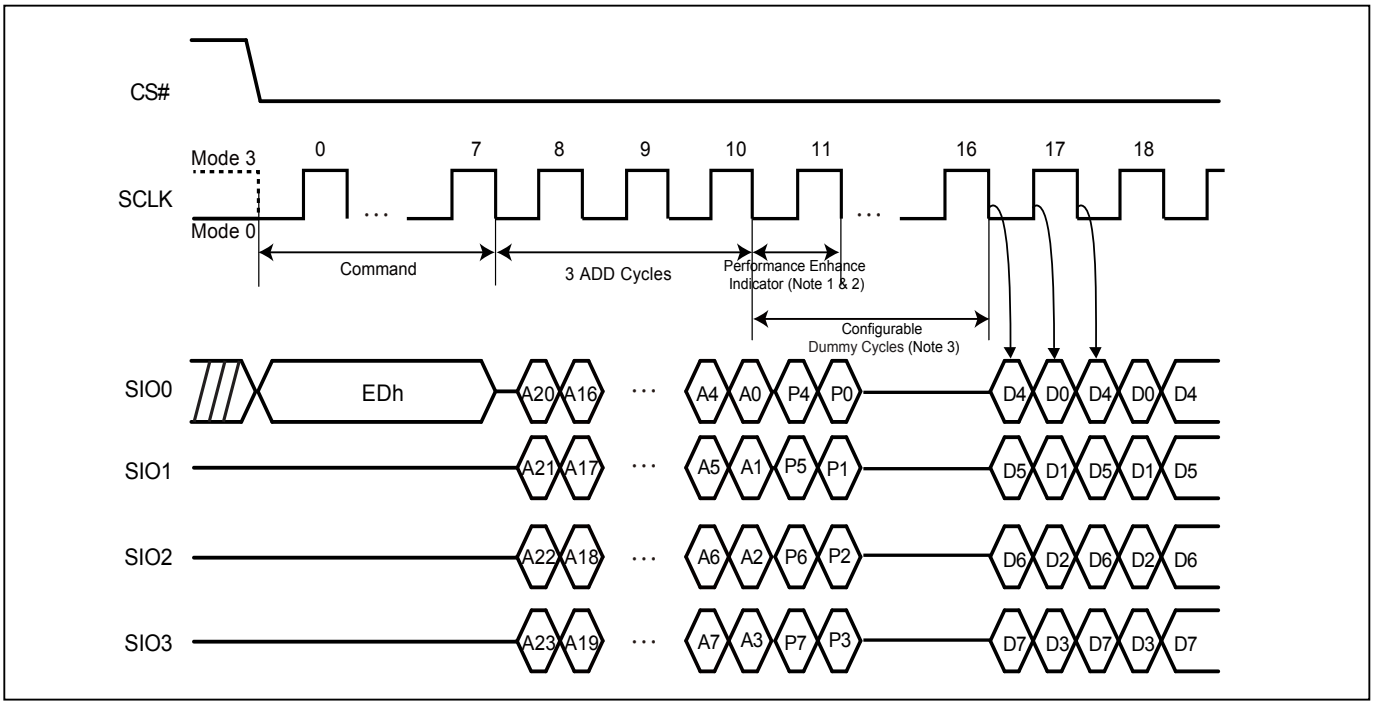
9-17. 4 x I/O Double Transfer Rate Read Mode (4DTRD)

The 4DTRD instruction enables Double Transfer Rate throughput on quad I/O of the Serial NOR Flash in read mode. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4DTRD instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

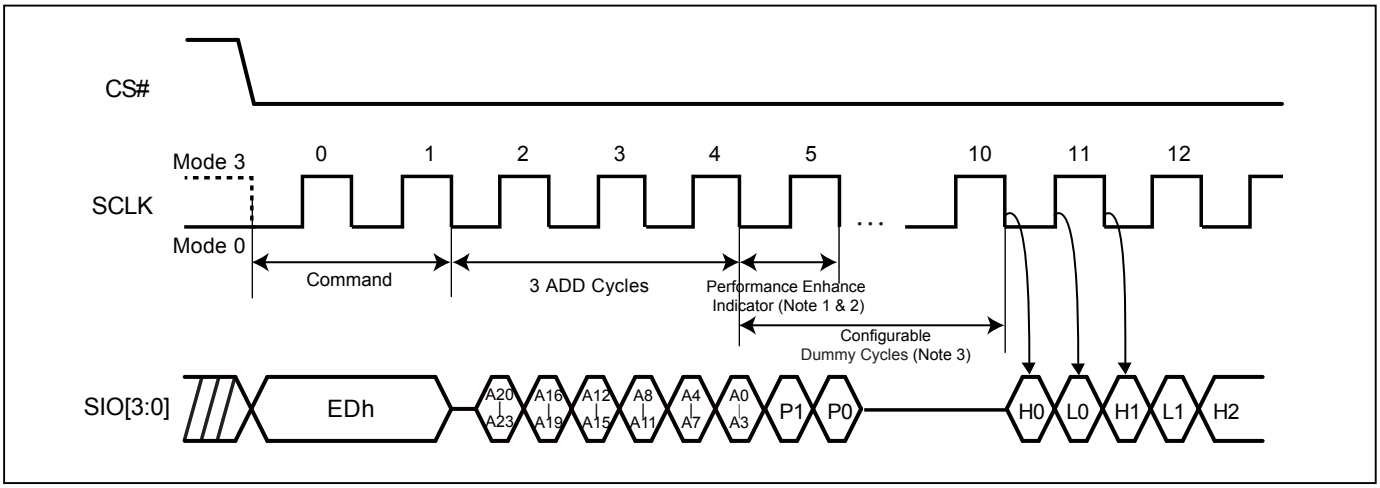
While Program/Erase/Write Status Register cycle is in progress, 4DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 39. Fast Quad I/O DT Read (4DTRD) Sequence (SPI Mode)



Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 40. Fast Quad I/O DT Read (4DTRD) Sequence (QPI Mode)



Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

9-18. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine valid window of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

Preamble Bit data pattern can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once the CR<4> is set, the preamble bit is inputted into dummy cycles.

Enabling preamble bit will not affect the function of enhance mode bit. In Dummy cycles, performance enhance mode bit still operates with the same function. Preamble bit will output after performance enhance mode bit.

The preamble bit is a fixed 8-bit data pattern (00110100). While dummy cycle number reaches 10, the complete 8 bits will start to output right after the performance enhance mode bit. While dummy cycle is not sufficient of 10 cycles, the rest of the preamble bits will be cut. For example, 8 dummy cycles will cause 6 preamble bits to output, and 6 dummy cycles will cause 4 preamble bits to output.

Figure 41. SDR 1I/O (10DC)

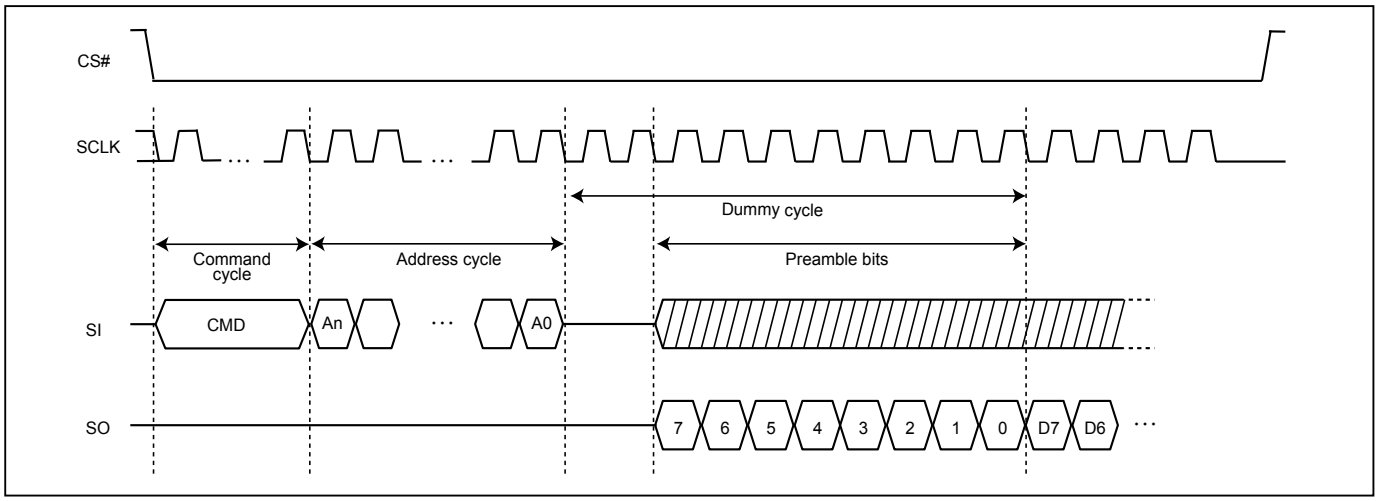


Figure 42. SDR 1I/O (8DC)

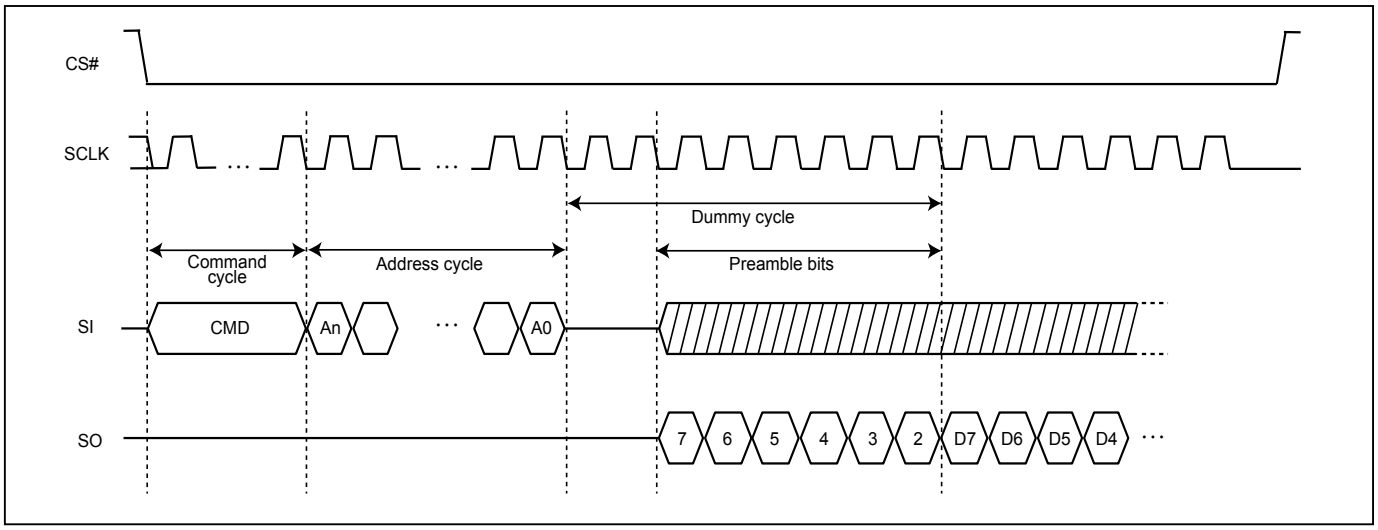


Figure 43. SDR 2I/O (10DC)

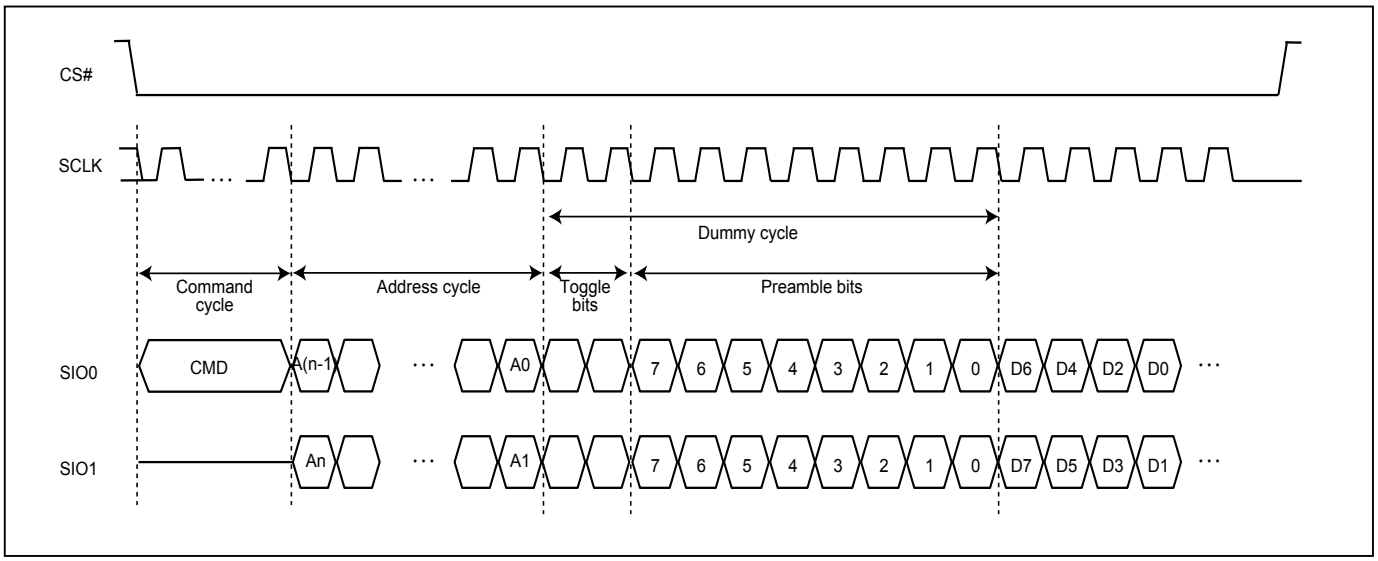


Figure 44. SDR 2I/O (8DC)

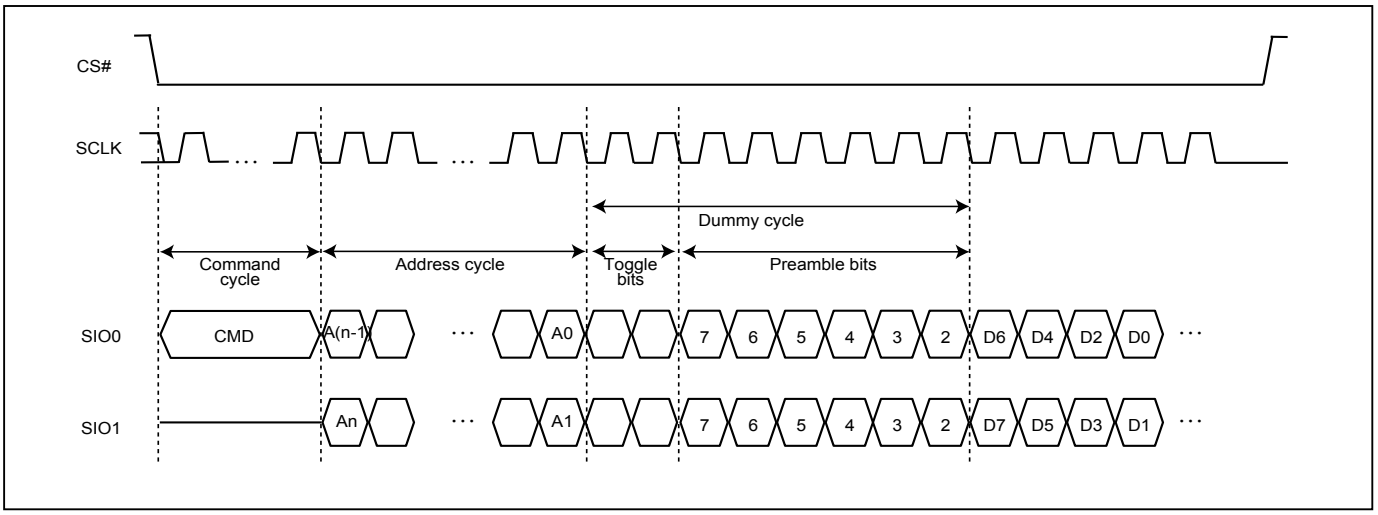


Figure 45. SDR 4I/O (10DC)

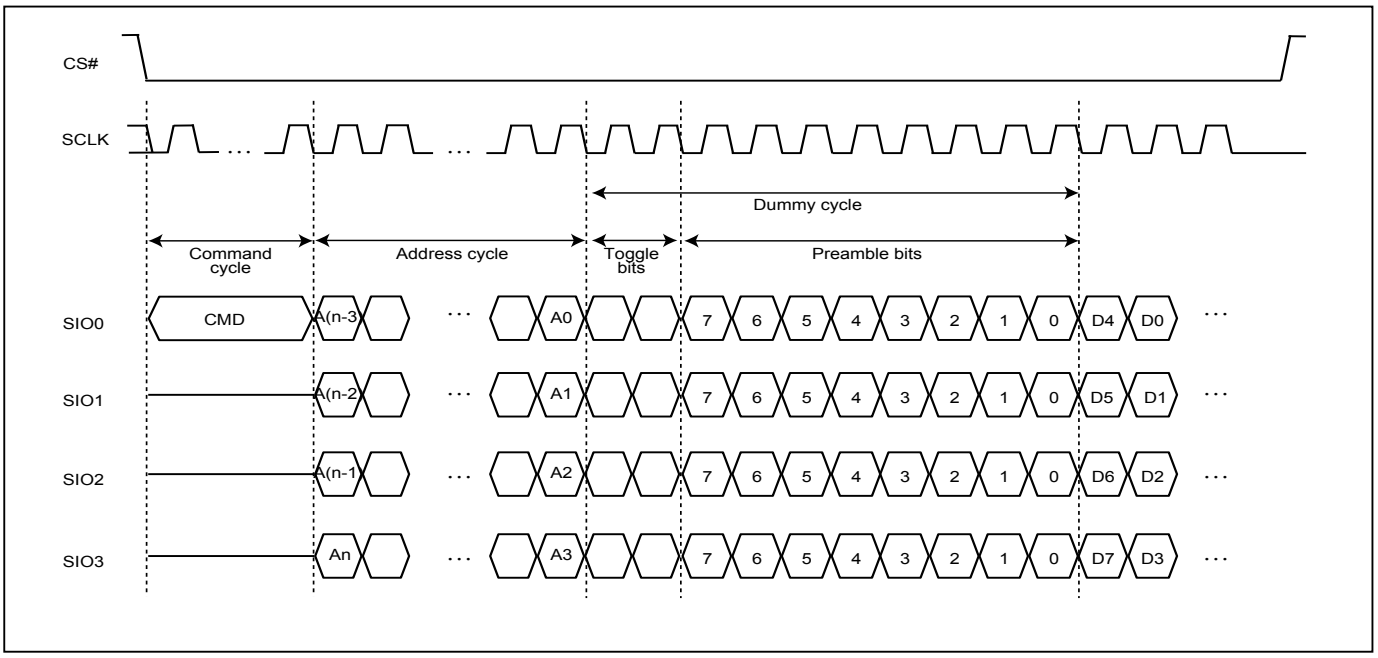


Figure 46. SDR 4I/O (8DC)

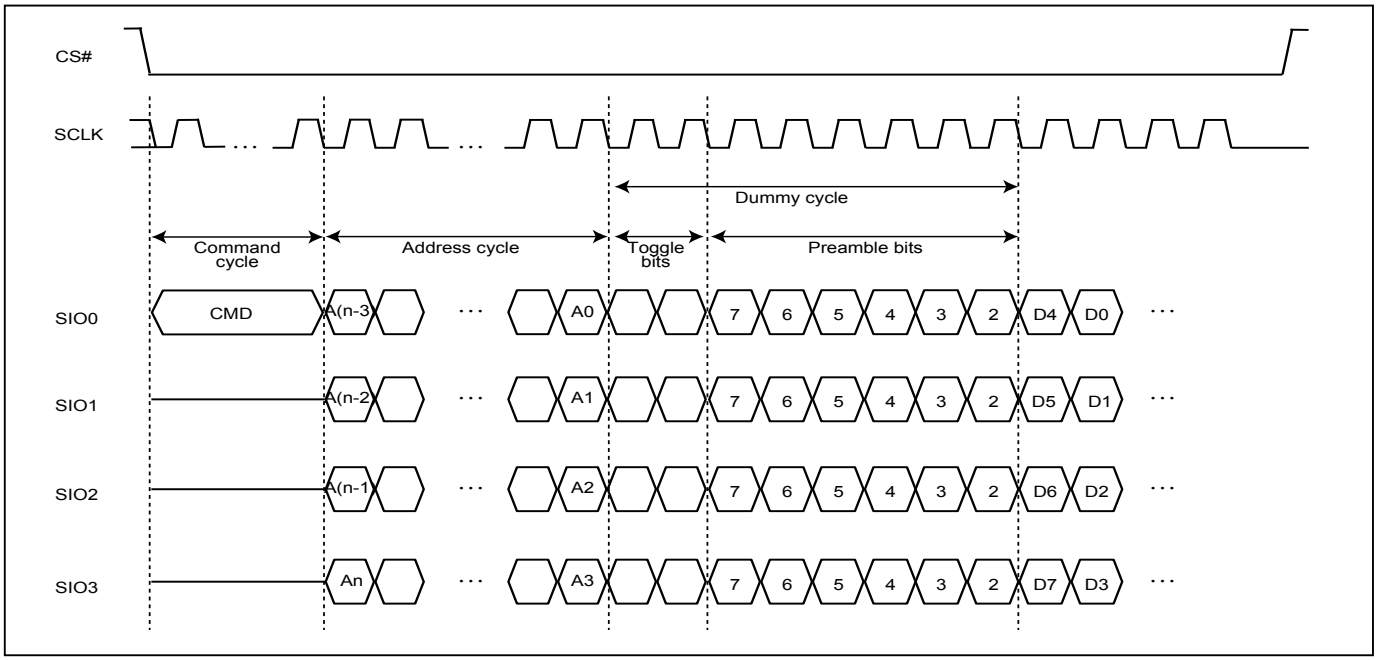
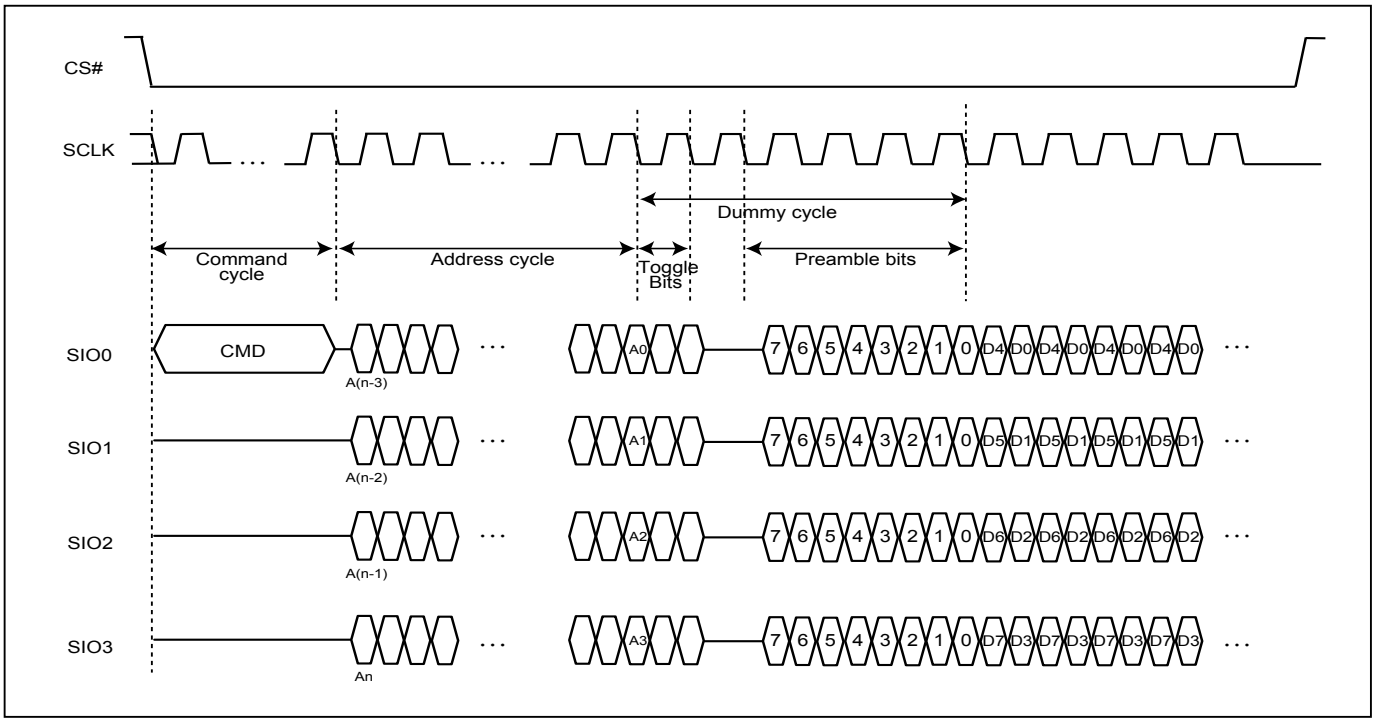


Figure 47. DTR4IO (6DC)



9-19. Burst Read

The Burst Read feature allows applications to fill a cache line with a fixed length of data without using multiple read commands. Burst Read is disabled by default at power-up or reset. Burst Read is enabled by setting the Burst Length. When the Burst Length is set, reads will wrap on the selected boundary (8/16/32/64-bytes) containing the initial target address. For example if an 8-byte Wrap Depth is selected, reads will wrap on the 8-byte-page-aligned boundary containing the initial read address.

To set the Burst Length, drive CS# low → send SET BURST LENGTH instruction code (C0h) → send WRAP CODE →drive CS# high. Refer to the table below for valid 8-bit Wrap Codes and their corresponding Wrap Depth.

Data	Wrap Around	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

Once Burst Read is enabled, it will remain enabled until the device is power-cycled or reset. The SPI and QPI mode 4READ read commands support the wrap around feature after Burst Read is enabled. To change the wrap depth, resend the Burst Read instruction with the appropriate Wrap Code. To disable Burst Read, send the Burst Read instruction with Wrap Code 1xh. QPI “0Bh” “EBh” “E7h” and SPI “EBh” “E7h” support wrap around feature after wrap around is enabled. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 48. Burst Read (SPI Mode)

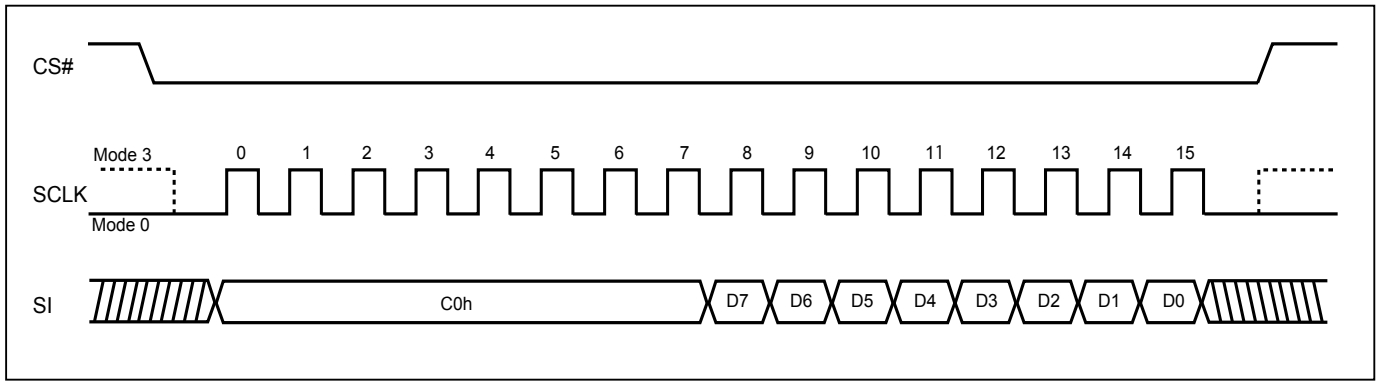
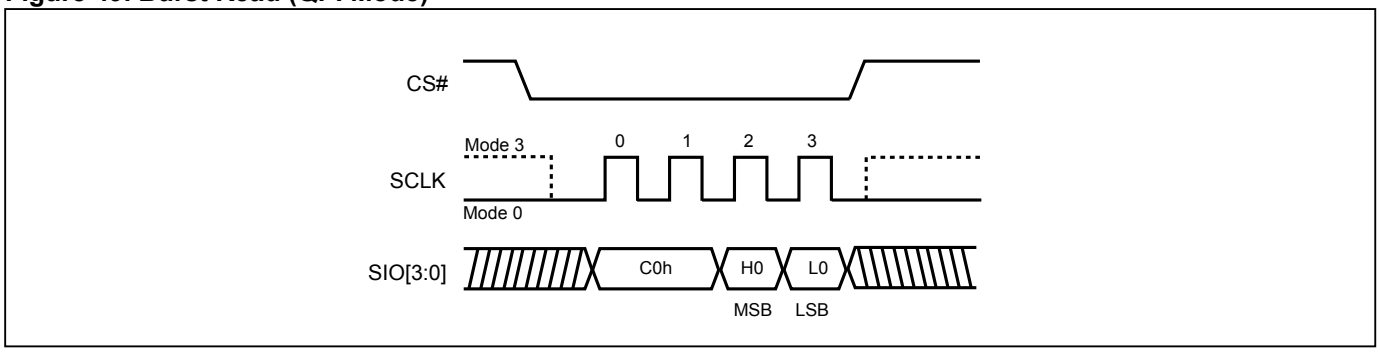


Figure 49. Burst Read (QPI Mode)



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

9-20. Performance Enhance Mode - XIP (execute-in-place)

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

Performance enhance mode is supported in both SPI and QPI mode.

In QPI mode, "EBh" "EDh" and SPI “EBh” "EDh" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing ”FFh” data cycle can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

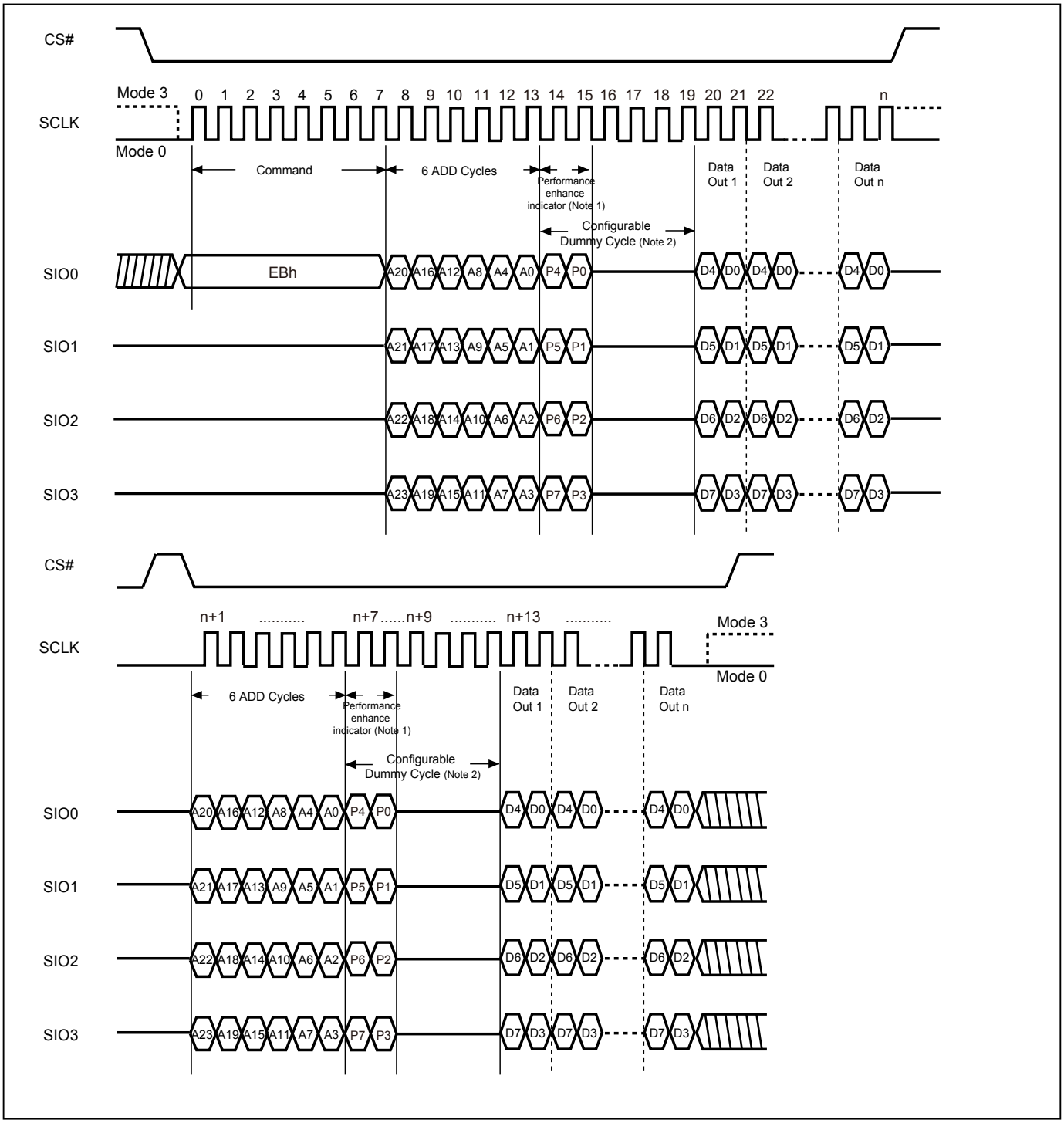
After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

This sequence of issuing 4READ instruction especially useful in random access: CS# goes low→send 4READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0→performance enhance toggling bit P[7:0]→ 4 dummy cycles (Default) →data out until CS# goes high → CS# goes low (The following 4READ instruction is not allowed, hence 8 cycles of 4READ can be saved comparing to normal 4READ mode) → 3-bytes random access address.

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh data should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh data cycle, in 4 I/O should be issued.

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

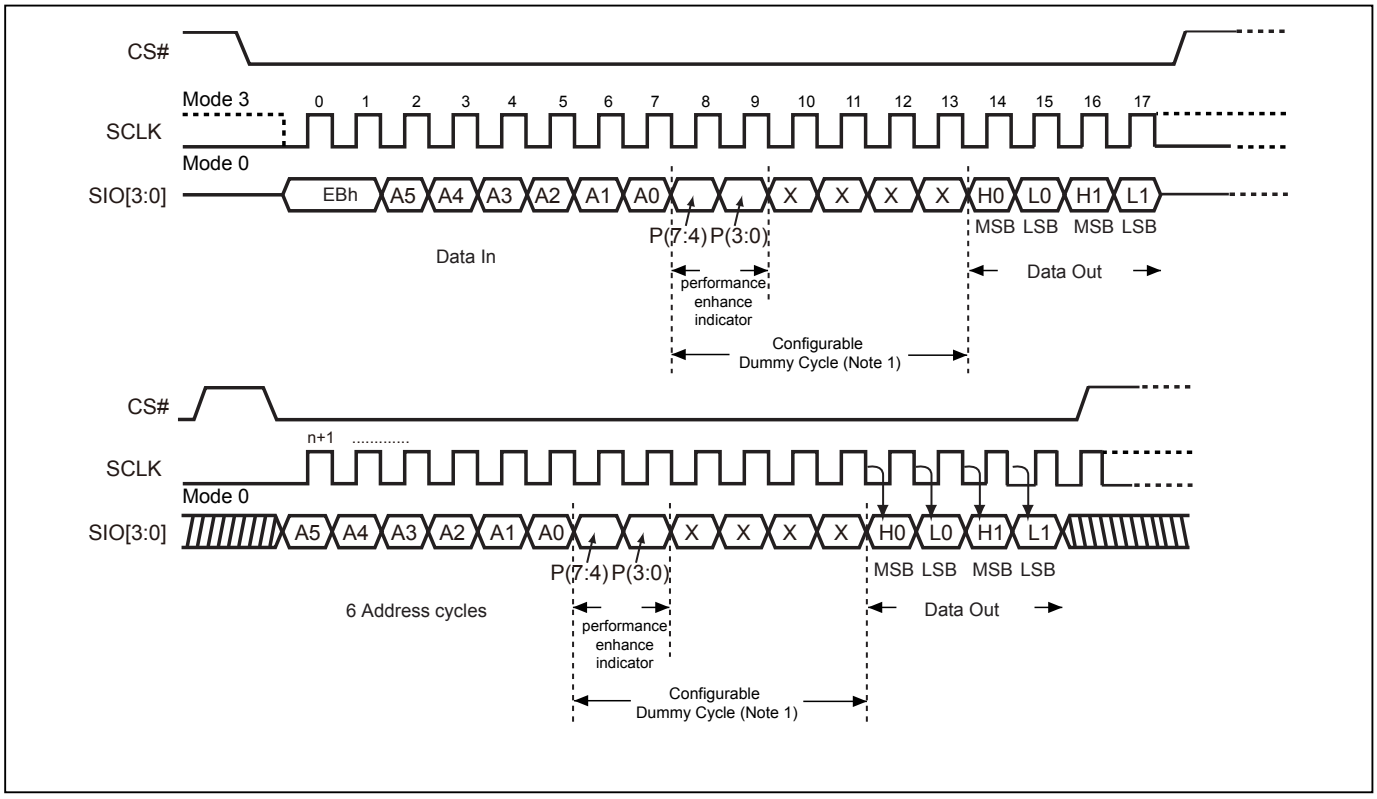
Figure 50. 4 x I/O Read Performance Enhance Mode Sequence (SPI Mode)



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Figure 51. 4 x I/O Read Performance Enhance Mode Sequence (QPI Mode)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
2. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.

9-21. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low→ send SE instruction code→ 3-byte on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 52. Sector Erase (SE) Sequence (SPI Mode)

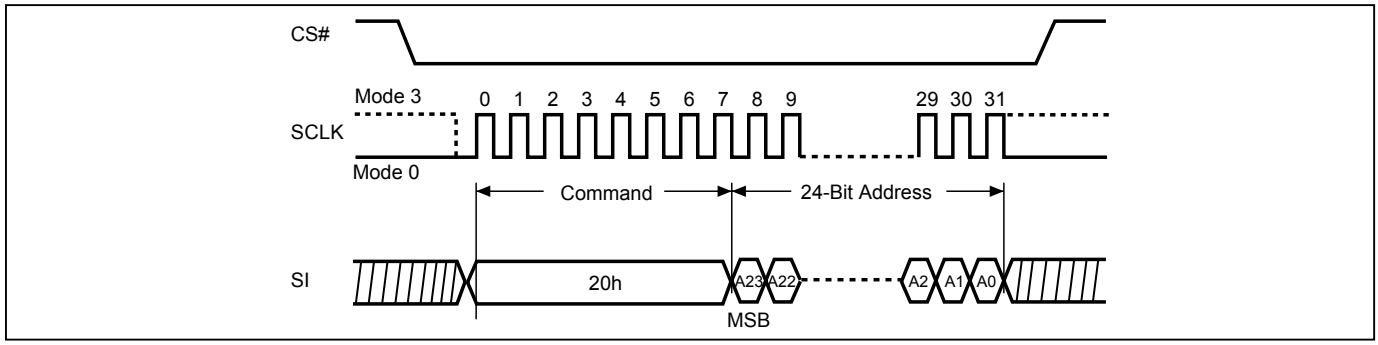
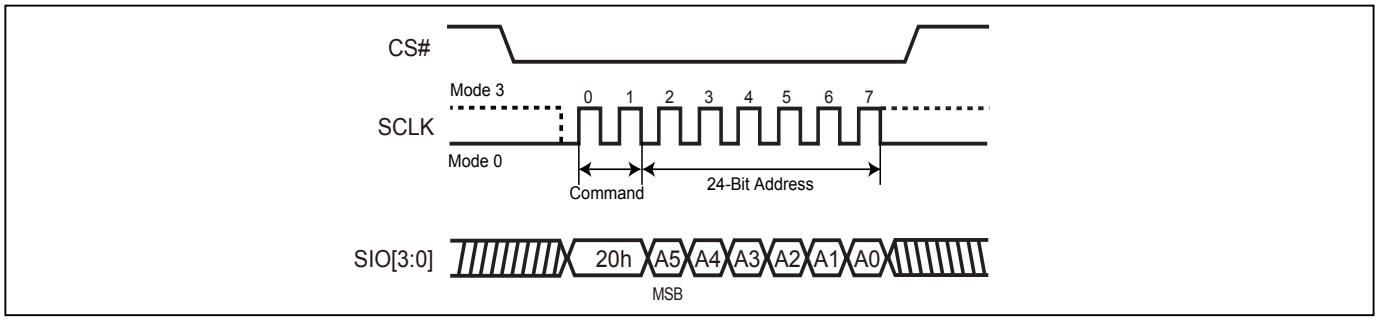


Figure 53. Sector Erase (SE) Sequence (QPI Mode)



9-22. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (as shown in *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A15] (Am is the most significant address) select the 32KB block address.

The sequence of issuing BE32K instruction is: CS# goes low→ send BE32K instruction code→ 3-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE32K) instruction will not be executed on the block.

Figure 54. Block Erase 32KB (BE32K) Sequence (SPI Mode)

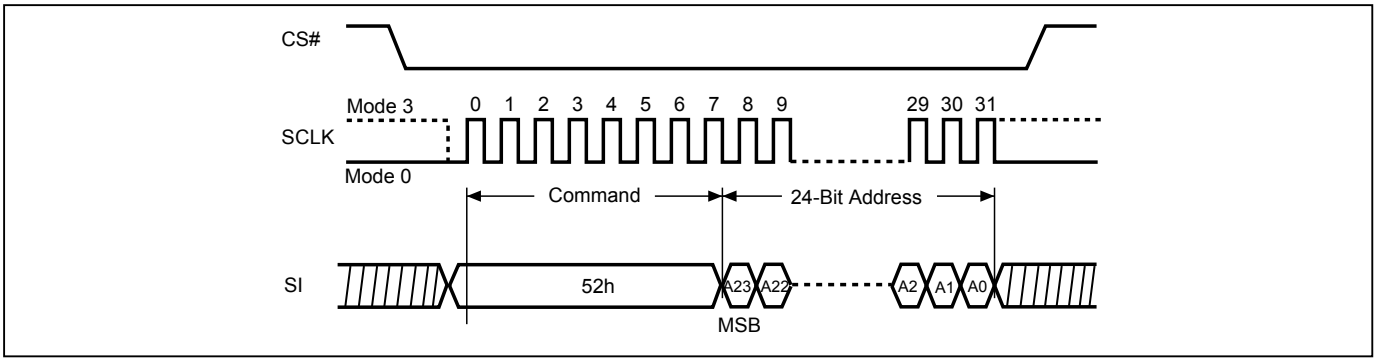
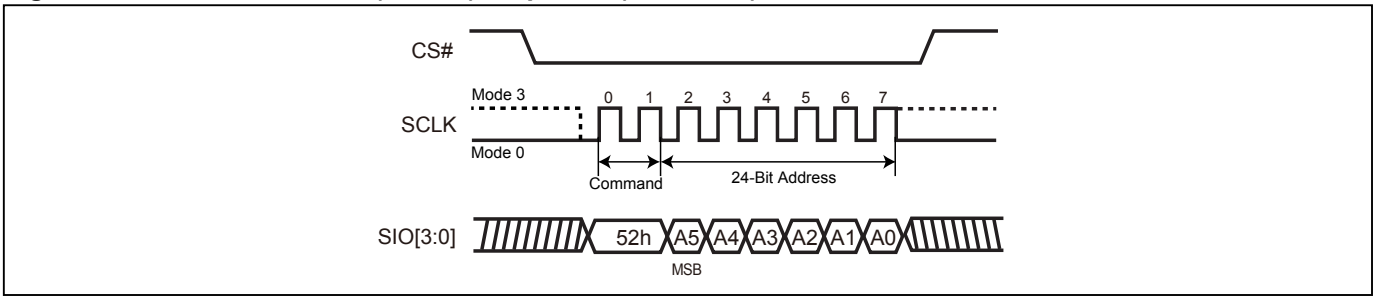


Figure 55. Block Erase 32KB (BE32K) Sequence (QPI Mode)



9-23. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ send BE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 56. Block Erase (BE) Sequence (SPI Mode)

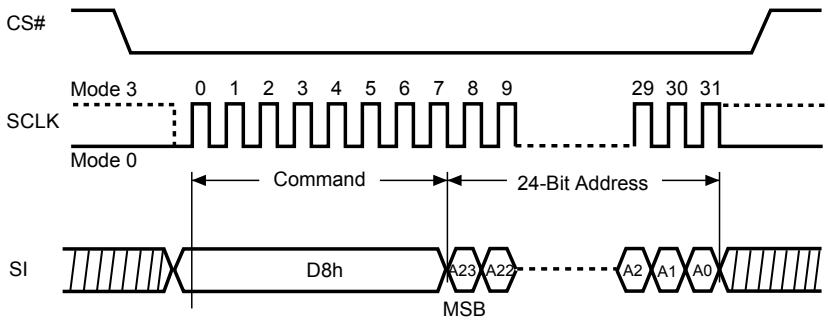
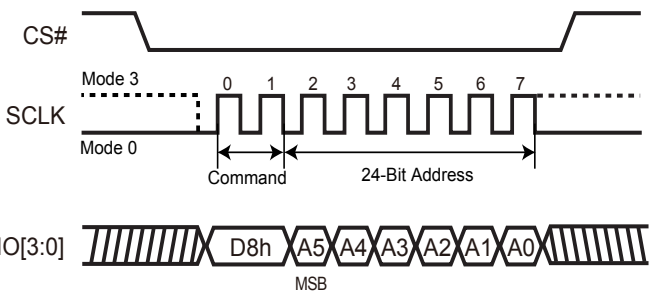


Figure 57. Block Erase (BE) Sequence (QPI Mode)



9-24. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→send CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode" (WPSEL=0). The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Individual Block Protection Mode" (WPSEL=1). The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

Figure 58. Chip Erase (CE) Sequence (SPI Mode)

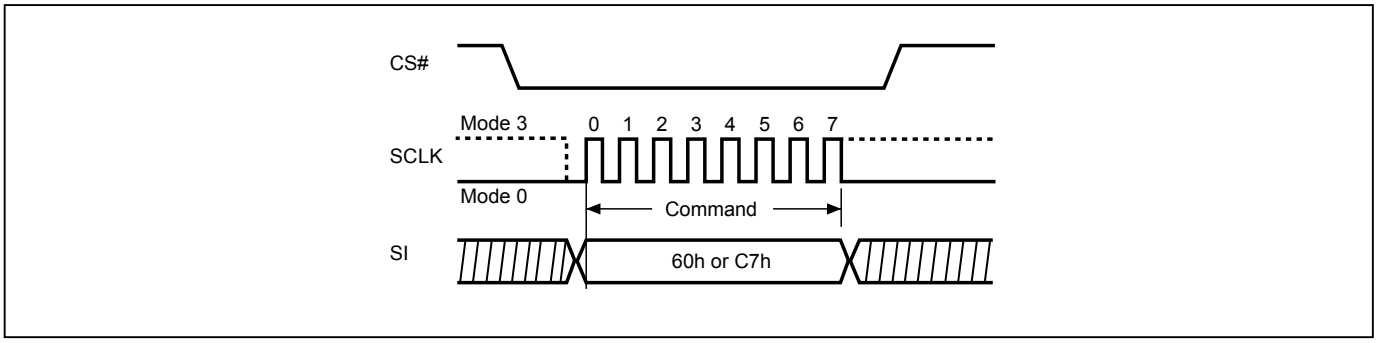
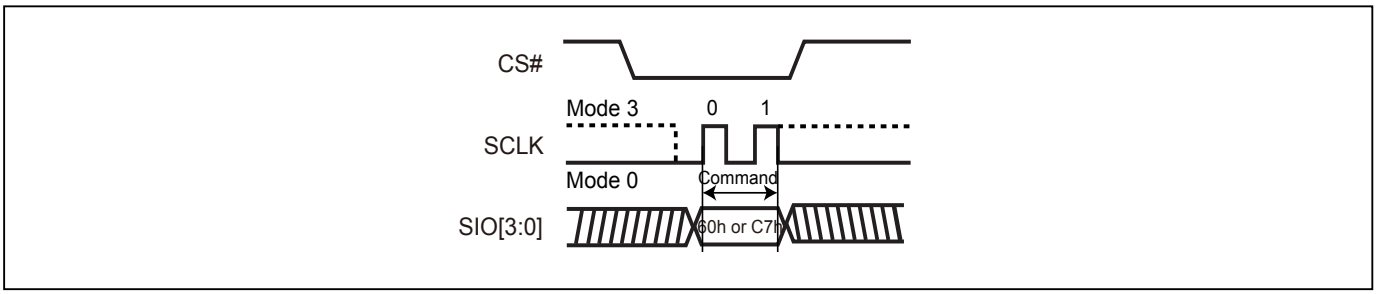


Figure 59. Chip Erase (CE) Sequence (QPI Mode)



9-25. Page Program (PP)

The Page Program (PP) instruction is for programming memory bits to "0". One to 256 bytes can be sent to the device to be programmed. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If more than 256 data bytes are sent to the device, only the last 256 data bytes will be accepted and the previous data bytes will be disregarded. The Page Program instruction requires that all the data bytes fall within the same 256-byte page. The low order address byte A[7:0] specifies the starting address within the selected page. Bytes that will cross a page boundary will wrap to the beginning of the selected page. The device can accept (256 minus A[7:0]) data bytes without wrapping. If 256 data bytes are going to be programmed, A[7:0] should be set to 0.

The sequence of issuing PP instruction is: CS# goes low→ send PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 60. Page Program (PP) Sequence (SPI Mode)

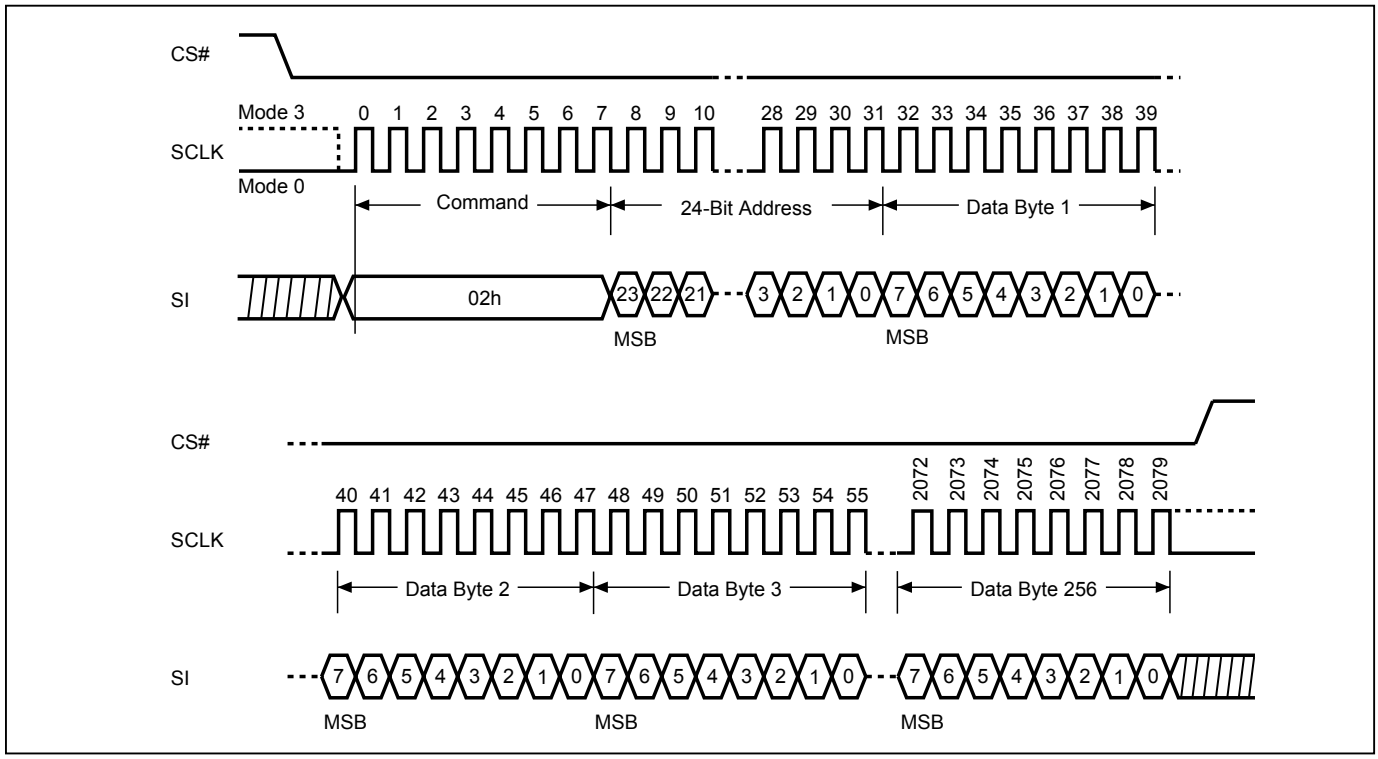
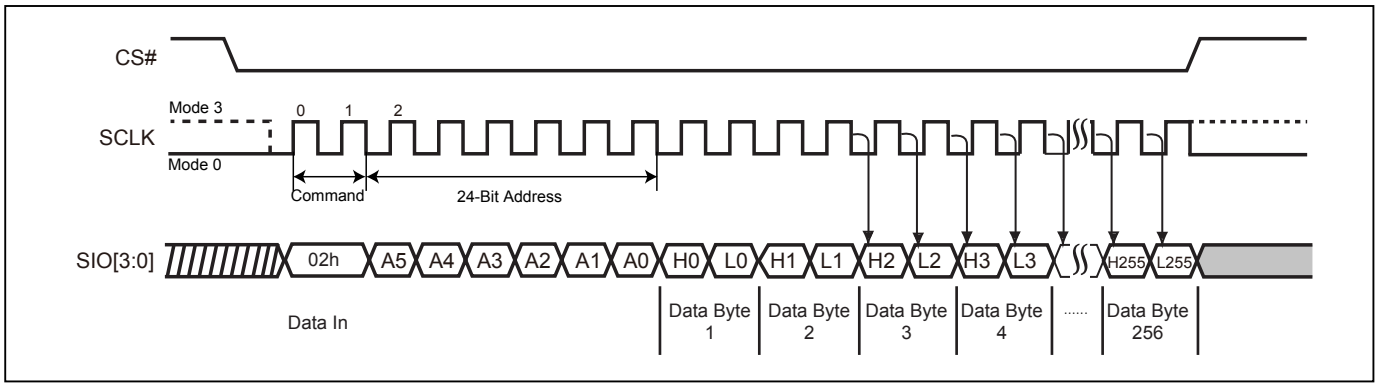


Figure 61. Page Program (PP) Sequence (QPI Mode)



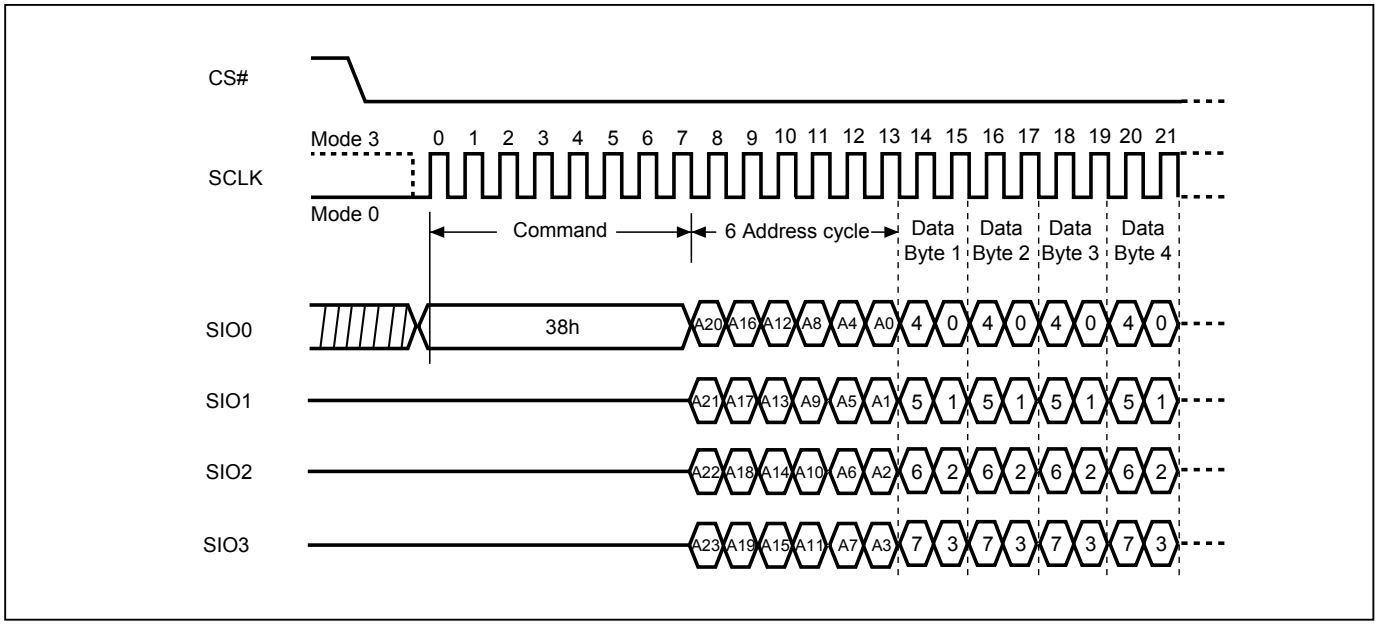
9-26. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sen 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP3, BP2, BP1, BP0 bits, the Quad Page Program (4PP) instruction will not be executed.

Figure 62. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)



9-27. Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Powerdown (RDP) instruction, power-cycle, or reset. Please refer to *"Figure 17. Release from Deep Power-down (RDP) Sequence (SPI Mode)"* and *"Figure 18. Release from Deep Power-down (RDP) Sequence (QPI Mode)"*.

Figure 63. Deep Power-down (DP) Sequence (SPI Mode)

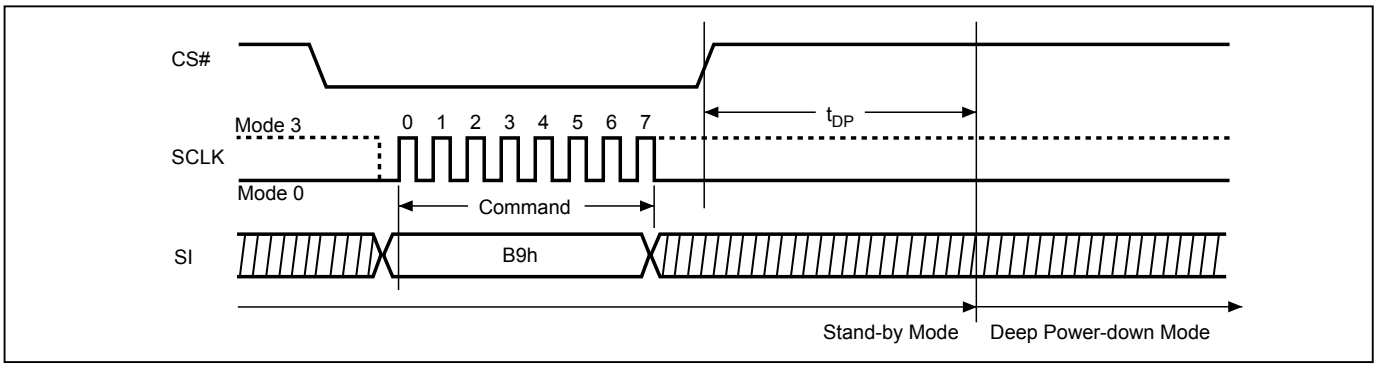
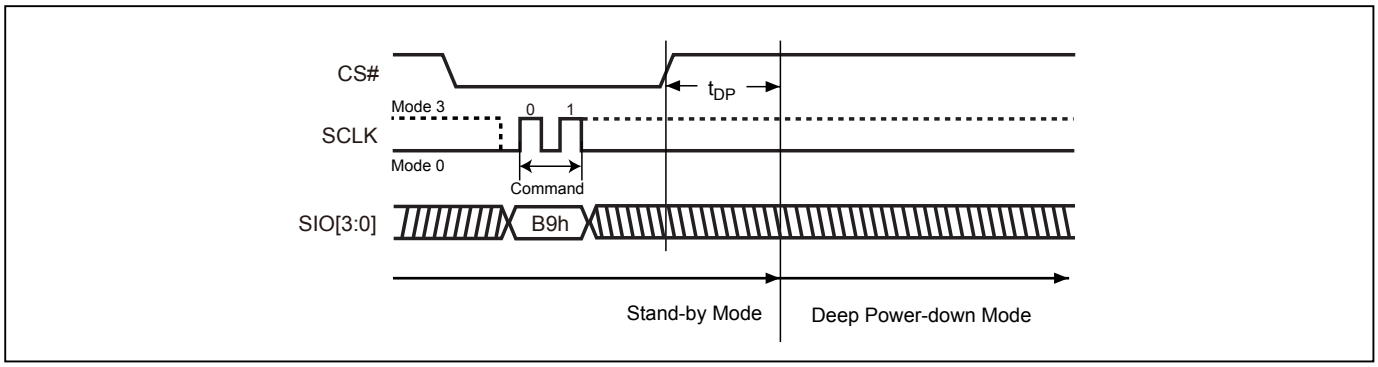


Figure 64. Deep Power-down (DP) Sequence (QPI Mode)



9-28. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. While device is in 4K-bit secured OTPmode, main array access is not available. The additional 4K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ send ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

9-29. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ send EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

9-30. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is: CS# goes low→send RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Figure 65. Read Security Register (RDSCUR) Sequence (SPI Mode)

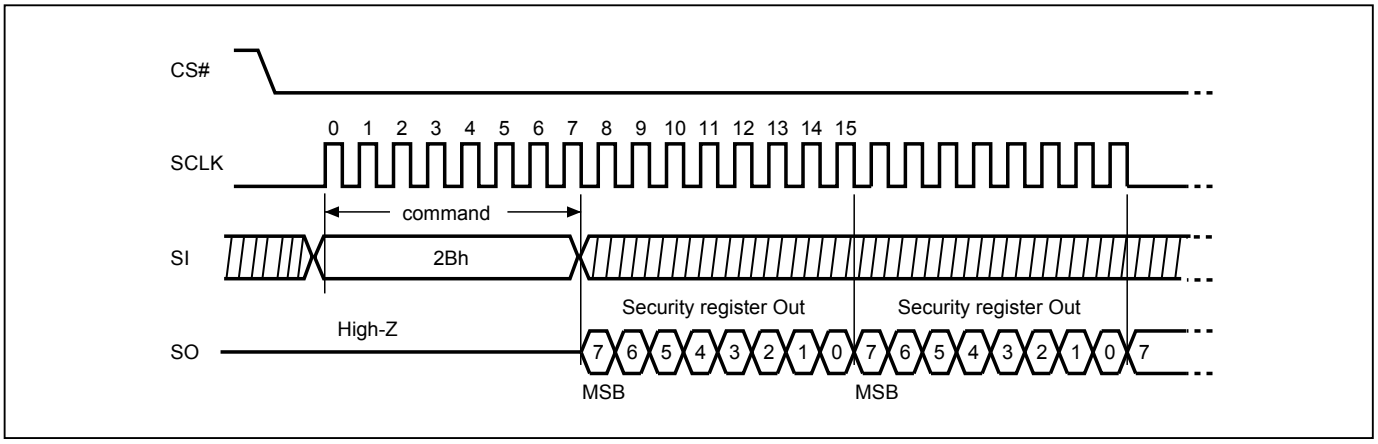
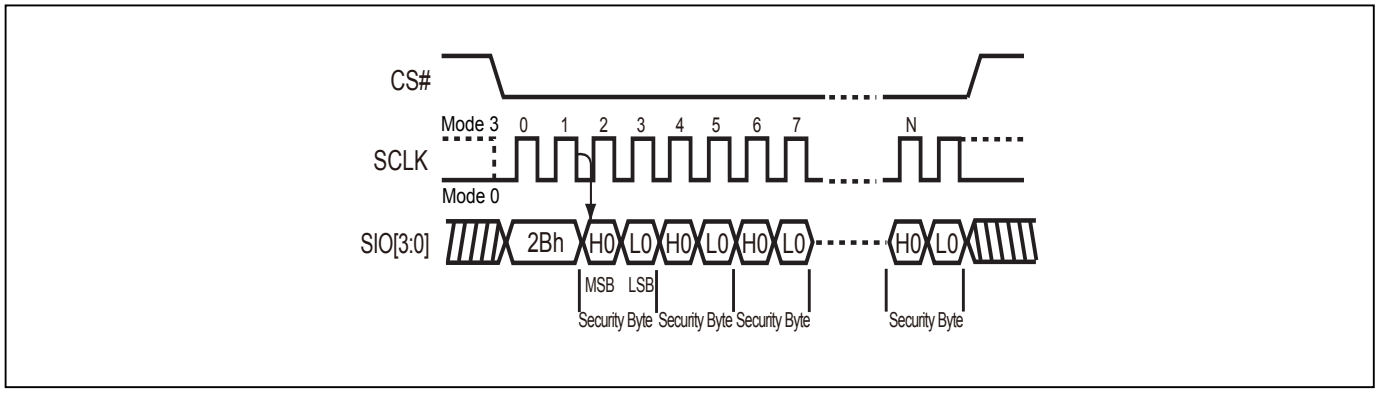


Figure 66. Read Security Register (RDSCUR) Sequence (QPI Mode)



9-31. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is: CS# goes low→ send WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 67. Write Security Register (WRSCUR) Sequence (SPI Mode)

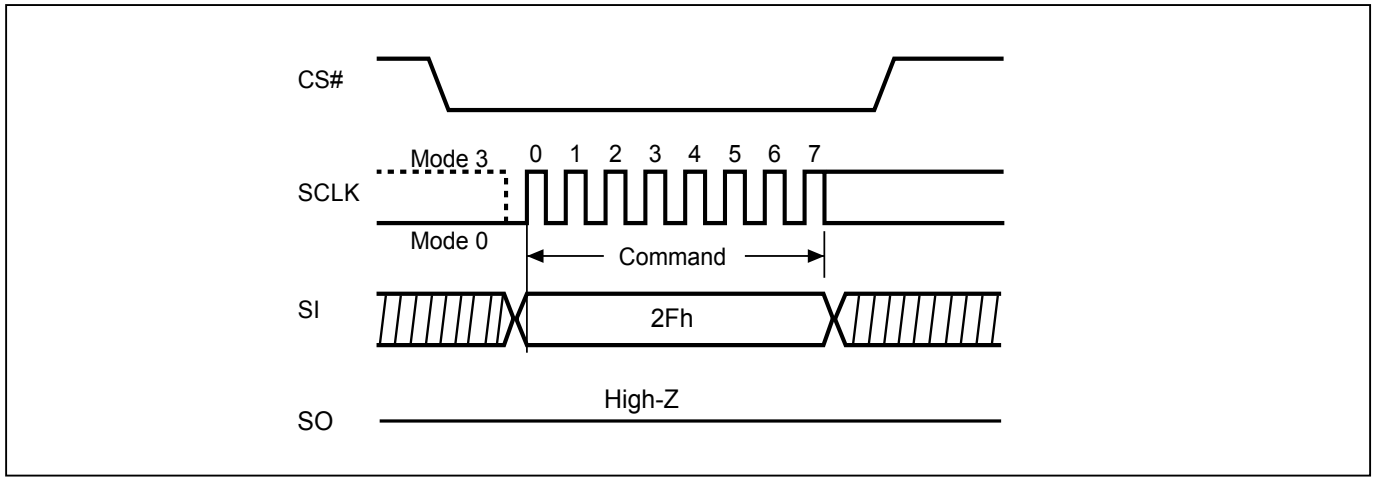
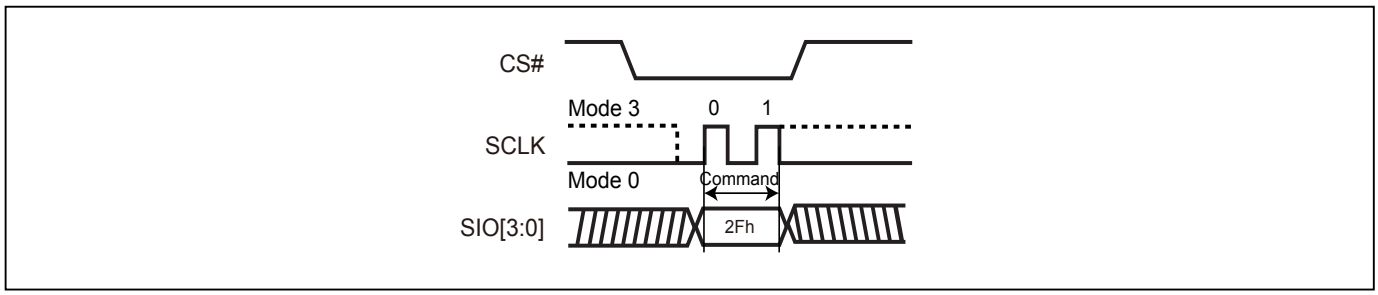


Figure 68. Write Security Register (WRSCUR) Sequence (QPI Mode)



Security Register

The definition of the Security Register bits is as below:

Write Protection Selection bit. Please reference to *"9-32. Write Protection Selection (WPSEL)"*.

Erase Fail bit. The Erase Fail bit is a status flag, which indicates the status of last Erase operation. It will be set to "1", if the erase operation fails. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit is a status flag, which indicates the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the Secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit secured OTP mode, main array access is not allowed.

Table 12. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=Block Lock (BP) protection mode 1=Individual Block Protection mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (Secured OTP can no longer be programmed)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

9-32. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Individual Block Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Individual Block Protection mode is disabled. If WPSEL=1, Individual Block Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command. Please note that the WPSEL bit is an OTP bit. Once WPSEL is set to "1", it cannot be programmed back to "0".

When WPSEL = 0: Block Lock (BP) protection mode,
The memory array is write protected by the BP3-BP0 bits as in *"Figure 69. BP and SRWD if WPSEL=0"*.

When WPSEL =1: Individual Block Protection mode,
Blocks are individually protected by their own SRAM lock bits. On power-up, all blocks are write protected by the SRAM bits by default. The Individual Block Protection instructions SBLK, SBULK, RDBLOCK, GBLK, and GBULK are activated. The BP3-BP0 bits of the Status Register are disabled and have no effect. Hardware protection is performed by driving WP#=0. Once WP#=0 all blocks and sectors are write protected regardless of the state of each SRAM lock bit. Please refer to *"Figure 70. The individual block lock mode is effective after setting WPSEL=1"*.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enable the Individual Block Protect mode → CS# goes high. Please refer to *"Figure 71. Write Protection Selection (WPSEL) Sequence (Command 68h)"*.

Figure 69. BP and SRWD if WPSEL=0

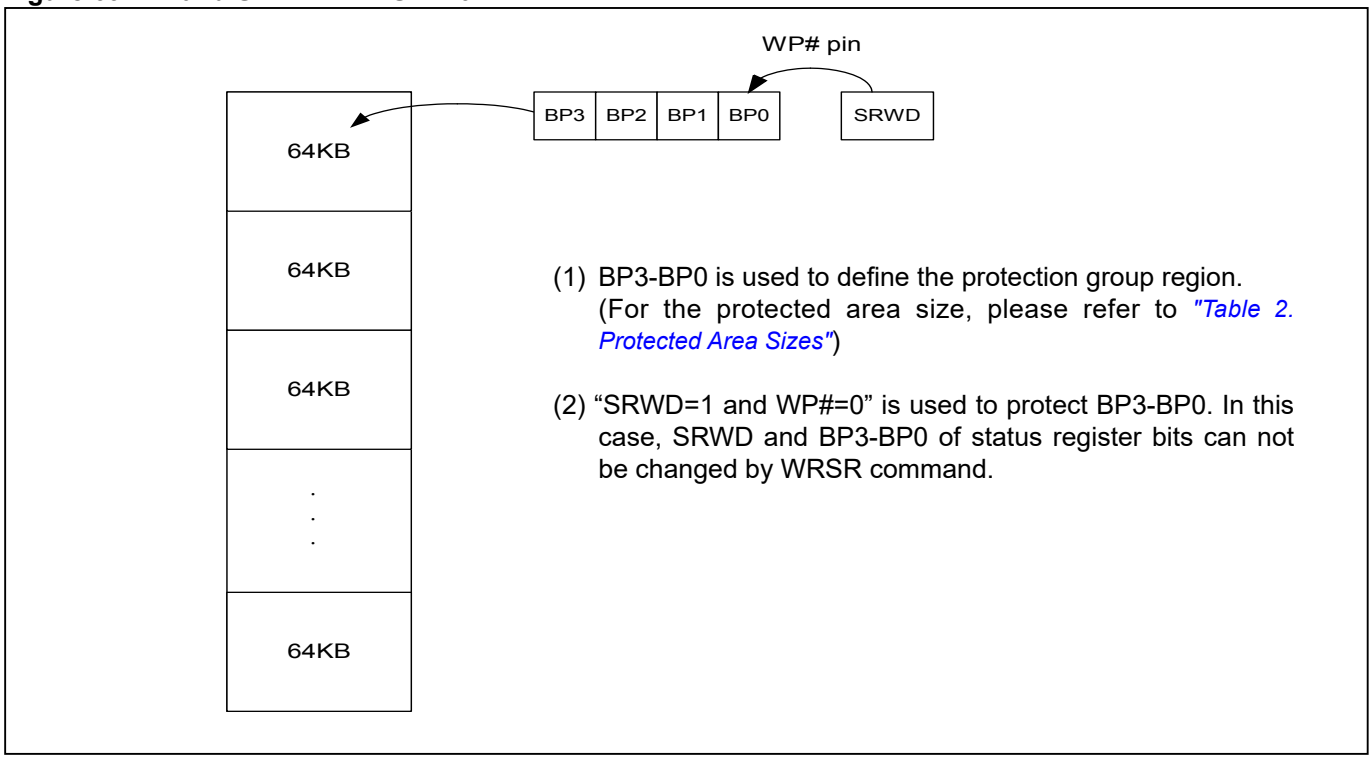
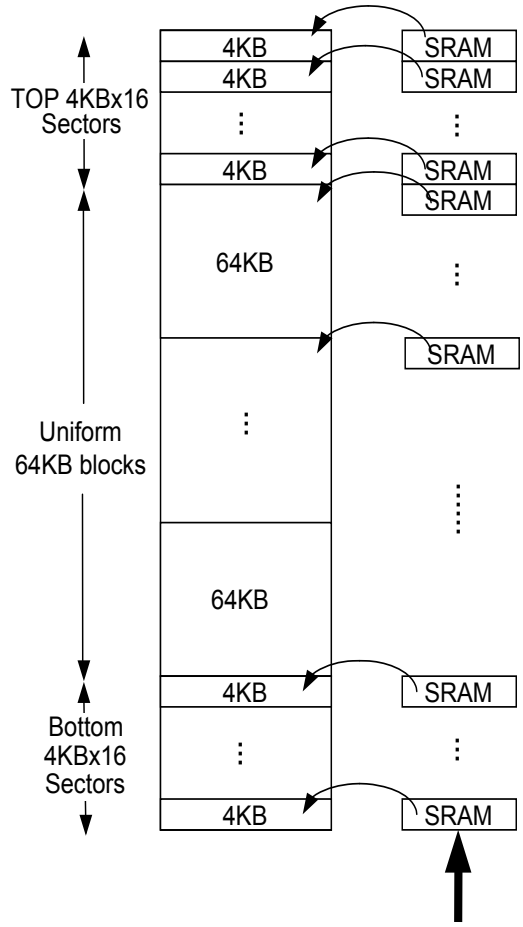


Figure 70. The individual block lock mode is effective after setting WPSEL=1



- Power-Up: All SRAM bits=1 (all blocks are default protected). All array cannot be programmed/erased
- SBLK/SBULK(36h/39h):
  - SBLK(36h): Set SRAM bit=1 (protect) : array can not be programmed/erased
  - SBULK(39h): Set SRAM bit=0 (unprotect): array can be programmed/erased
  - All top 4KBx16 sectors and bottom 4KBx16 sectors and other 64KB uniform blocks can be protected and unprotected by SRAM bits individually by SBLK/SBULK command set.
- GBLK/GBULK(7Eh/98h):
  - GBLK(7Eh): Set all SRAM bits=1, whole chip is protected and cannot be programmed/erased.
  - GBULK(98h): Set all SRAM bits=0, whole chip is unprotected and can be programmed/erased.
  - All sectors and blocks SRAM bits of whole chip can be protected and unprotected at one time by GBLK/GBULK command set.
- RDBLOCK(3Ch):
  - use RDBLOCK mode to check the SRAM bits status after SBULK /SBLK/GBULK/GBLK command set.

Figure 71. Write Protection Selection (WPSEL) Sequence (Command 68h)

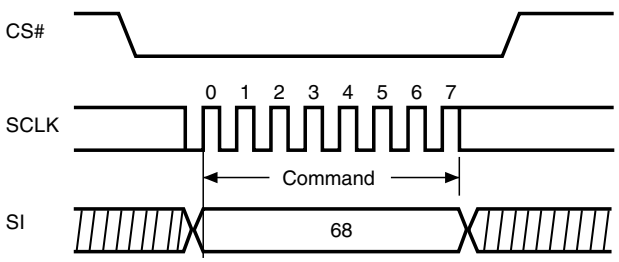
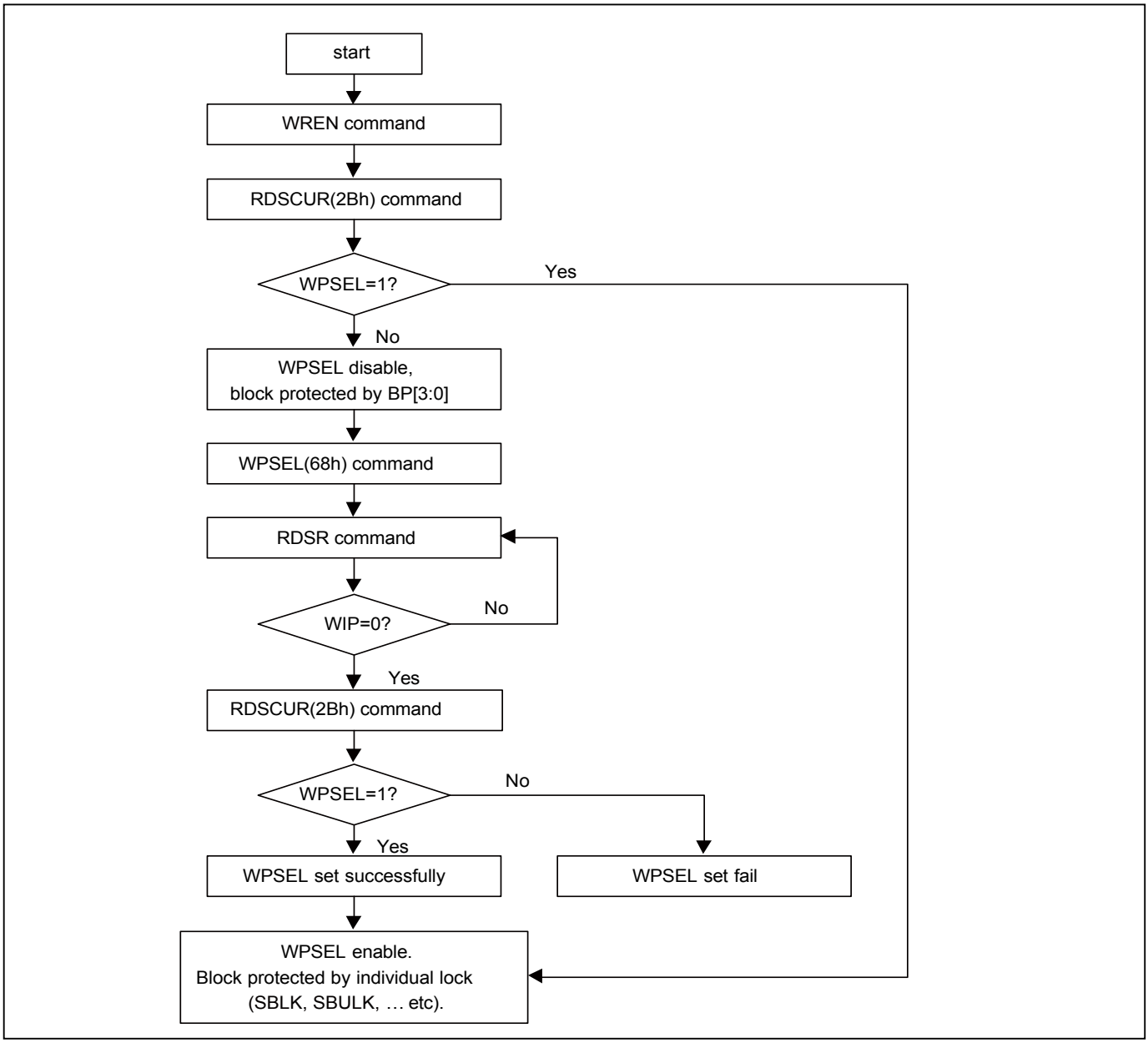


Figure 72. WPSEL Flow



9-33. Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective if WPSEL=1. The SBLK instruction is for write protection a specified block (or sector) of memory, using A_{MAX}-A16 or (A_{MAX}-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction→send 3-byte address assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are "don't care" in SPI mode.

SBLK/SBULK instruction function flow is as follows:

Figure 73. Block Lock Flow

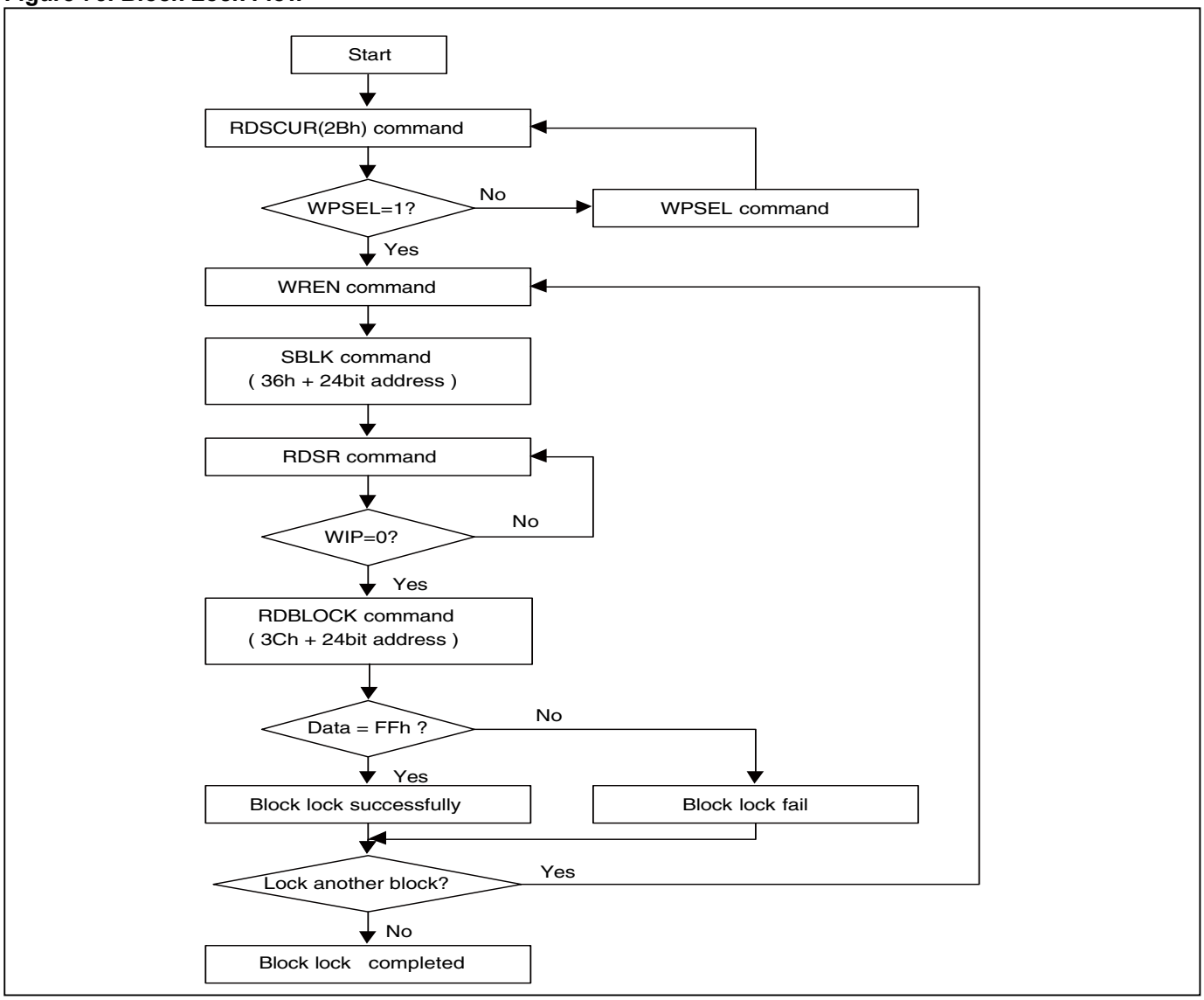
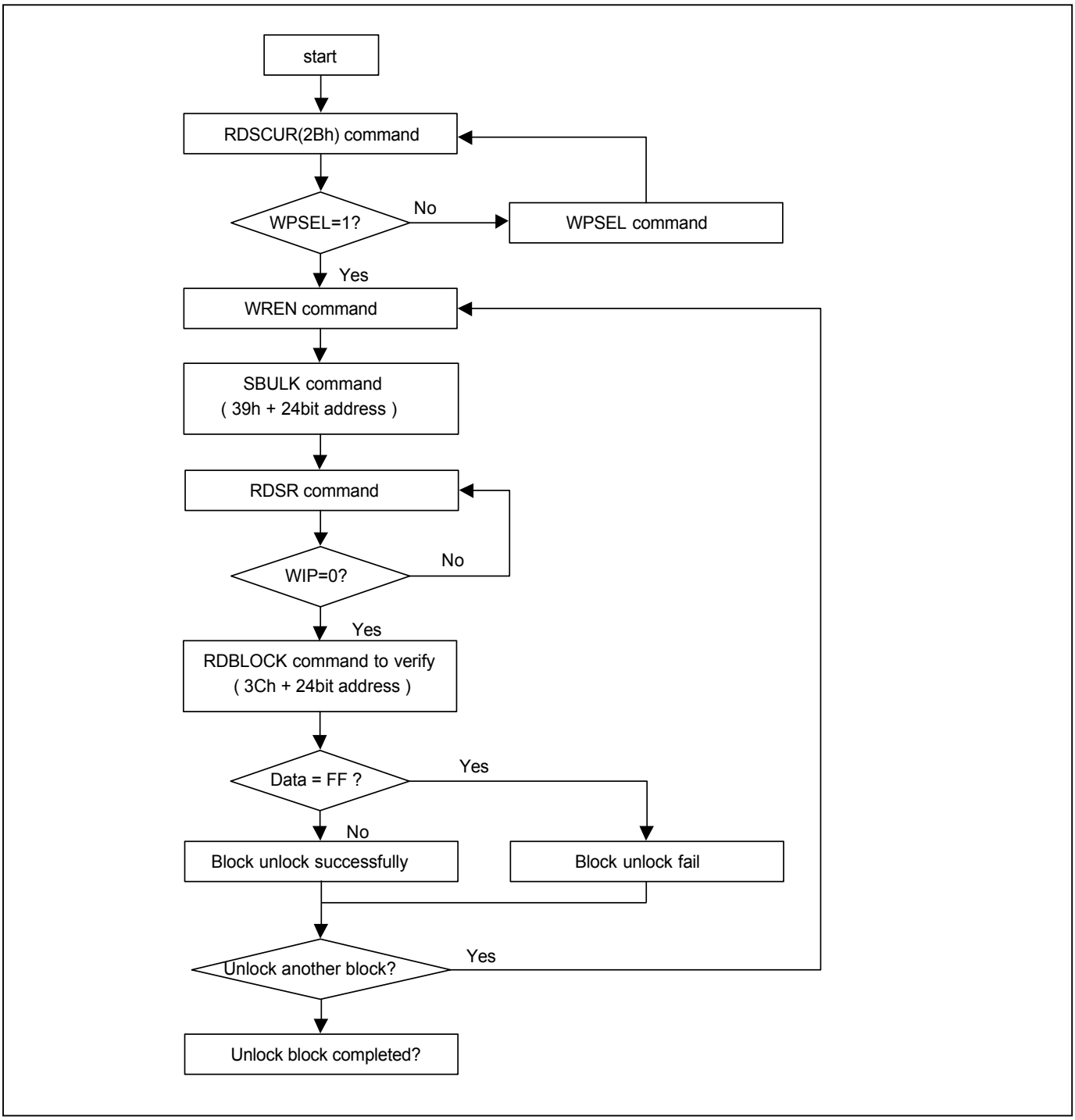


Figure 74. Block Unlock Flow



9-34. Read Block Lock Status (RDBLOCK)

This instruction is only effective if WPSEL=1. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using A_{MAX}-A16 (or A_{MAX}-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3-byte address to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

This instruction are accepted in both SPI and QPI mode. The SIO[3:1] are "don't care" in SPI mode.

9-35. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective if WPSEL=1. The GBLK and GBULK instructions provide a quick method to enable/disable the lock protection block of the whole chip at once.

The WREN (Write Enable) instruction is required before issuing the GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

This instruction are accepted in both SPI and QPI mode. The SIO[3:1] are "don't care" in SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

9-36. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased (*"Table 13. Readable Area of Memory While a Program or Erase Operation is Suspended"*).

Table 13. Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Sector Erase (4KB)	All but the 4KB Sector being erased
Block Erase (32KB)	All but the 32KB Block being erased
Block Erase (64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL (*"Figure 75. Suspend to Read Latency"*) before the Write Enable Latch (WEL) bit clears to “0” and the PSB or ESB sets to “1”, after which the device is ready to accept one of the commands listed in *"Table 14. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"* (e.g. FAST READ). Refer to *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"* for tPSL and tESL timings.

"Table 15. Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status (please refer to *"Table 12. Security Register Definition"*). The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

Figure 75. Suspend to Read Latency

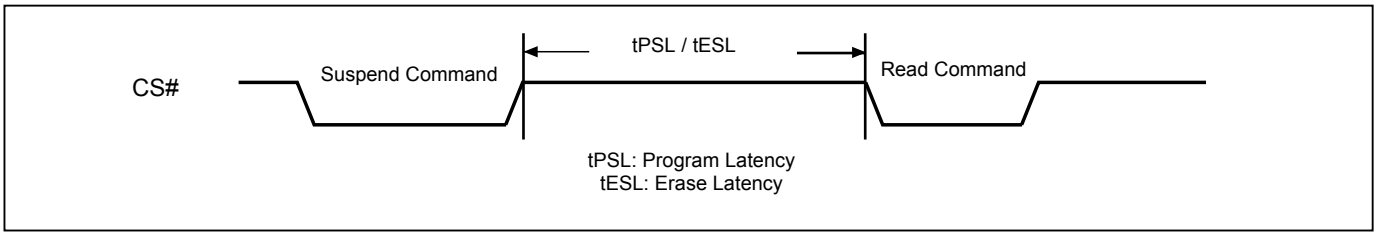


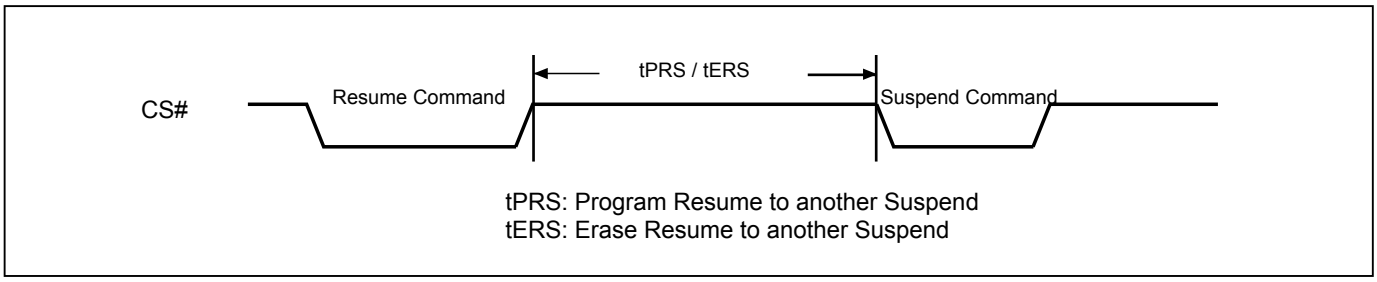
Table 14. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03h	•	•
FAST READ	0Bh	•	•
DREAD	3Bh	•	•
QREAD	6Bh	•	•
2READ	BBh	•	•
4READ	EBh	•	•
4DTRD	EDh	•	•
W4READ	E7h	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
QPIID	AFh	•	•
REMS	90h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h	•	•
EQIO	35h	•	•
RSTQIO	F5h	•	•
RESUME	7Ah or 30h	•	•
SBL	C0h	•	•

Table 15. Acceptable Commands During Suspend (tPSL/tESL not required)

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

Figure 76. Resume to Suspend Latency



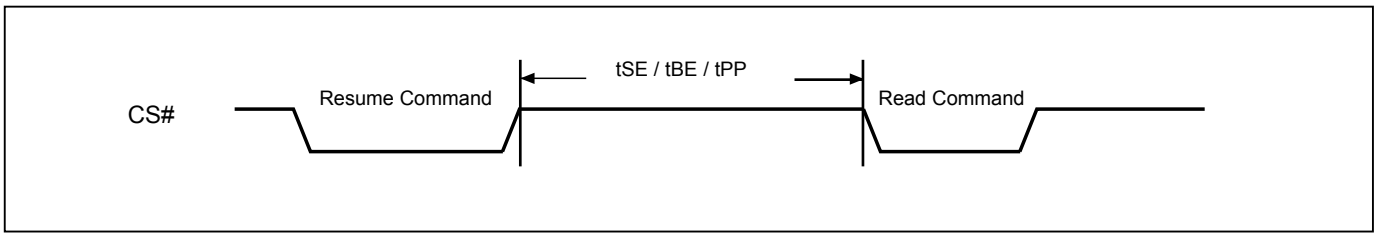
9-37. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”. The program or erase operation will continue until finished (*"Figure 77. Resume to Read Latency"*) or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction (*"Figure 76. Resume to Suspend Latency"*).

Please note that the Resume instruction will be ignored if the Serial NOR Flash is in “Performance Enhance Mode”. Make sure the Serial NOR Flash is not in “Performance Enhance Mode” before issuing the Resume instruction.

Figure 77. Resume to Read Latency



9-38. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

9-39. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

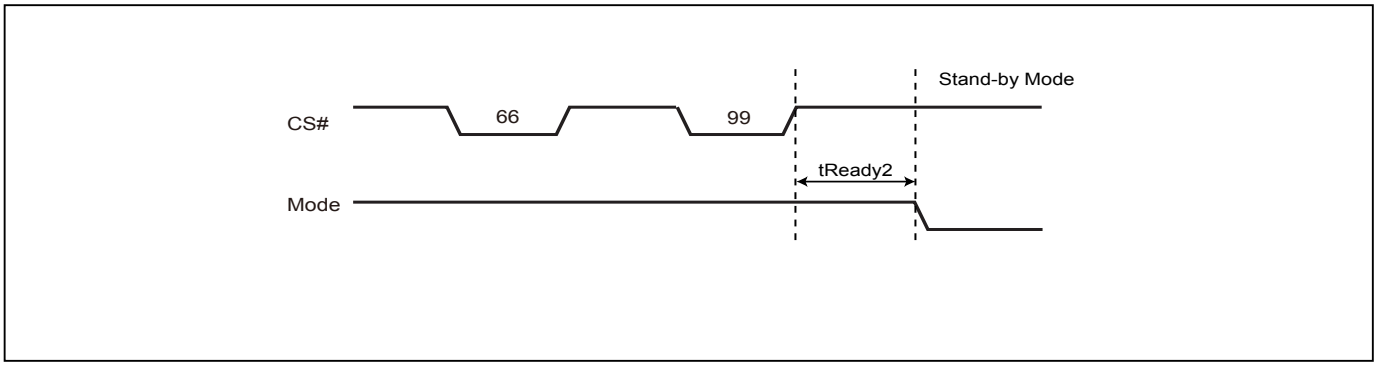
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"* for tREADY2.

Figure 78. Software Reset Recovery



Note: Refer to *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"* for tREADY2 data.

Figure 79. Reset Sequence (SPI mode)

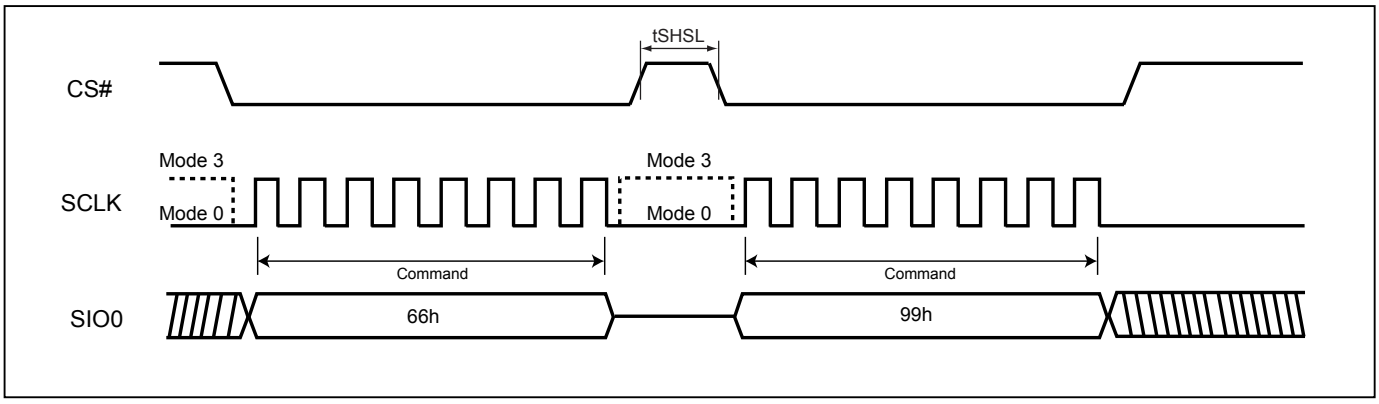
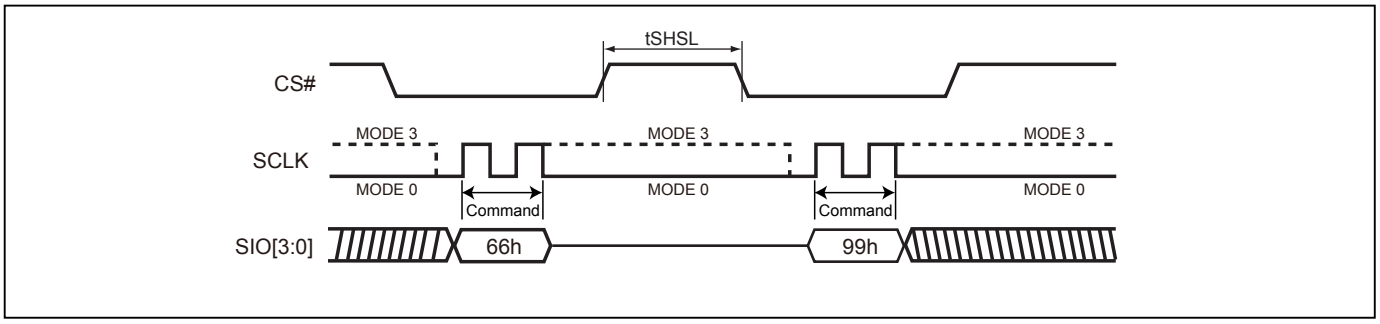


Figure 80. Reset Sequence (QPI mode)



9-40. Read SFDP Mode (RDSFDP)

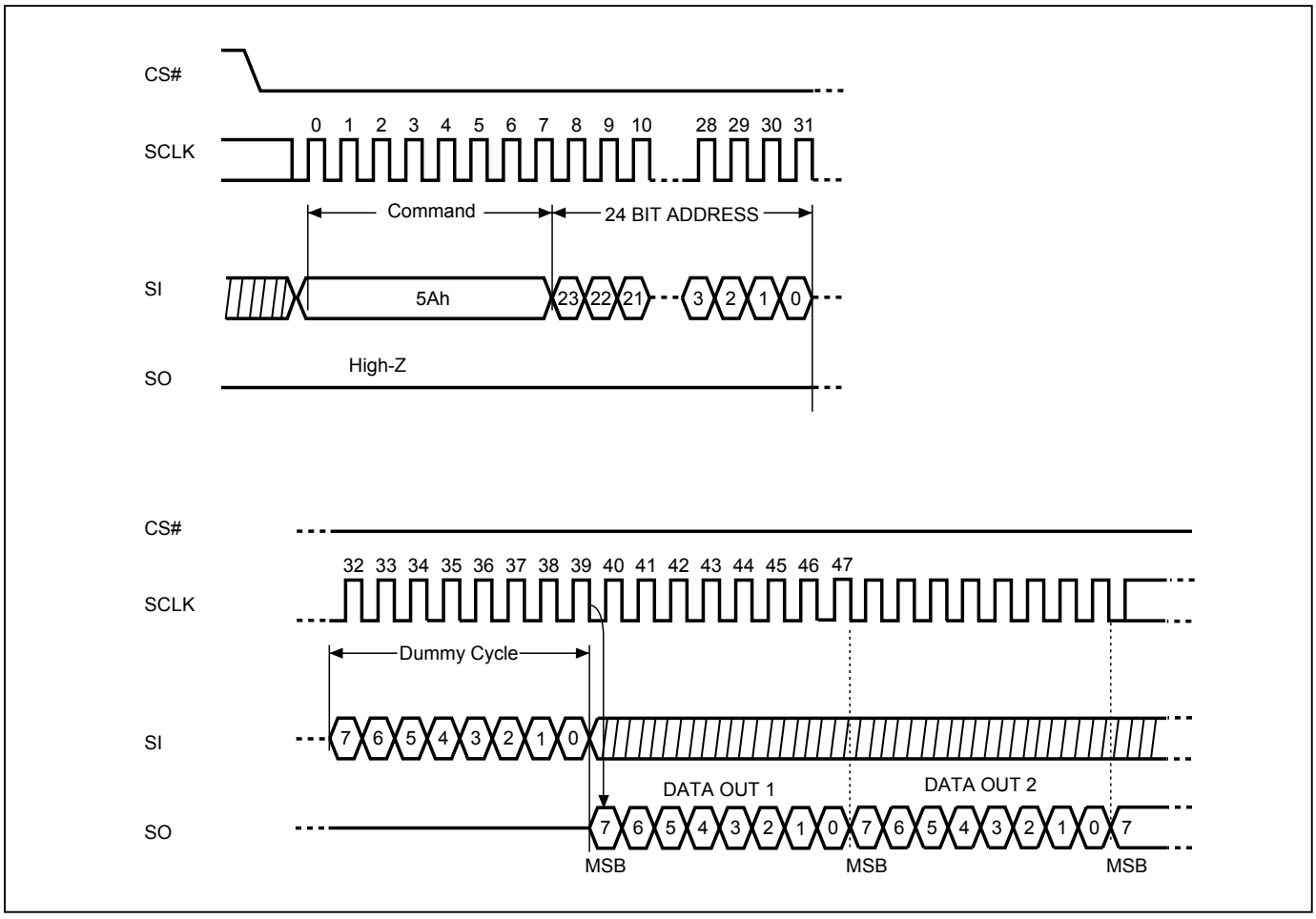
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC standard, JESD216B.

For SFDP register values detail, please contact local Macronix sales channel.

Figure 81. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



10. POWER-ON STATE

The device is in the states below when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the *"Figure 89. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

11. ELECTRICAL SPECIFICATIONS

Table 16. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 82. Maximum Negative Overshoot Waveform

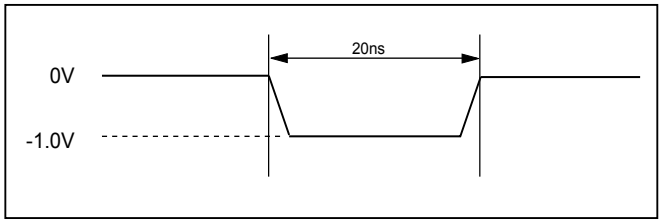


Figure 83. Maximum Positive Overshoot Waveform

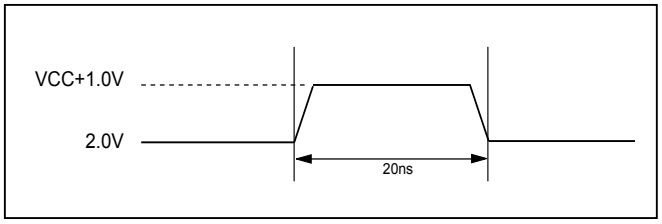
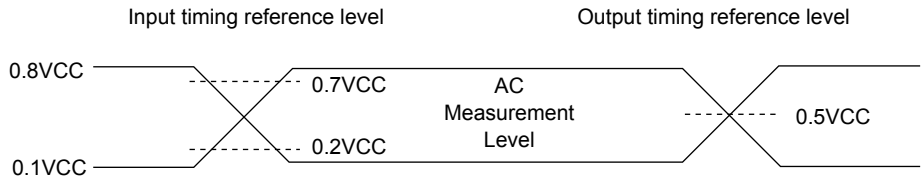


Table 17. CAPACITANCE TA = 25°C, f = 1.0 MHz

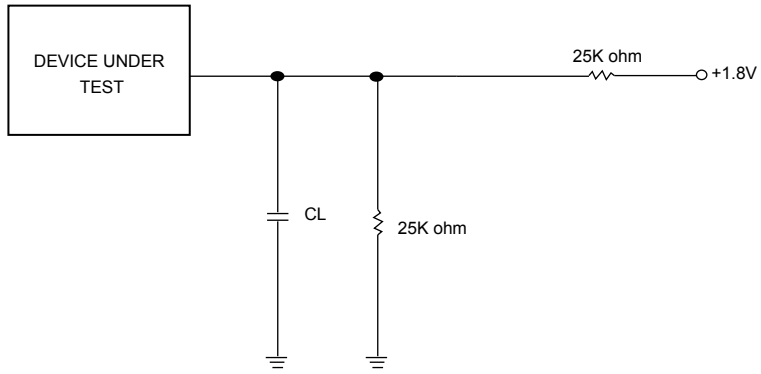
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 84. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <5ns

Figure 85. OUTPUT LOADING



CL=30pF Including jig capacitance

Figure 86. SCLK TIMING DEFINITION

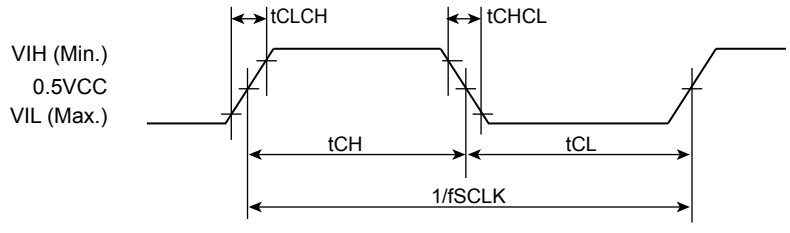


Table 18. DC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		15	70	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			0.8	30	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		11	25	mA	f=133MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				9	20	mA	f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				7	15	mA	f=84MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		15	25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			10	20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		10	25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		12	25	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.2VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :

1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for all commands (except Read)			D.C.		133	MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions			Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"*			MHz
	fQ	Clock Frequency for 4READ/QREAD instructions						MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK/fTSCLK)	> 50MHz	45% x (1/fSCLK)			ns
				≤ 50MHz	7			ns
			Normal Read (fRSCLK)		7			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK/fTSCLK)	> 50MHz	45% x (1/fSCLK)			ns
				≤ 50MHz	7			ns
			Normal Read (fRSCLK)		7			ns
tCLCH(2)		Clock Rise Time (peak to peak)			0.1			V/ns
tCHCL(2)		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			5			ns
tDVCH/ tDVCL	tDSU	Data In Setup Time			2			ns
tCHDX/ tCLDX	tDH	Data In Hold Time			3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			5			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read		7			ns
			From Write/Erase/Program to Read Status Register		30			ns
tSHQZ(2)	tDIS	Output Disable Time					8	ns
tCLQV	tV	Clock Low to Output Valid Loading: 30pF/15pF	Loading: 30pF				8	ns
			Loading: 15pF				6	ns
tCLQX	tHO	Output Hold Time	Loading: 30pF		1			ns
			Loading: 15pF		1			ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tDP(2)		CS# High to Deep Power-down Mode					10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read					30	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read					30	us

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tW		Write Status/Configuration Register Cycle Time			40	ms
tBP		Byte-Program		14	30	us
tPP		Page Program Cycle Time		0.36	3	ms
tSE		Sector Erase Cycle Time		35	400	ms
tBE32		Block Erase (32KB) Cycle Time		170	1000	ms
tBE		Block Erase (64KB) Cycle Time		300	2000	ms
tCE		Chip Erase Cycle Time		55	150	s
tQVD(5)		Data Output Valid Time Difference among all SIO pins			600	ps
tESL(6)		Erase Suspend Latency			25	us
tPSL(6)		Program Suspend Latency			25	us
tPRS(7)		Latency between Program Resume and next Suspend	0.3	100		us
tERS(8)		Latency between Erase Resume and next Suspend	0.3	100		us
tREADY2		Reset Recovery time (During instruction decoding)	40			
		Reset Recovery time (for read operation)	35			
		Reset Recovery time (for program operation)	310			
		Reset Recovery time(for SE4KB operation)	12			
		Reset Recovery time (for BE64KB/BE32KB operation)	25			
		Reset Recovery time (for Chip Erase operation)	100			
		Reset Recovery time (for WRSR operation)	40			

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. The value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as *"Figure 84. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL"* and *"Figure 85. OUTPUT LOADING"*.
5. Not 100% tested.
6. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
7. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
8. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.

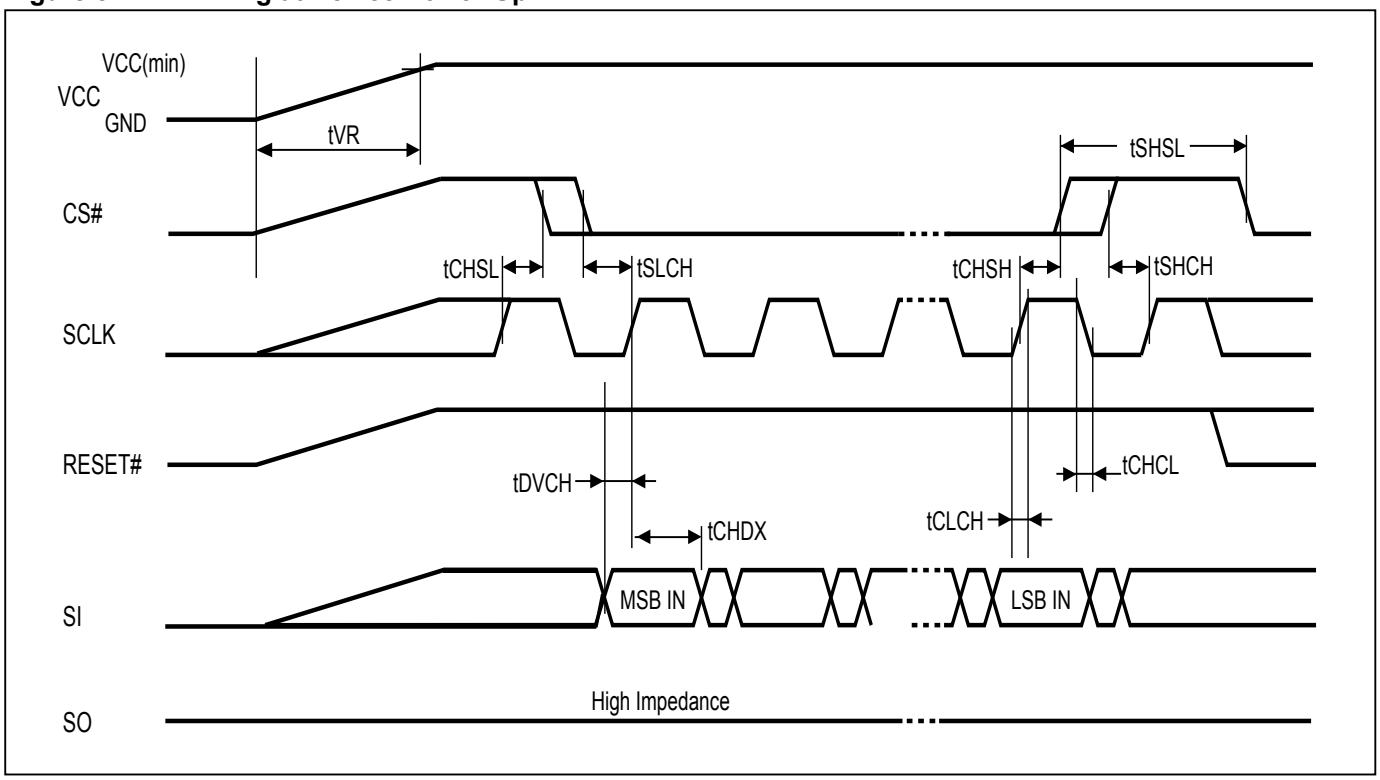
12. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 87. AC Timing at Device Power-Up"* and *"Figure 88. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 87. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes:
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V - 2.0V)"*.

Figure 88. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

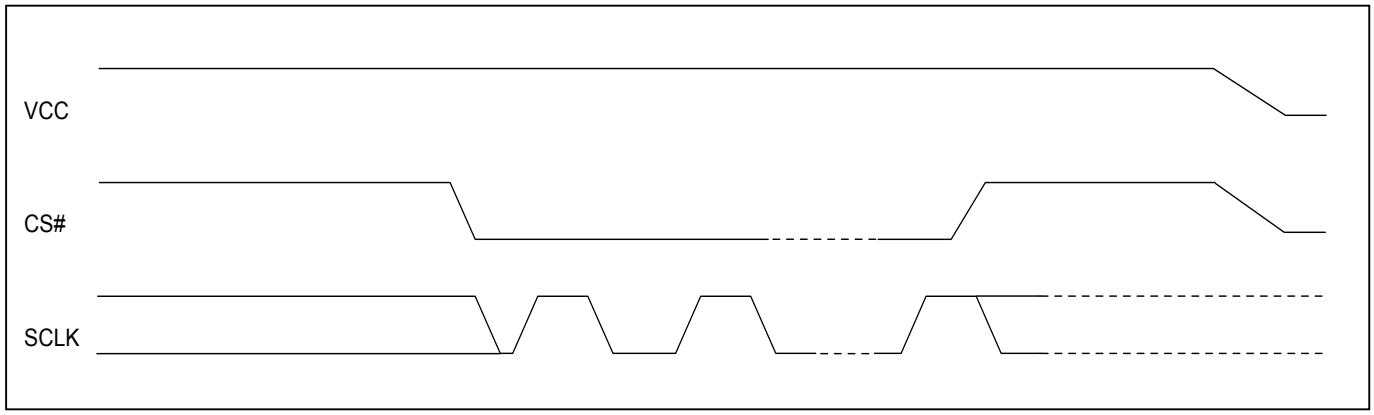


Figure 89. Power-up Timing

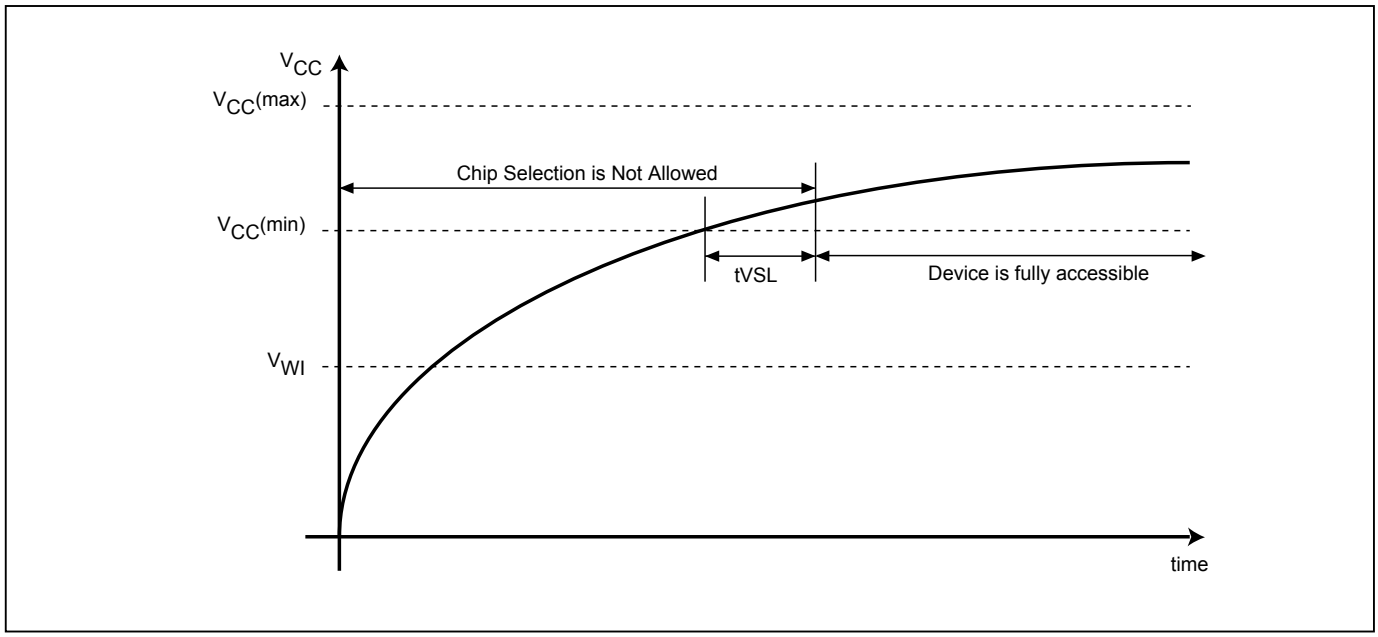


Figure 90. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 90. Power Up/Down and Voltage Drop"* and *"Table 20. Power-Up/Down Voltage and Timing"* below for more details.

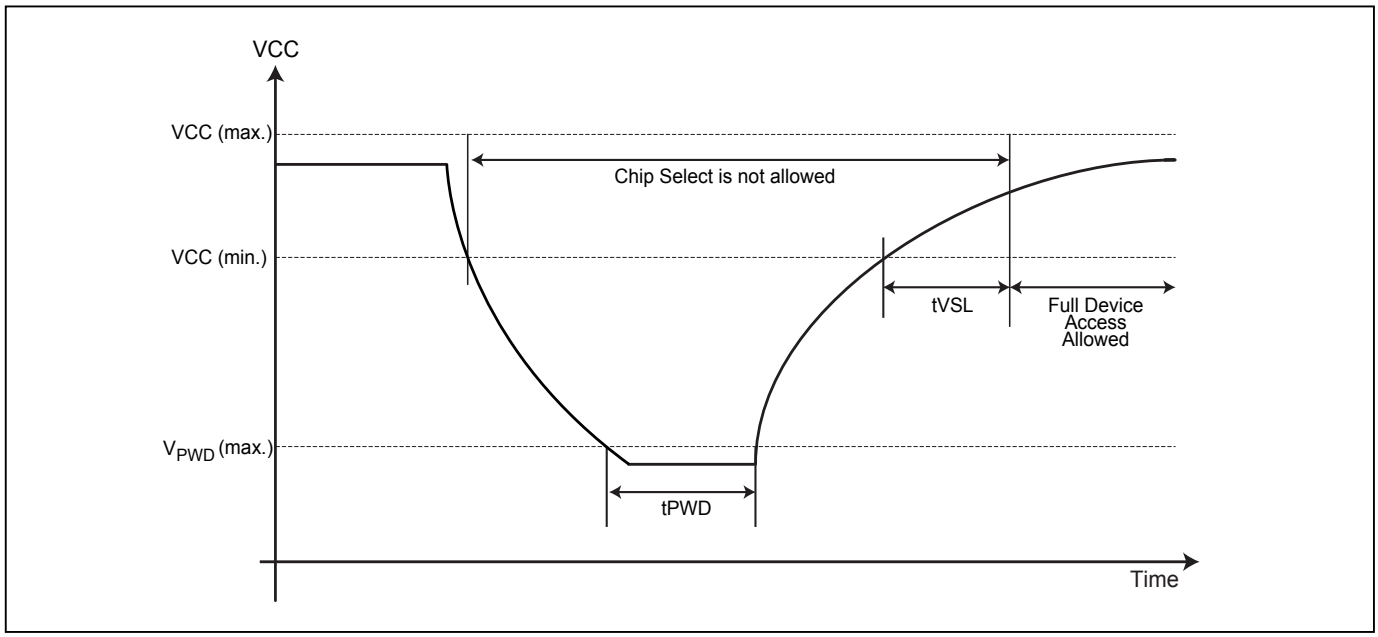


Table 20. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	1500		us
VWI	Write Inhibit Voltage	1.0	1.4	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
VCC	VCC Power Supply	1.65	2.0	V

Note: These parameters are characterized only.

12-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 40h (all Status Register bits are 0 except QE bit: QE=1).

13. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		35	400	ms
Block Erase Cycle Time (32KB)		0.17	1	s
Block Erase Cycle Time (64KB)		0.3	2	s
Chip Erase Cycle Time		55	150	s
Byte Program Time (via page program command)		14	30	us
Page Program Time		0.36	3	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.
2. Under worst conditions of 1.65V, highest operation temperature, post program/erase cycling.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

14. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode)

Parameter	Min.	Typ.	Max.	Unit
Sector Erase Cycle Time (4KB)		20		ms
Block Erase Cycle Time (32KB)		0.1		s
Block Erase Cycle Time (64KB)		0.2		s
Chip Erase Cycle Time		50		s
Page Program Time		0.3		ms
Erase/Program Cycle			50	cycles

Notice:
1. Factory Mode must be operated in 20°C to 45°C and VCC 1.8V-2.0V.
2. In Factory mode, the Erase/Program operation should not exceed 50 cycles, and "ERASE AND PROGRAMMING PERFORMANCE" 100k cycles will not be affected.
3. During factory mode, Suspend command (75h or B0h) cannot be executed.

15. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

16. LATCH-UP CHARACTERISTICS

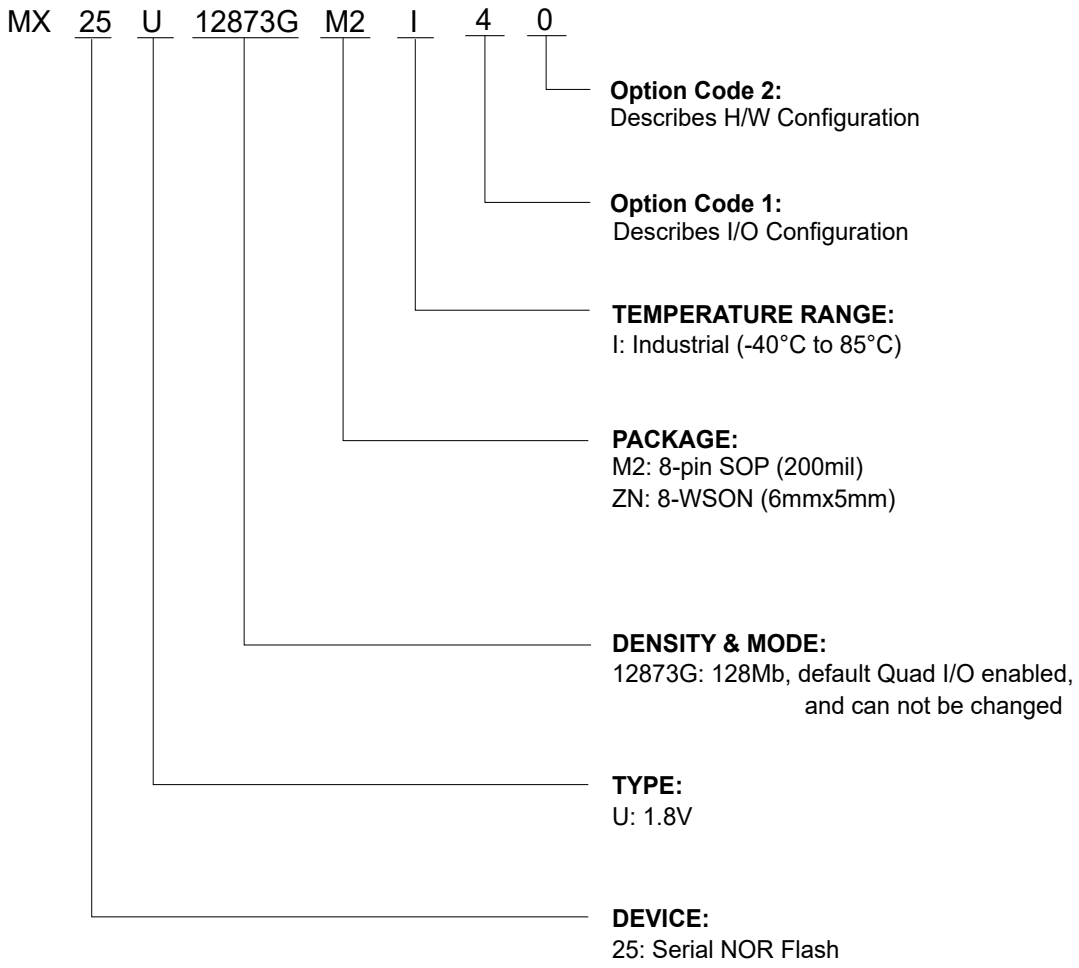
	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-100mA	+100mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard).		

17. ORDERING INFORMATION

Please refer to the individual product pages of Macronix Website or contact Macronix regional Sales for the latest Full Part Numbers and available form factor selection.

PART NO.	Package	Temp.	I/O Configuration			H/W Configuration	Remark
			CS#	Default I/O	Dummy Cycle	H/W Pin	
MX25U12873GM2I40	8-SOP (200mil)	-40°C to 85°C	1 Pin	Permanent 4 I/O	Standard		
MX25U12873GZNI40	8-WSON (6x5mm)	-40°C to 85°C	1 Pin	Permanent 4 I/O	Standard		

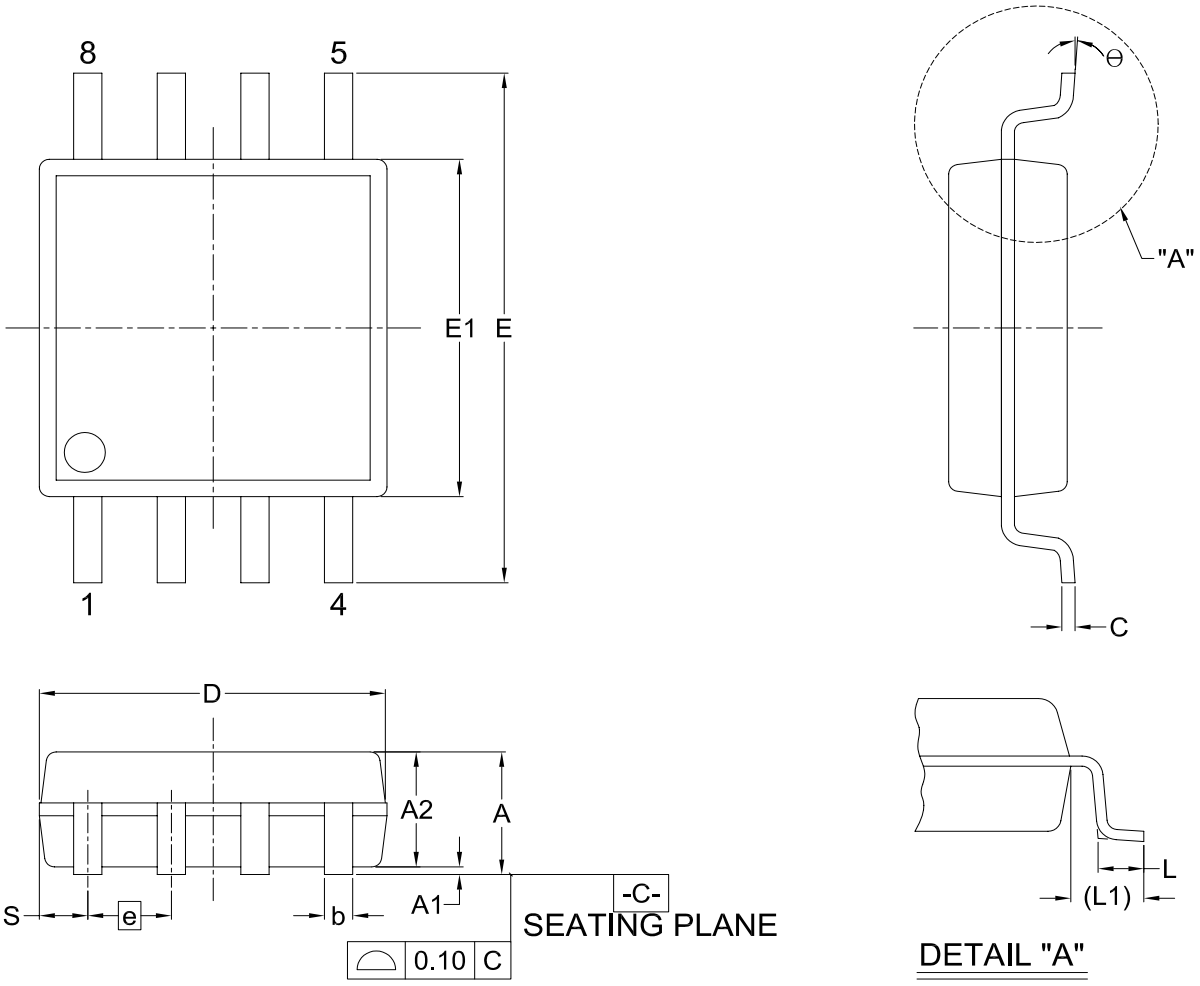
18. PART NAME DESCRIPTION



19. PACKAGE INFORMATION

19-1. 8-pin SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL

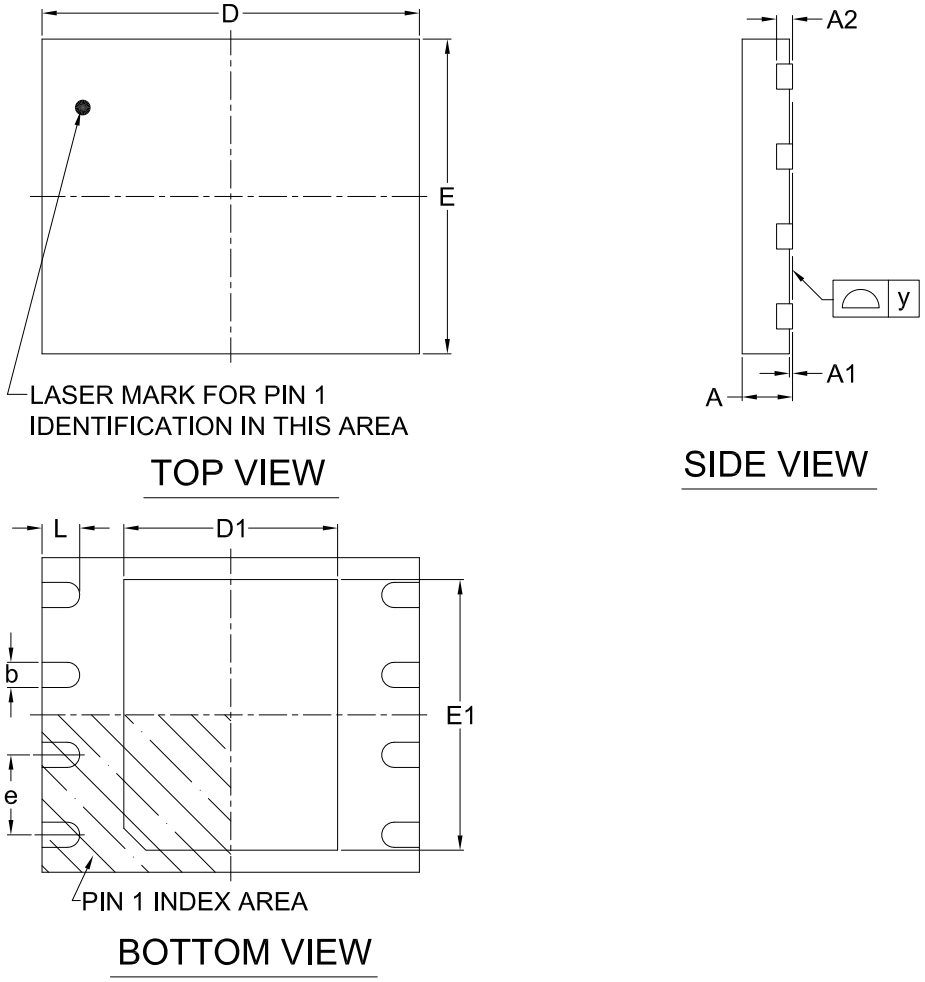


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8°

19-2. 8-land WSON (6x5mm)

Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.35	4.90	3.95	0.55	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.45	5.10	4.05	0.65	---	0.05
Inch	Mln.	0.028	---	---	0.014	0.232	0.132	0.193	0.156	0.022	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.136	0.201	0.159	0.026	---	0.002

20. REVISION HISTORY

Revision	Descriptions	Page
March 23, 2021		
0.00	1. Initial Release.	All
July 02, 2025		
0.01	1. Added Part Number: MX25U12873GZNI40.	P4, 6, 92-93, 95
	2. Description modification.	P9, 13, 35-36, 38, 43-47, 92
	3. Corrected *"Table 3. 4K-bit Secured OTP Definition"*.	P10
	4. Modified RES descriptions.	P27
September 19, 2025		
1.0	1. Removed "ADVANCED INFORMATION" to align with the product status.	ALL
	2. Corrected document P/N number.	ALL

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