4M-BIT [x 1] CMOS SERIAL FLASH

FEATURES

GENERAL

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 4,194,304 x 1 bit structure
- 128 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 8 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
  - Fast access time: 85MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Fast erase time: 60ms(typ.) and 120ms(max.)/sector (4K-byte per sector) ; 1s(typ.) and 2s(max.)/block (64K-byte per block)
- Low Power Consumption
  - Low active read current: 12mA(max.) at 85MHz, 8mA(max.) at 66MHz and 4mA(max.) at 33MHz
  - Low active programming current: 15mA (max.)
  - Low active erase current: 15mA (max.)
  - Low standby current: 10uA (max.)
  - Deep power-down mode 1uA (typical)
- Minimum 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Block Lock protection
  - The BP0~BP2 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 2-byte Device ID
  - RES command, 1-byte Device ID

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- WP# pin
  - Hardware write protection

- HOLD# pin
  - pause the chip without diselecting the chip
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)
  - 8-pin PDIP (300mil)
  - 8-land SON (6x5mm)
  - **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX25L4005A is a CMOS 4,194,304 bit serial Flash memory, which is configured as 524,288 x 8 internally. The MX25L4005A feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input.

The MX25L4005A provide sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or byte /sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector(4K-bytes) or block(64K-bytes).

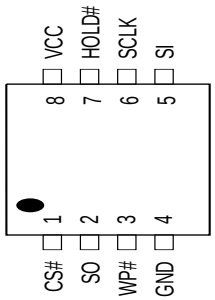
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current.

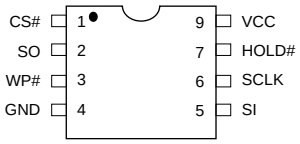
The MX25L4005A utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

PIN CONFIGURATIONS

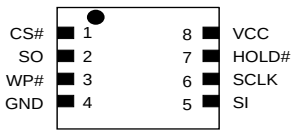
8-PIN SOP (150/200mil)



8-PIN PDIP (300mil)



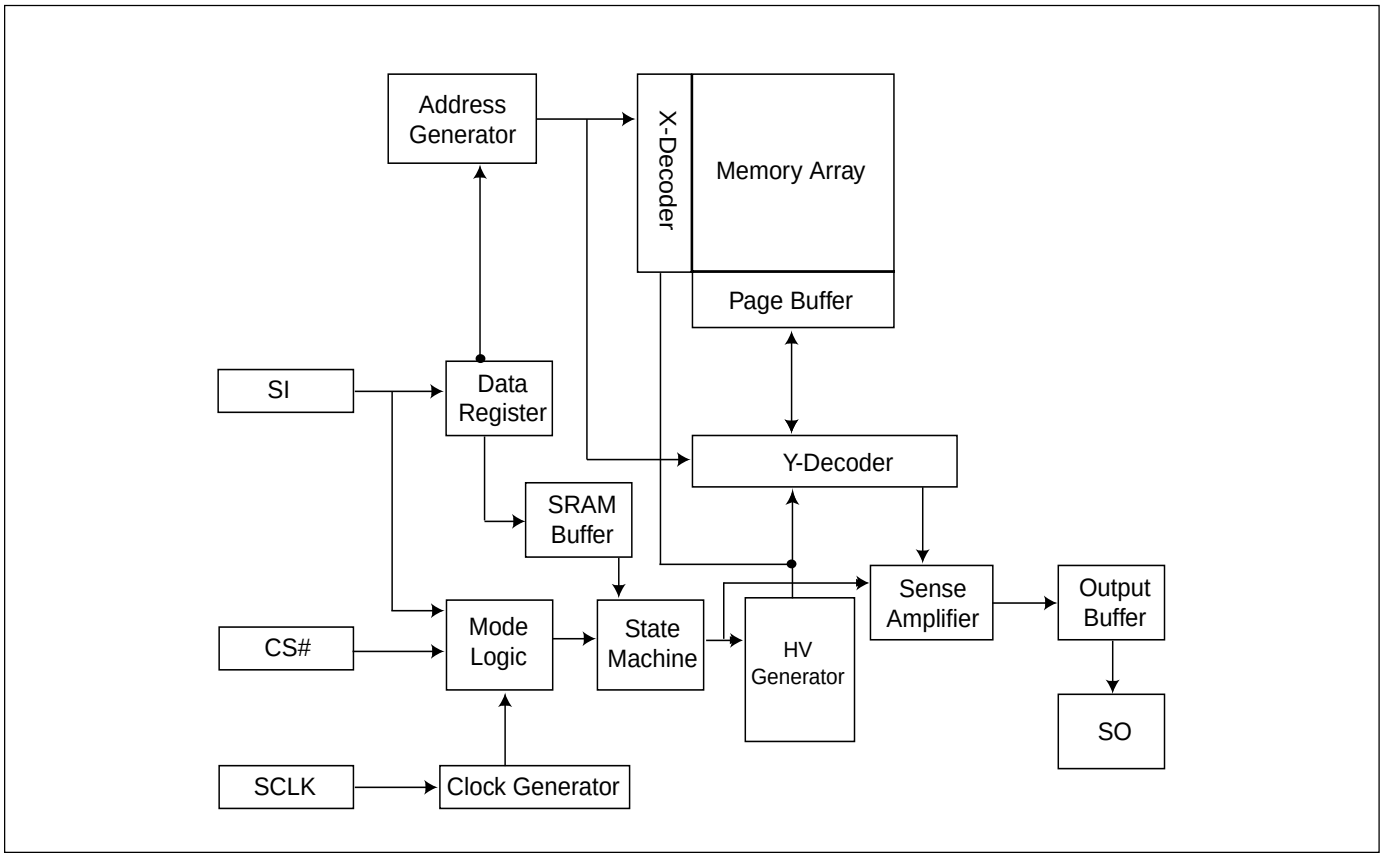
8-LAND SON (6x5mm)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
HOLD#	Hold, to pause the device without deselecting the device
WP#	Write Protection
VCC	+ 3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



DATA PROTECTION

The MX25L4005A are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Software Protection Mode (SPM): by using BP0-BP2 bits to set the part of Flash protected from data change.

- Hardware Protection Mode (HPM): by using WP# going low to protect the BP0-BP2 bits and SRWD bit from data change.

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

Table 1. Protected Area Sizes

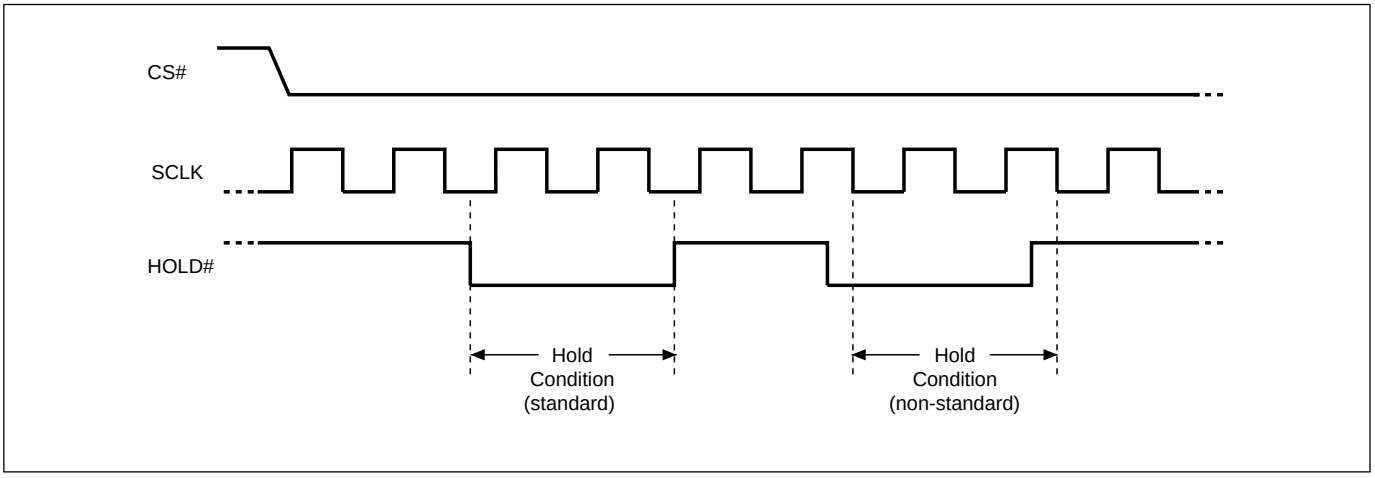
Status bit			Protect level	4Mb
BP2	BP1	BP0		
0	0	0	0 (none)	None
0	0	1	1 (1 block)	Block 7
0	1	0	2 (2 blocks)	Block 6-7
0	1	1	3 (4 blocks)	Block 4-7
1	0	0	4 (8 blocks)	All
1	0	1	5 (All)	All
1	1	0	6 (All)	All
1	1	1	7 (All)	All

HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 1.

Figure 1. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Table 2. COMMAND DEFINITION

COMMAND (byte)	WREN (write Enable)	WRDI (write disable)	RDID (read ident-ification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	Fast Read (fast read data)
1st	06 Hex	04 Hex	9F Hex	05 Hex	01 Hex	03 Hex	0B Hex
2nd						AD1	AD1
3rd						AD2	AD2
4th						AD3	AD3
5th							x
Action	sets the (WEL) write enable latch bit	reset the (WEL) write enable latch bit	output the manufacturer ID and 2-byte device ID	to read out the status register	to write new values to the status register	n bytes read out until CS# goes high	

COMMAND (byte)	SE (Sector Erase)	BE (Block Erase)	CE (Chip Erase)	PP (Page Program)	DP (Deep Power Down)	RDP (Release from Deep Power-down)	RES (Read Electronic ID)	REMS (Read Electronic Manufacturer & Device ID)
1st	20 Hex	52 or D8 Hex	60 or C7 Hex	02 Hex	B9 Hex	AB Hex	AB Hex	90 Hex
2nd	AD1	AD1		AD1			x	x
3rd	AD2	AD2		AD2			x	x
4th	AD3	AD3		AD3			x	ADD(1)
5th								
Action								Output the manufacturer ID and device ID

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

(2) It is not recommended to adopt any other code which is not in the above command definition table.

Table 3. Memory Organization

Block	Sector	Address Range	
7	127	07F000h	07FFFFh
	⋮	⋮	⋮
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	⋮	⋮	⋮
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	⋮	⋮	⋮
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮	⋮	⋮
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮	⋮	⋮
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮	⋮	⋮
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮	⋮	⋮
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮	⋮	⋮
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

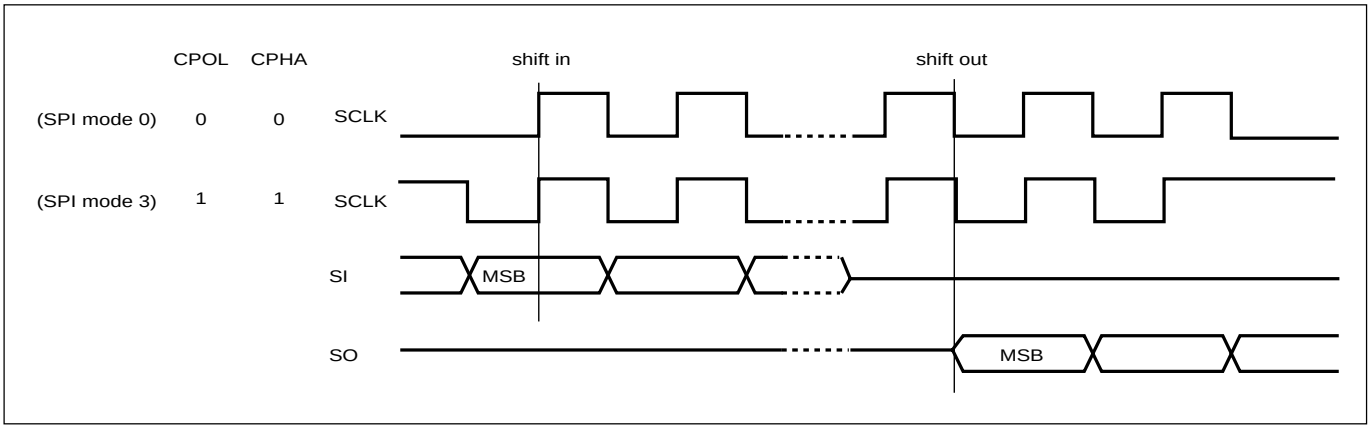
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of SPI mode 0 and mode 3 is shown as Figure 2.

5. For the following instructions: RDID, RDSR, READ, FAST_READ, RES and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP and DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 2. SPI Modes Supported



Note:
CPOL indicates clock polarity of SPI master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which SPI mode is supported.

COMMAND DESCRIPTION

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low-> sending WREN instruction code-> CS# goes high. (see Figure 11)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low-> sending WRDI instruction code-> CS# goes high. (see Figure 12)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as followings: 13(hex) for MX25L4005A.

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data out on SO -> to end RDID operation can use CS# to high at any time during data out. (see Figure. 13)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low-> sending RDSR instruction code-> Status Register data out on SO (see Figure. 14)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in table 1) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed)

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRWD Status Register Write Protect	0	0	BP2 the level of protected block	BP1 the level of protected block	BP0 the level of protected block	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable			(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: 1. See the table "Protected Area Sizes".
2. The endurance cycles of protect bits are 100,000 cycles; however, the tW time out spec of protect bits is relaxed as tW = N x 15ms (N is a multiple of 10,000 cycles, ex. N = 2 for 20,000 cycles) after 10,000 cycles on those bits.

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP2, BP1, BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low-> sending WRSR instruction code-> Status Register data on SI-> CS# goes high. (see Figure 15)

The WRSR instruction has no effect on b6, b5, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 4. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP2 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP2 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM).

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP2, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP2, BP1, BP0.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address on SI -> data out on SO-> to end READ operation can use CS# to high at any time during data out. (see Figure. 16)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low-> sending FAST_READ instruction code-> 3-byte address on SI-> 1-dummy byte address on SI->data out on SO-> to end FAST_READ operation can use CS# to high at any time during data out. (see Figure. 17)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low -> sending SE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 19)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(9) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table 3) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low -> sending BE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 20)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

(10) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low-> sending CE instruction code-> CS# goes high. (see Figure 20)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP2, BP1, BP0 all set to "0".

(11) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low-> sending PP instruction code-> 3-byte address on SI-> at least 1-byte on data on SI-> CS# goes high. (see Figure 18)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(12) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/ Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low-> sending DP instruction code-> CS# goes high. (see Figure 22)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(13) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 6. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new deisng, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 23,24.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(14) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in figure 25. The Device ID values are listed in Table of ID Definitions on page 16. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table of ID Definitions:

RDID Command	manufacturer ID	memory type	memory density
	C2	20	13
RES Command	electronic ID		
	12		
REMS Command	manufacturer ID		device ID
	C2		12

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after VCC reaching the VWI level, a tPUW time delay is required before the device is fully accessible for commands like write enable(WREN), page program (PP), sector erase(SE), chip erase(CE) and write status register(WRSR). If the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tPUW after VCC reached VWI level
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL, even time of tPUW has not passed.
Please refer to the figure of "power-up timing".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C for Industrial grade 0°C to 70°C for Commercial grade
Storage Temperature	-55°C to 125°C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

Notes:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.
4. All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

Figure 3.Maximum Negative Overshoot Waveform

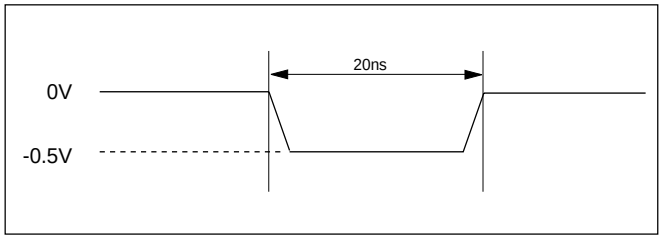
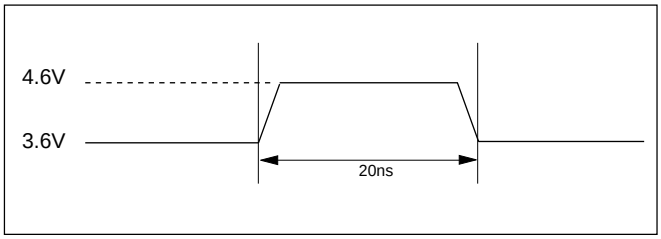


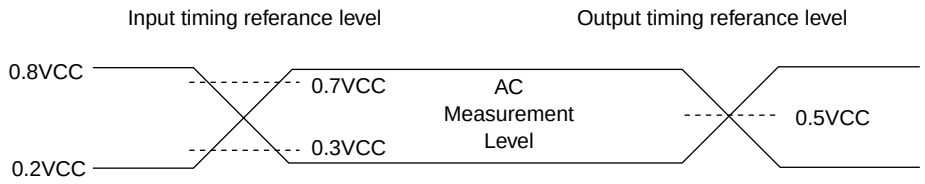
Figure 4. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

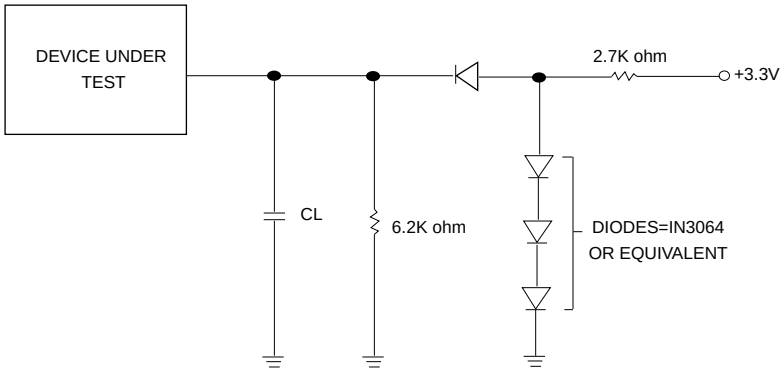
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 5. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <5ns

Figure 6. OUTPUT LOADING



CL=30pF Including jig capacitance
(CL=15pF Including jig capacitance for 85MHz)

Table 5. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current	1			10	uA	VIN = VCC or GND CS# = VCC
ISB2	Deep Power-down Current				10	uA	VIN = VCC or GND CS# = VCC
ICC1	VCC Read	1			12	mA	f=85MHz SCLK=0.1VCC/0.9VCC, SO=Open
					8	mA	f=66MHz SCLK=0.1VCC/0.9VCC, SO=Open
					4	mA	f=33MHz SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1			15	mA	Program in Progress CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current				15	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1			15	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1			15	mA	Erase in Progress CS#=VCC
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 6. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions:		D.C.		85	MHz
		FAST_READ, PP, SE, BE, CE, DP, RES,RDP				(Condition:15pF)	
		WREN, WRDI, RDID, RDSR, WRSR				66	MHz
						(Condition:30pF)	
fRSCLK	fR	Clock Frequency for READ instructions		D.C.		33	MHz
tCH(1)	tCLH	Clock High Time		7			ns
tCL(1)	tCLL	Clock Low Time		7			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tSHSL	tCSH	CS# Deselect Time		100			ns
tSHQZ(2)	tDIS	Output Disable Time				6	ns
tCLQV	tV	Clock Low to Output Valid	@33MHz 30pF			8	ns
			@85MHz 15pF or @66MHz 30pF			6	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		HOLD# Setup Time (relative to SCLK)		5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)		5			ns
tHHCH		HOLD Setup Time (relative to SCLK)		5			ns
tCHHL		HOLD Hold Time (relative to SCLK)		5			ns
tHHQX(2)	tLZ	HOLD to Output Low-Z				6	ns
tHLQZ(2)	tHZ	HOLD# to Output High-Z				6	ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power-down Mode				3	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				3	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				1.8	us
tW		Write Status Register Cycle Time			5	15	ms
tPP		Page Program Cycle Time			1.4	5	ms
tSE		Sector Erase Cycle Time			60	120	ms
tBE		Block Erase Cycle Time			1	2	s
tCE		Chip Erase Cycle Time			3.5	7.5	s

Note:
1. tCH + tCL must be greater than or equal to 1/ fC
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 3.

Table 7. Power-Up Timing and VWI Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	10		us
tPUW(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Write Inhibit Voltage	1.5	2.5	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Figure 7. Serial Input Timing

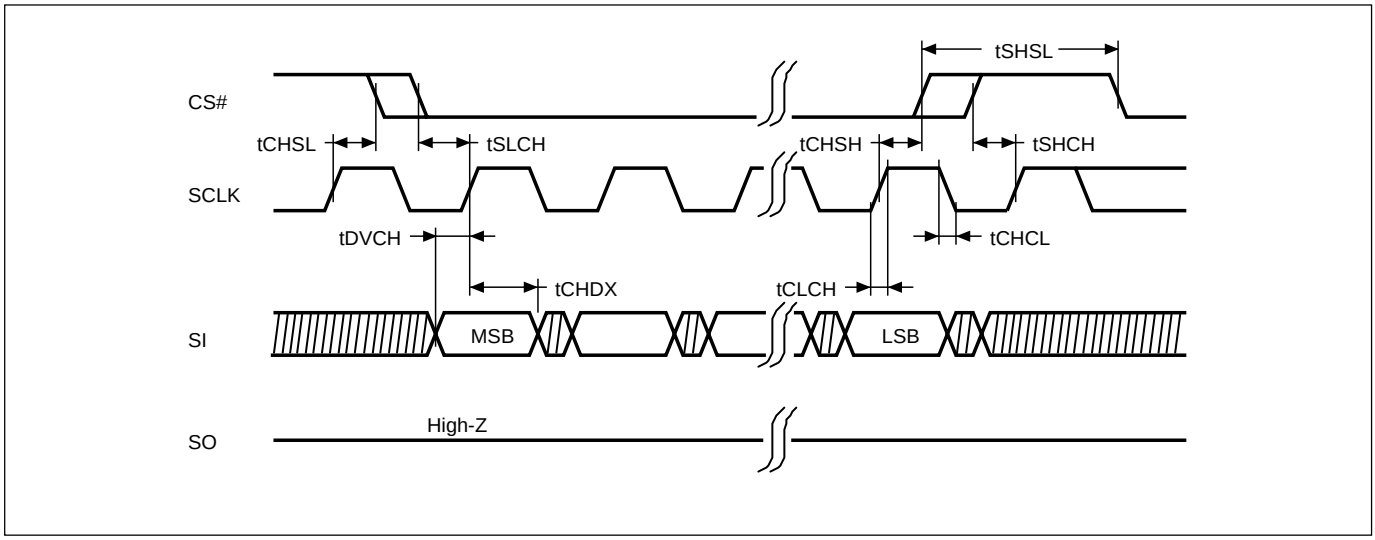


Figure 8. Output Timing

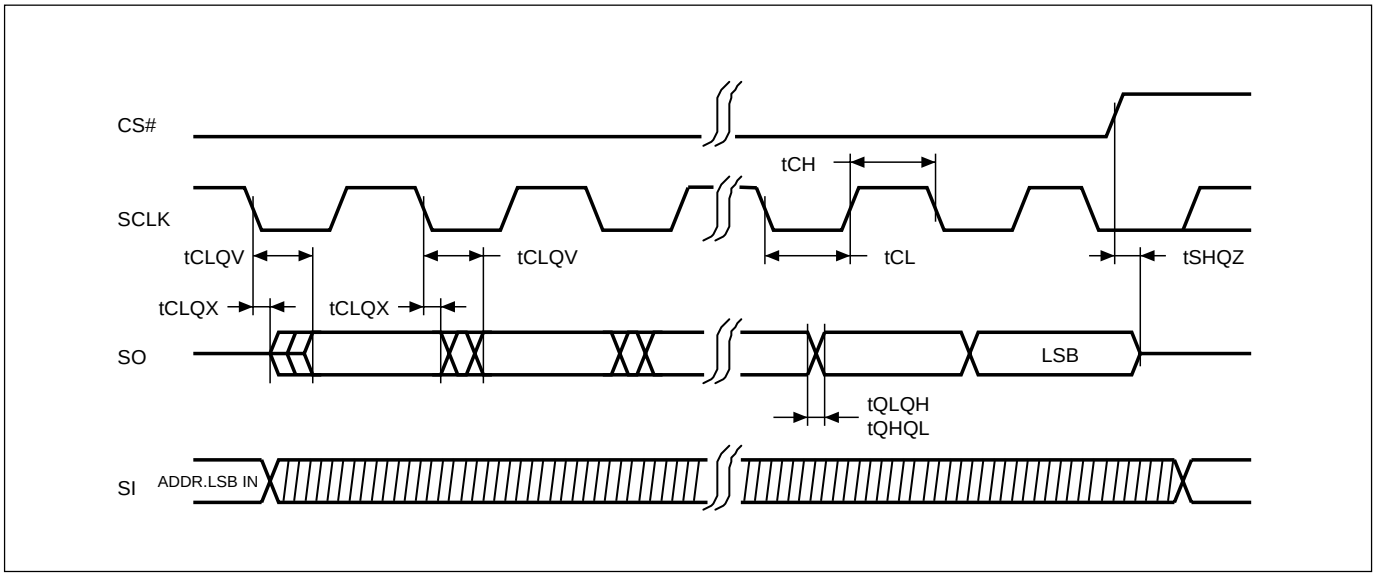
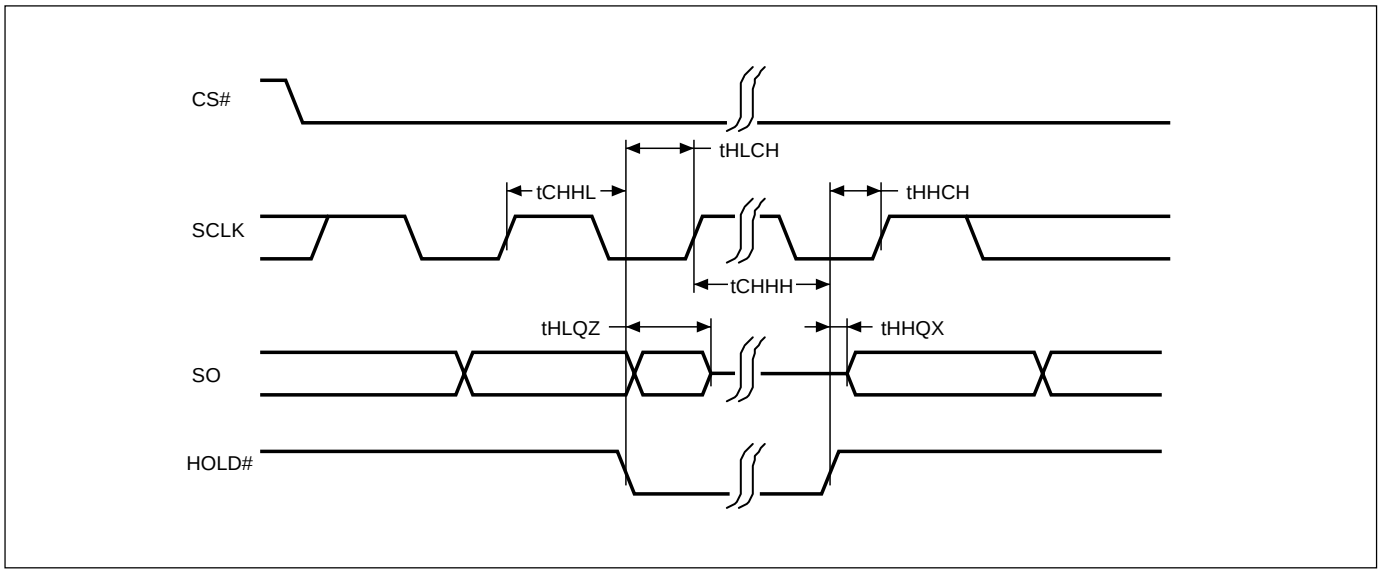


Figure 9. Hold Timing



* SI is "don't care" during HOLD operation.

Figure 10. WP# Disable Setup and Hold Timing during WRSR when SRWD=1

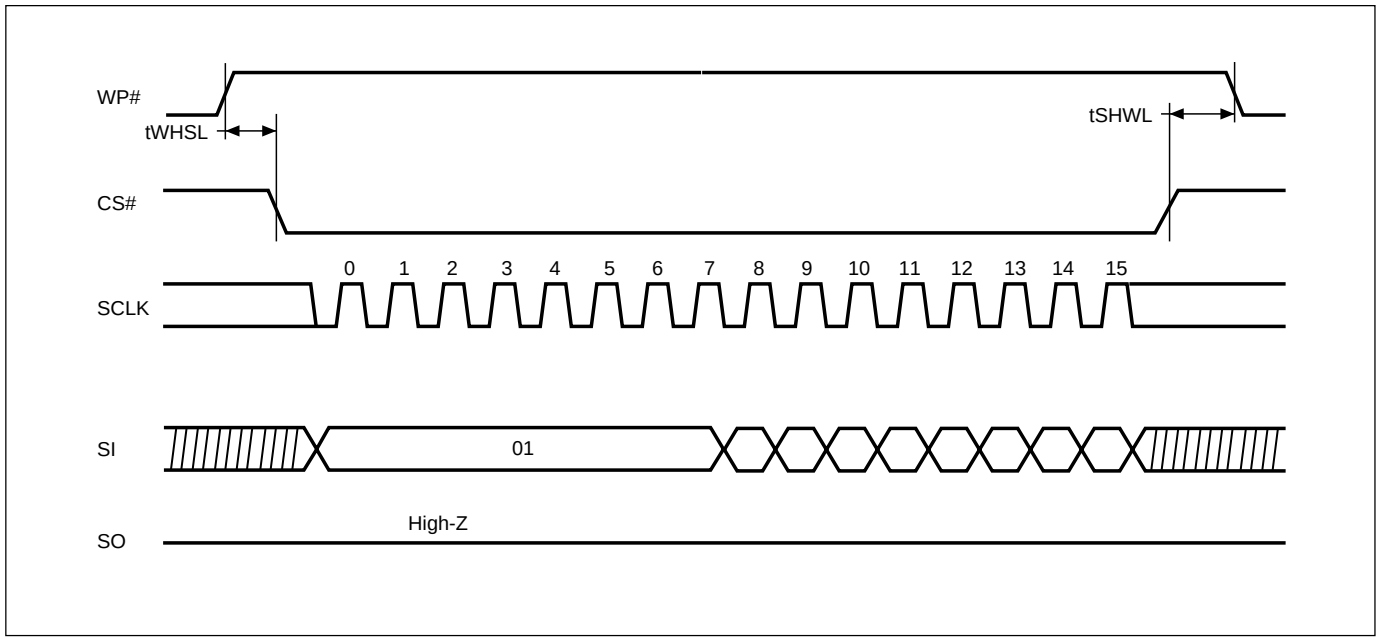


Figure 11. Write Enable (WREN) Sequence (Command 06)

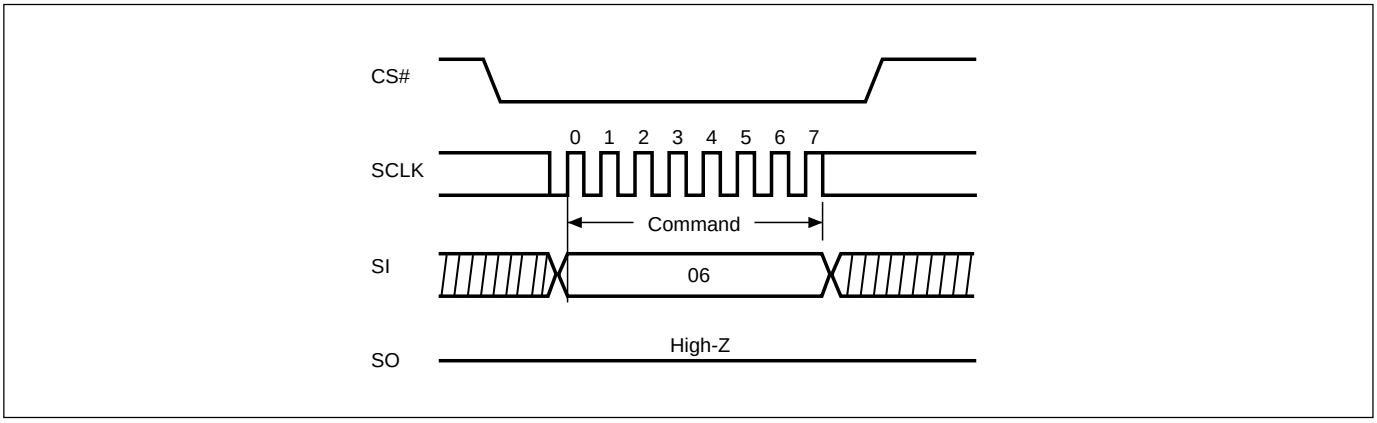


Figure 12. Write Disable (WRDI) Sequence (Command 04)

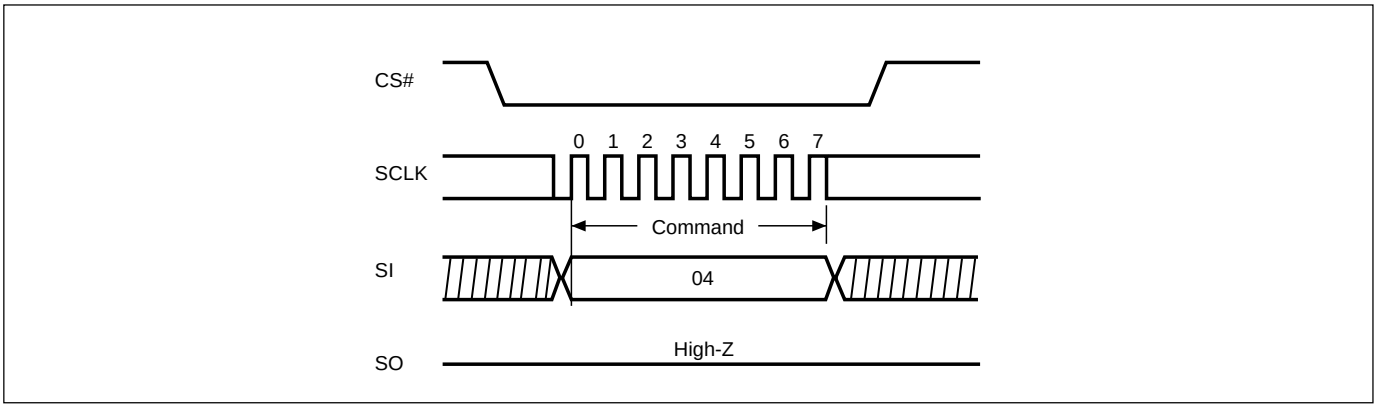


Figure 13. Read Identification (RDID) Sequence (Command 9F)

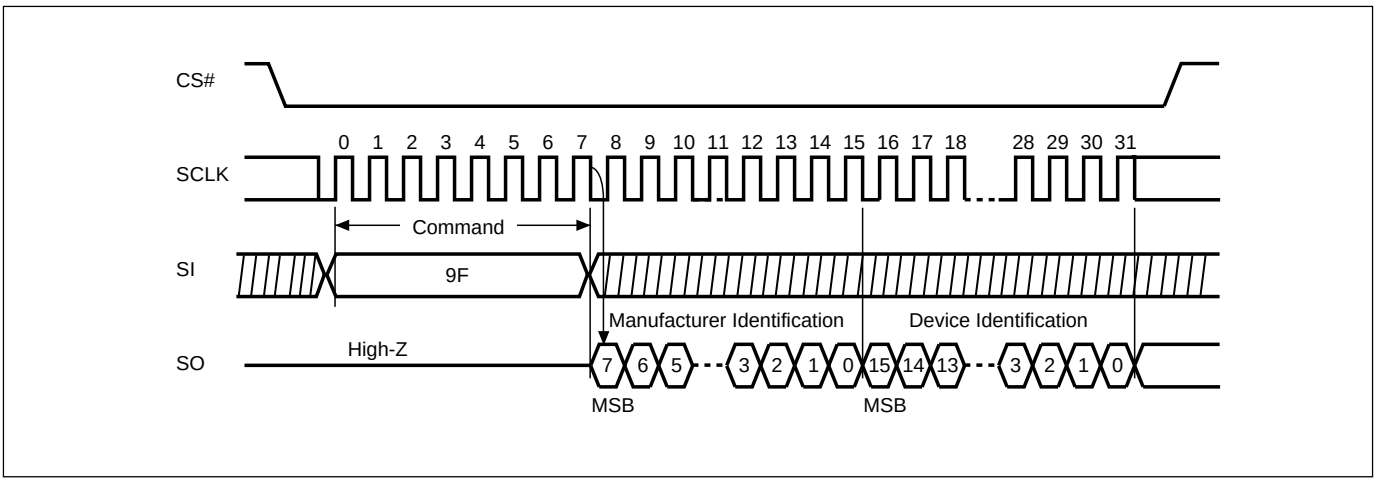


Figure 14. Read Status Register (RDSR) Sequence (Command 05)

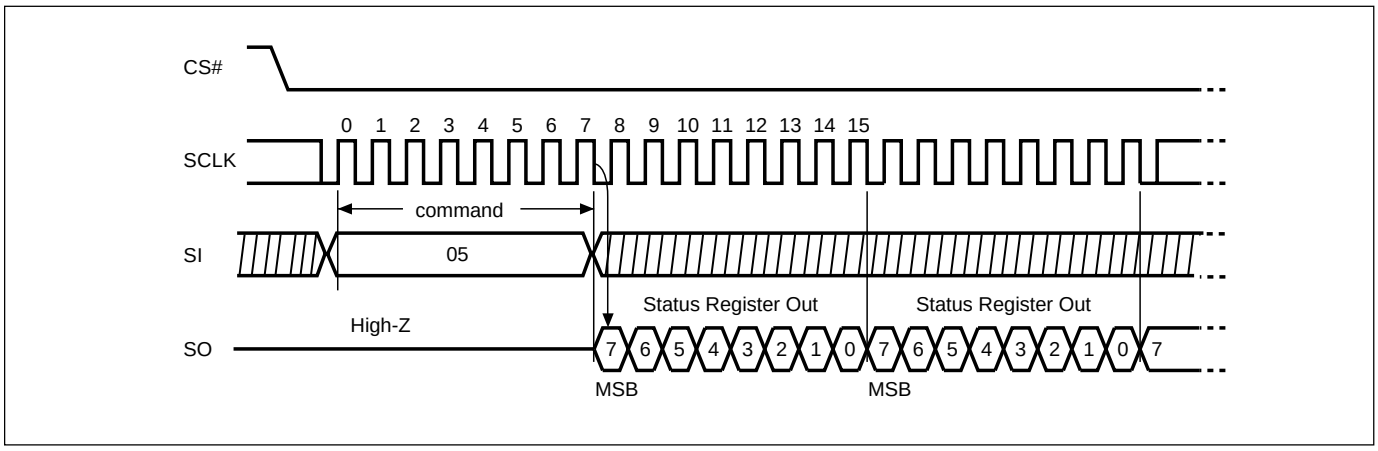


Figure 15. Write Status Register (WRSR) Sequence (Command 01)

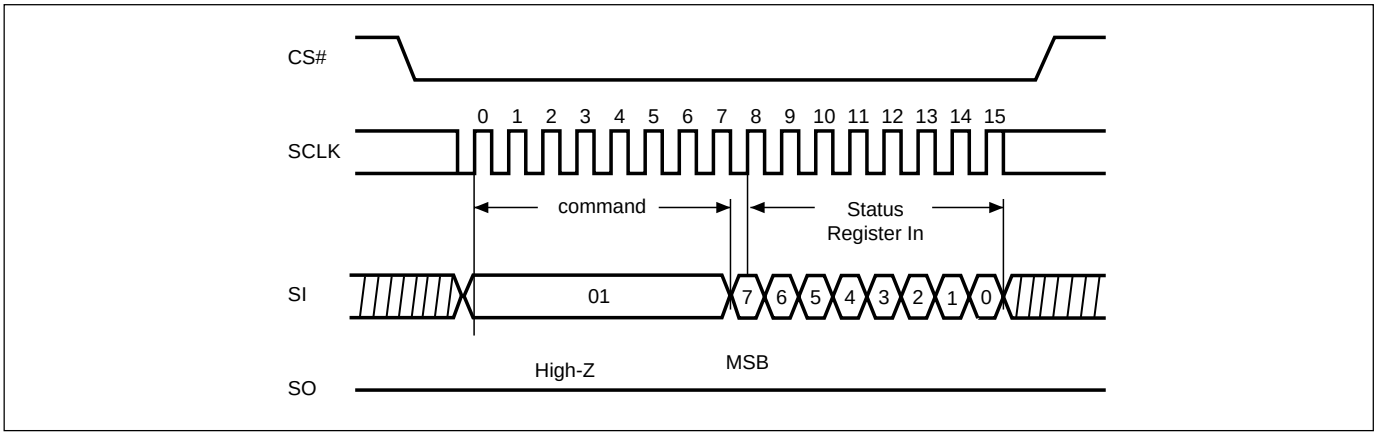


Figure 16. Read Data Bytes (READ) Sequence (Command 03)

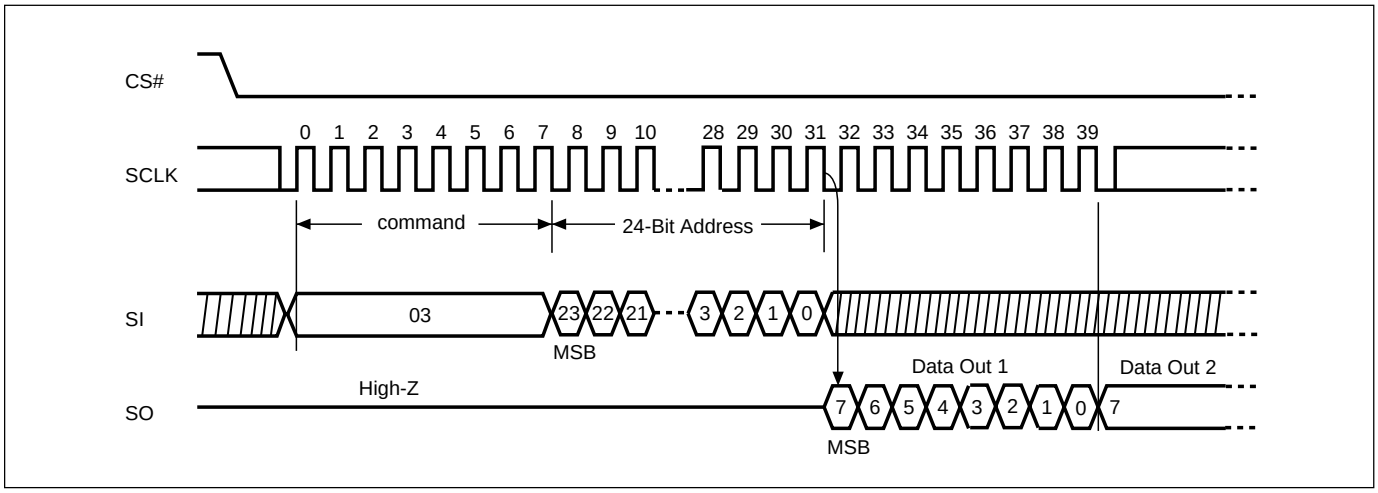


Figure 17. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

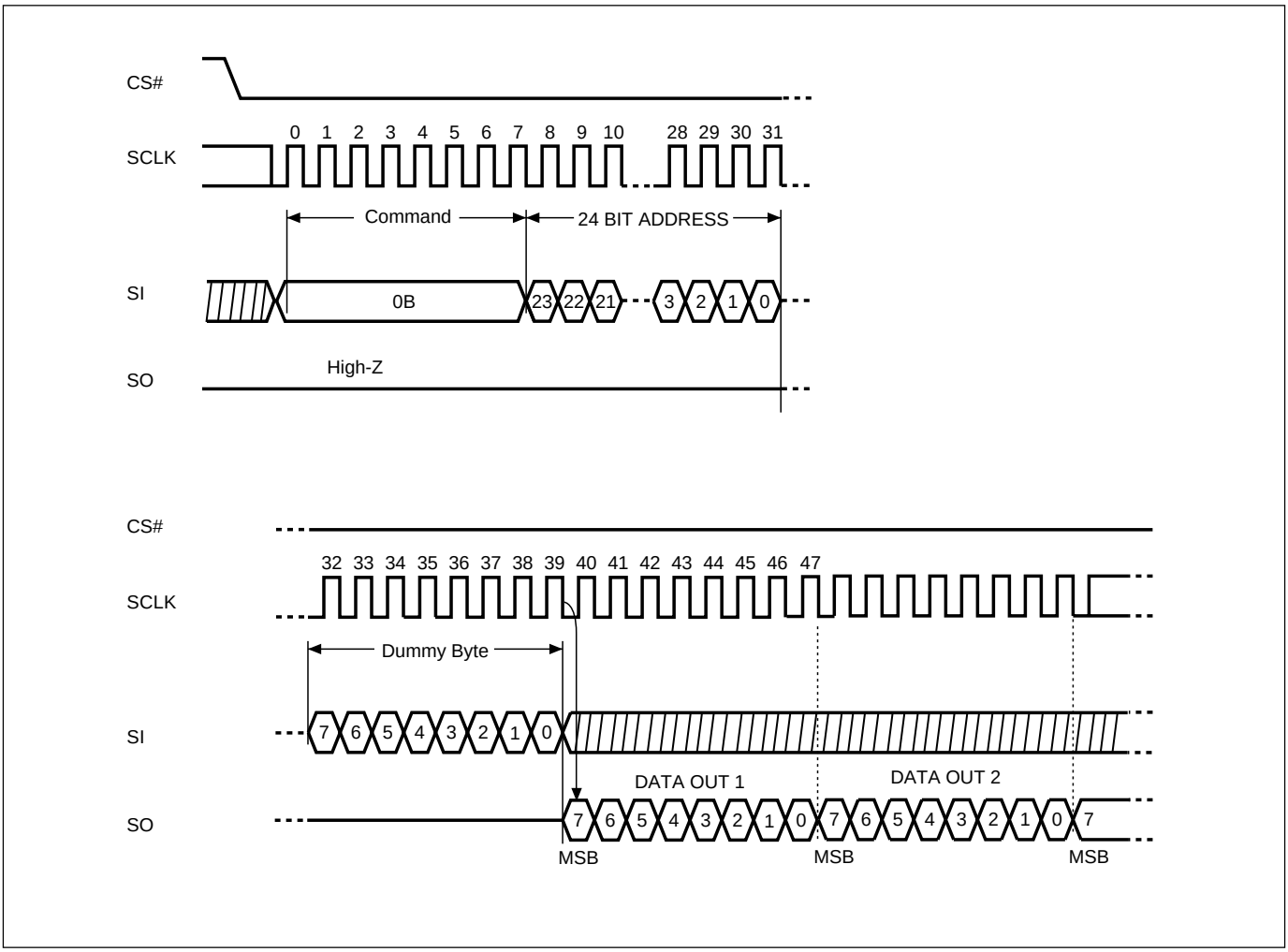


Figure 18. Page Program (PP) Sequence (Command 02)

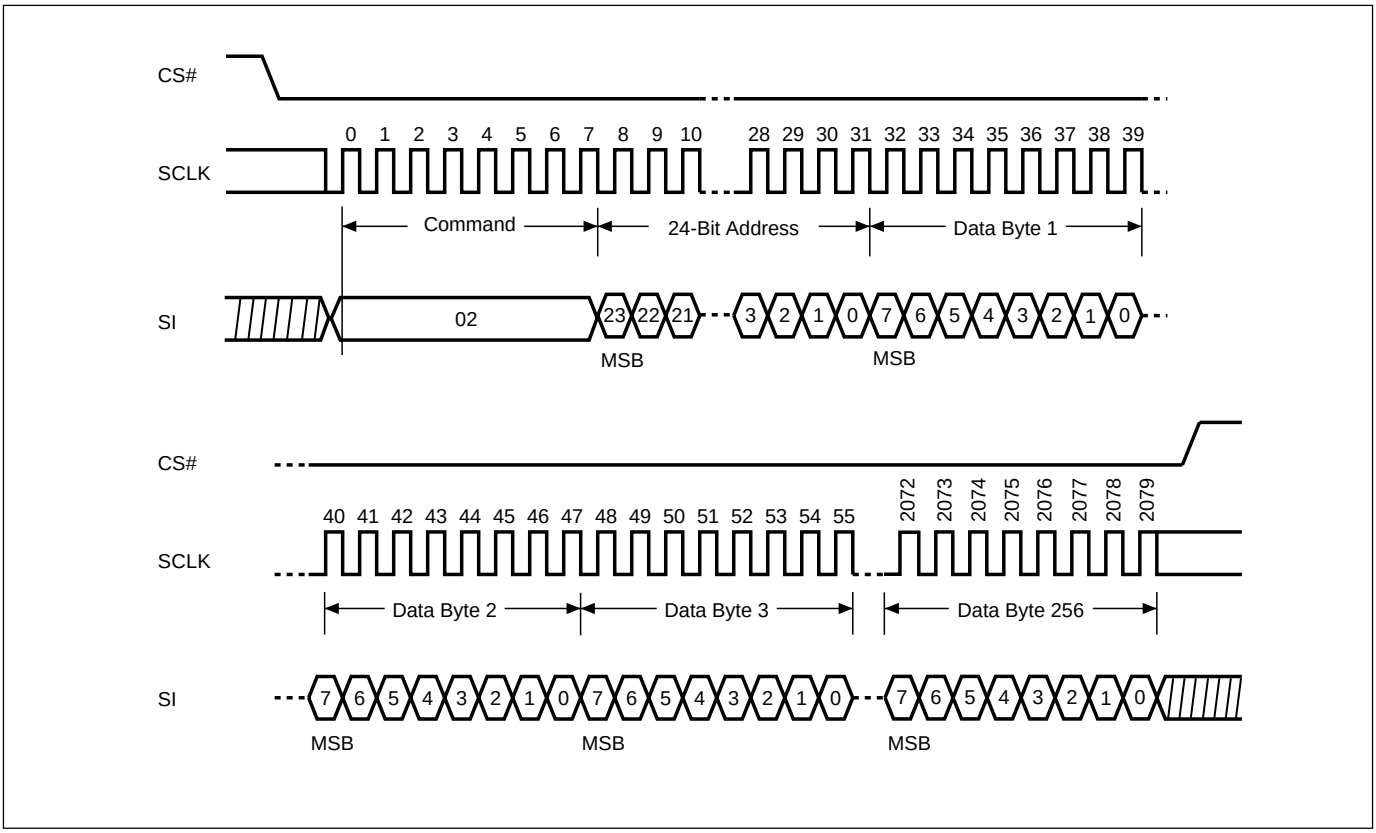
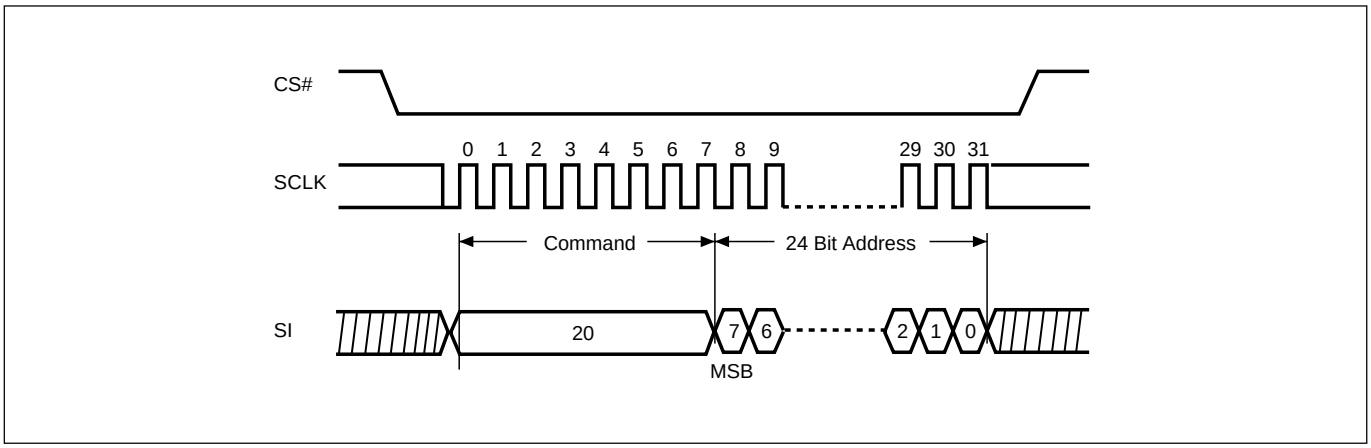
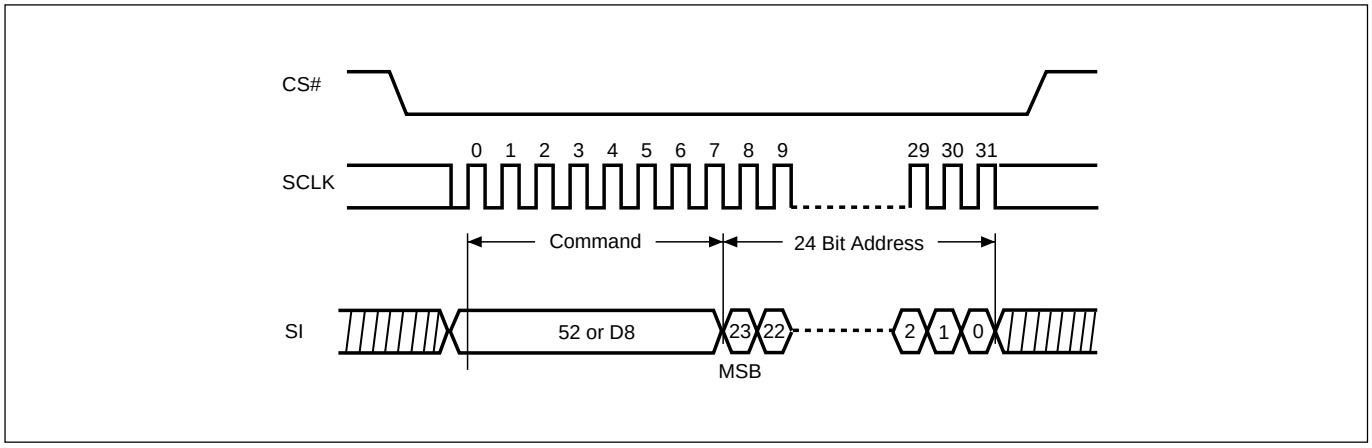


Figure 19. Sector Erase (SE) Sequence (Command 20)



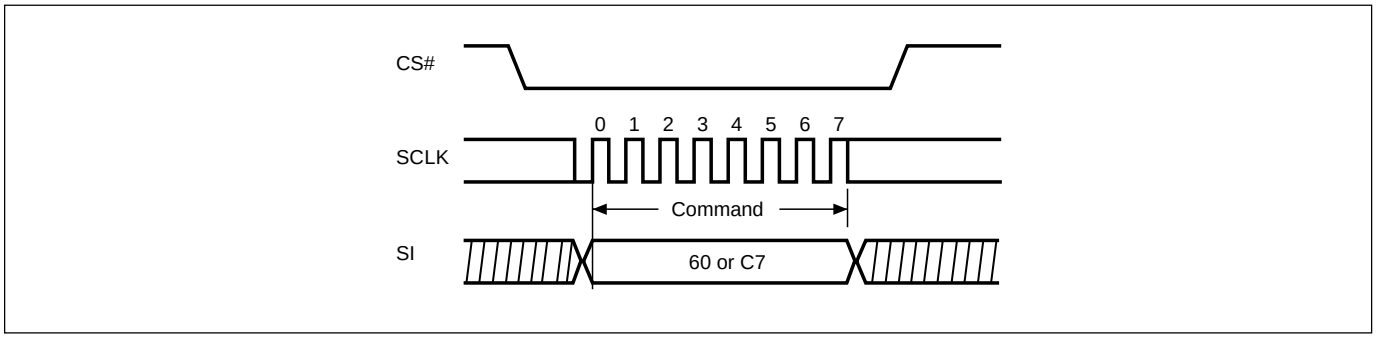
Note: SE command is 20(hex).

Figure 20. Block Erase (BE) Sequence (Command 52 or D8)



Note: BE command is 52 or D8(hex).

Figure 21. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 22. Deep Power-down (DP) Sequence (Command B9)

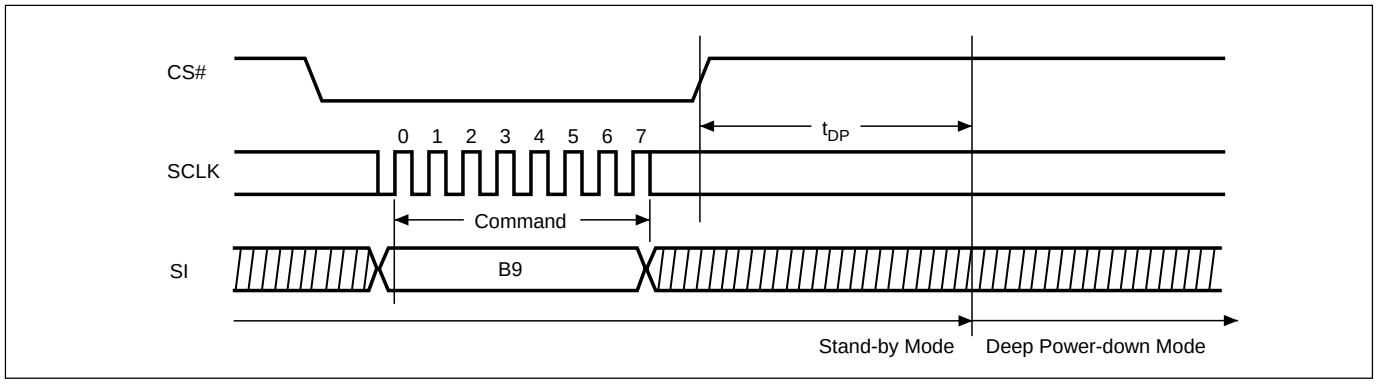


Figure 23. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

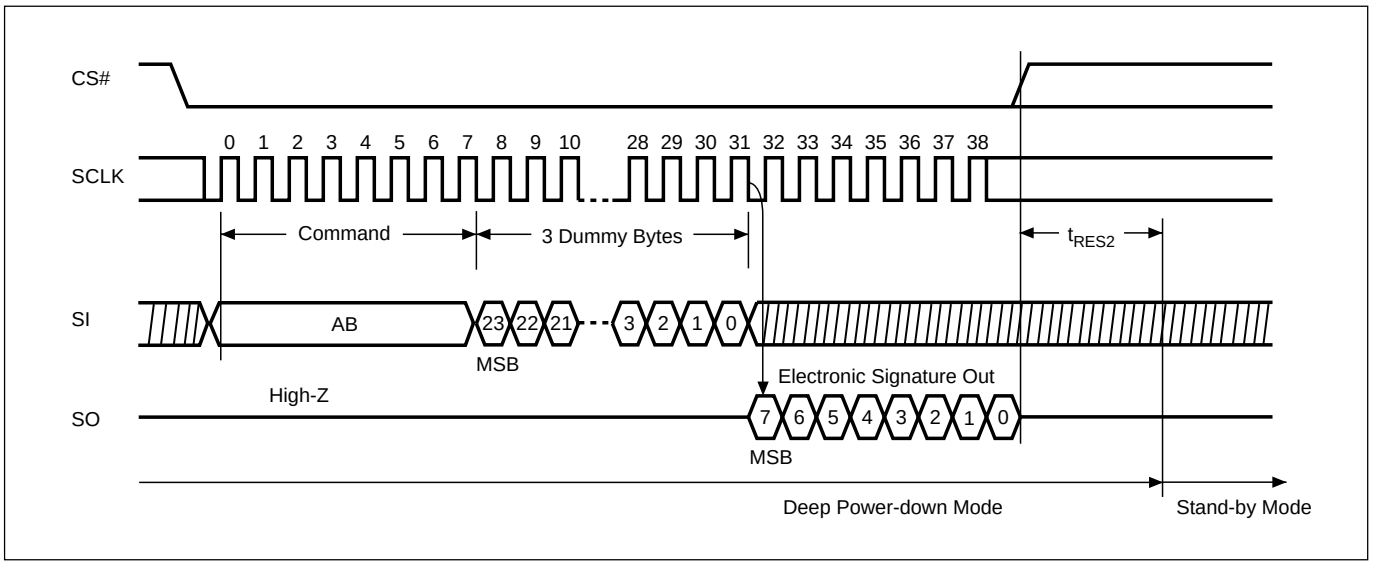


Figure 24. Release from Deep Power-down (RDP) Sequence (Command AB)

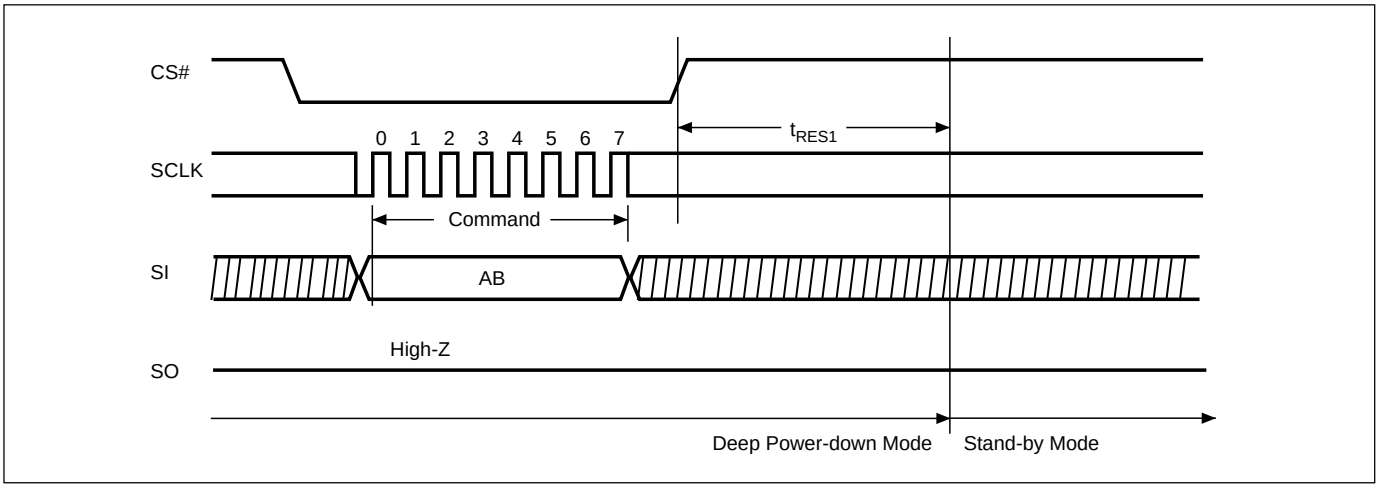
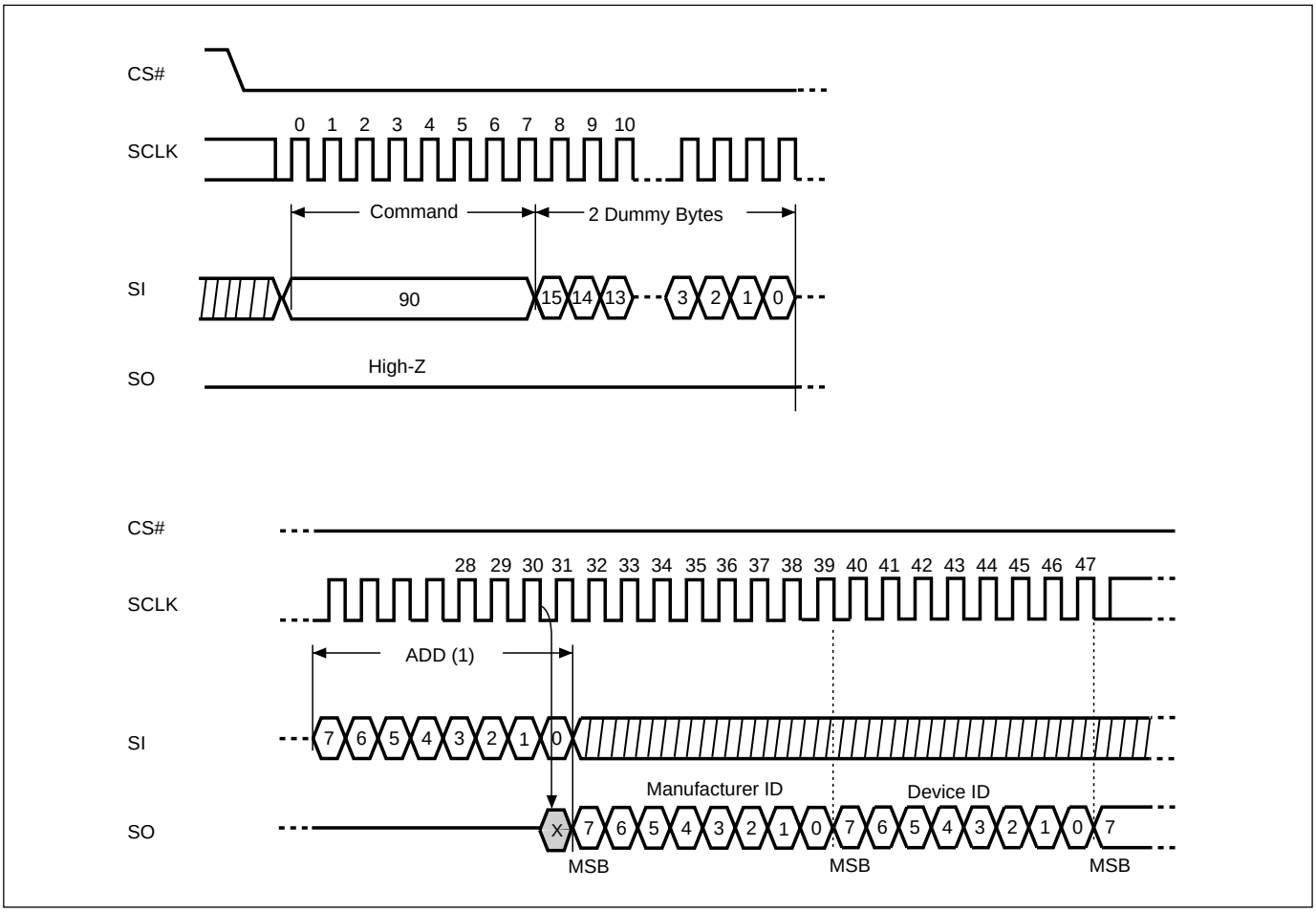


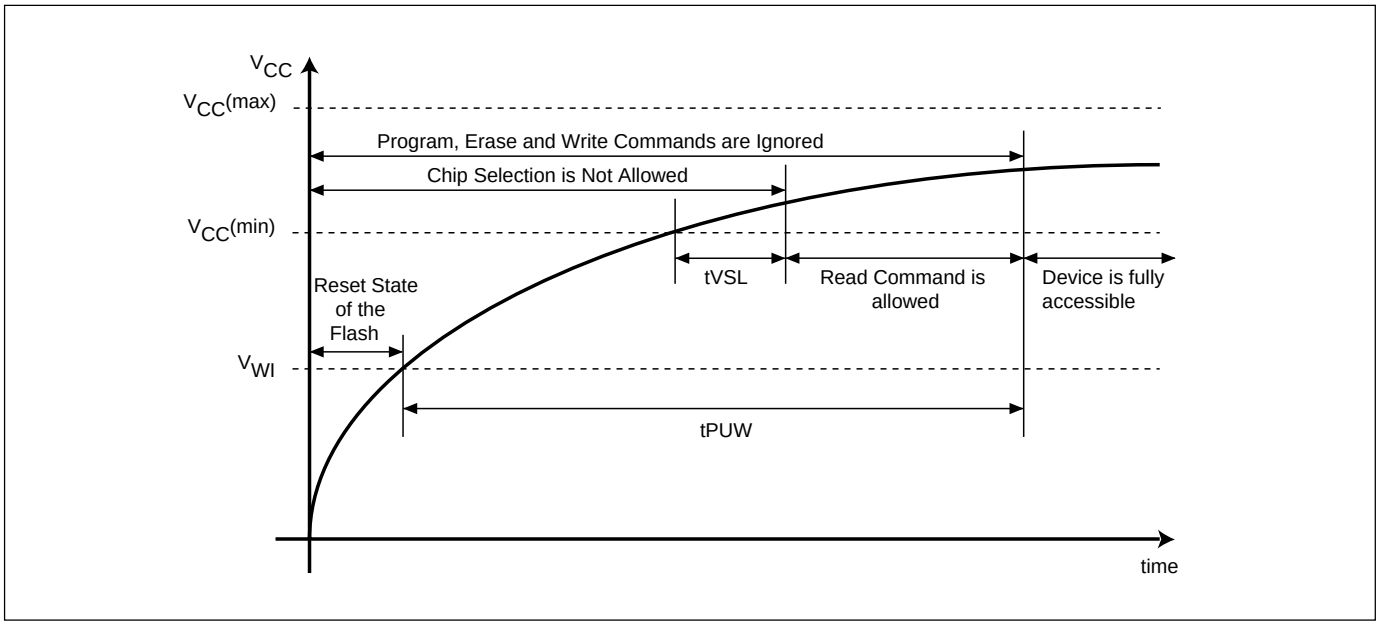
Figure 25. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)



Notes:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

Figure 26. Power-up Timing



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

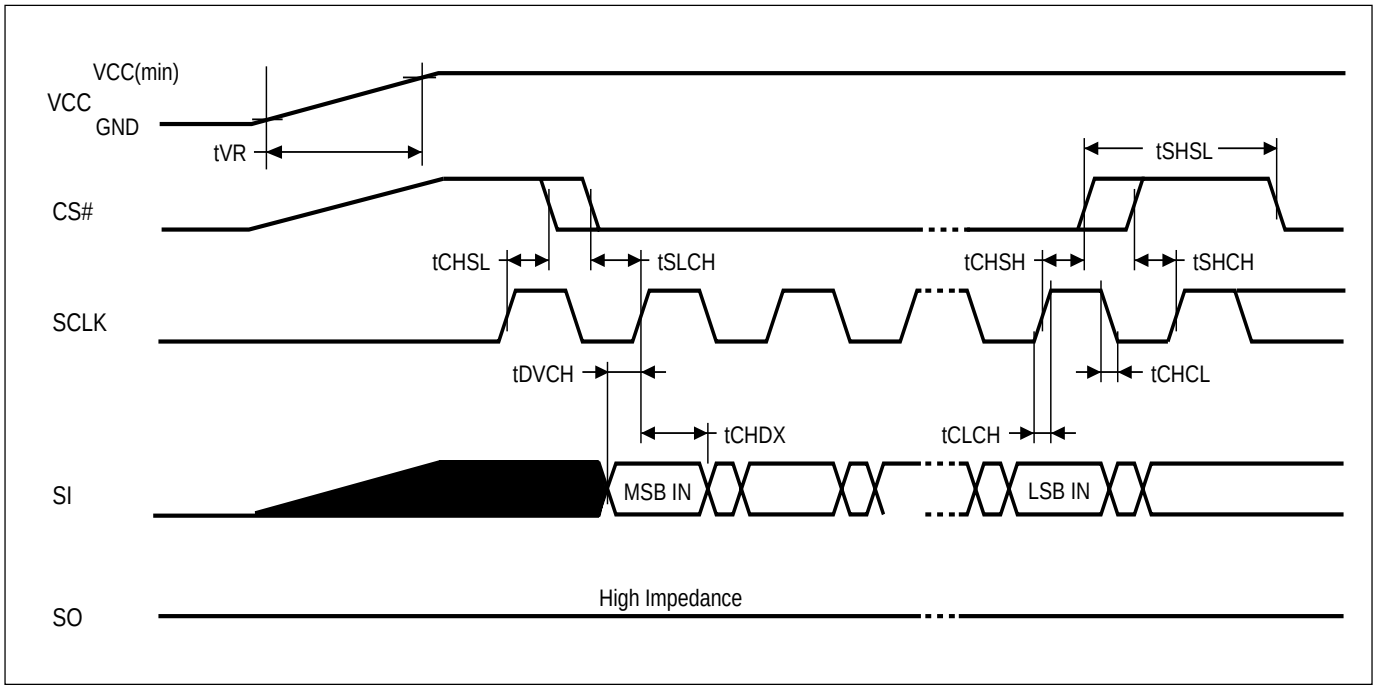


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	0.5	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time		5	15	ms
Sector erase Time		60	120	ms
Block erase Time		1	2	s
Chip Erase Time		3.5	7.5	s
Page Program Time		1.4	5	ms
Erase/Program Cycle	100,000			cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 70°C and 3.0V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0C, VCC=3.0V, and 100K cycle with 90% confidence level.

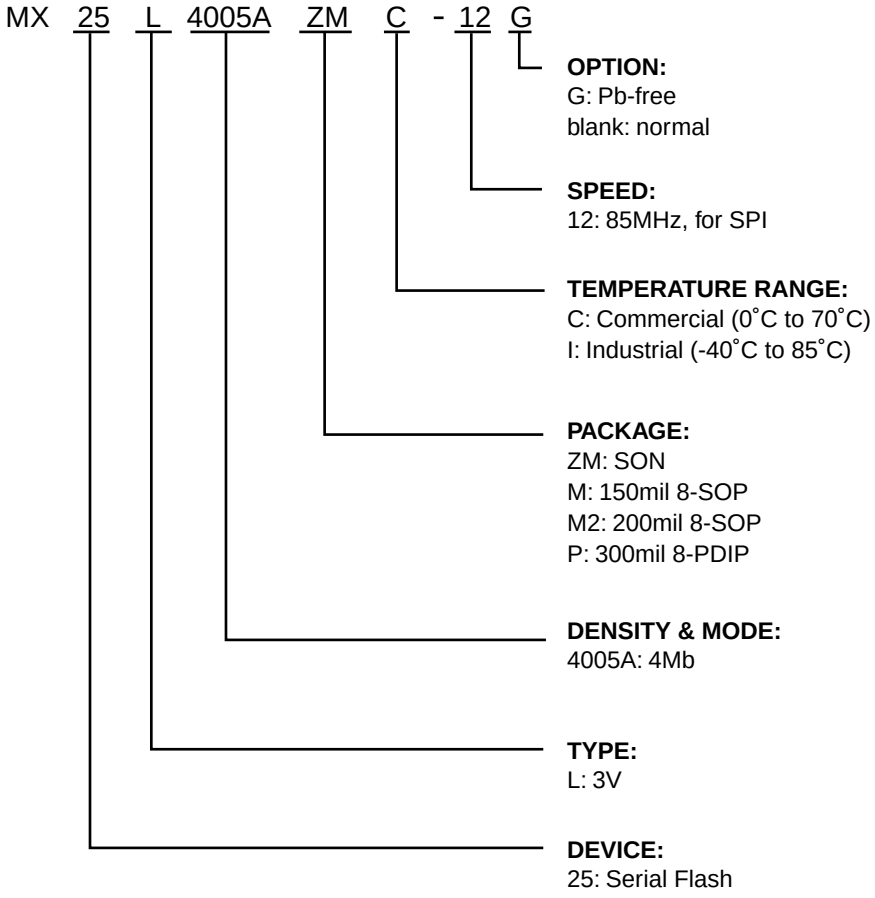
LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on ACC	-1.0V	12.5V
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

ORDERING INFORMATION

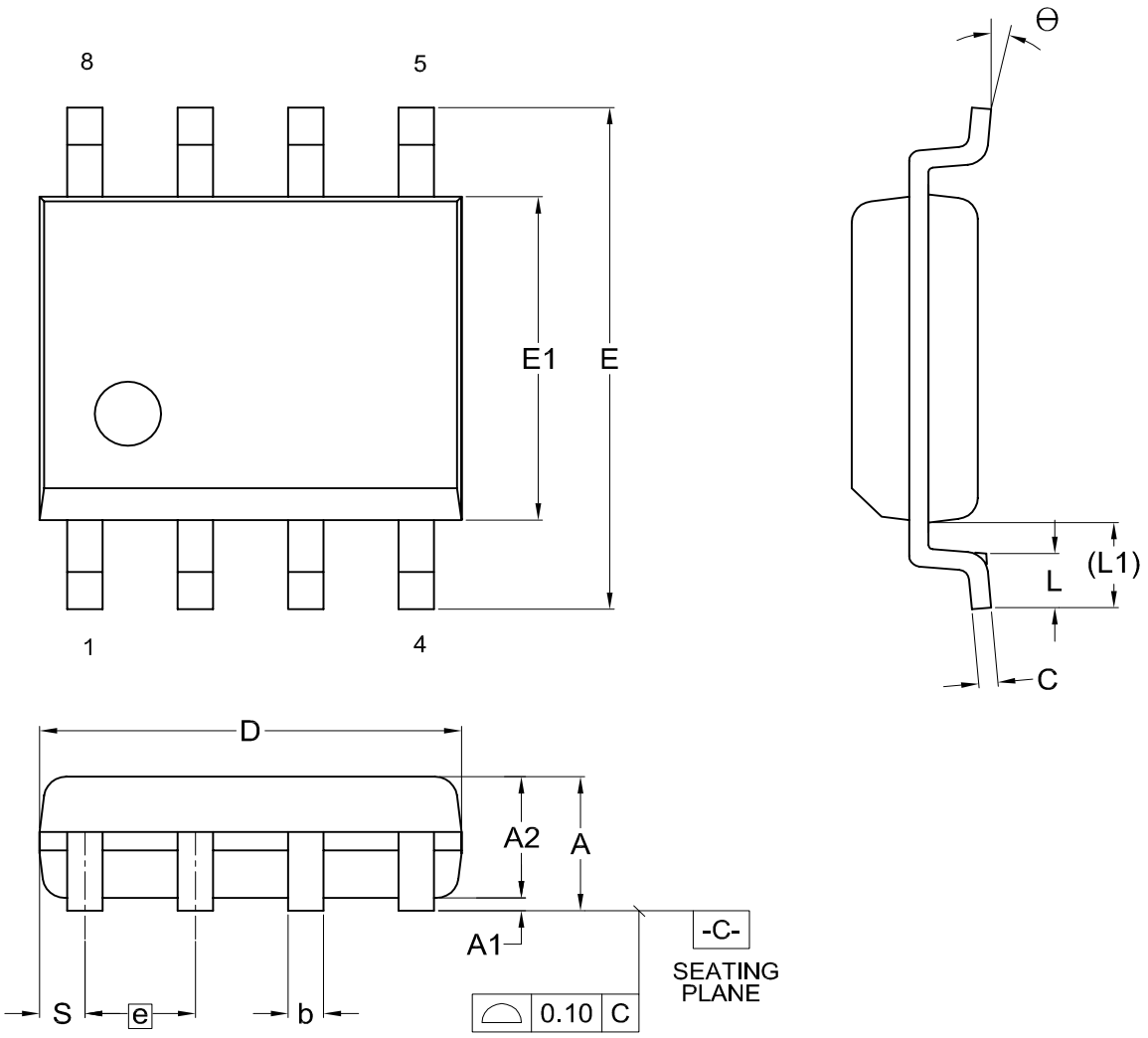
PART NO.	CLOCK (MHz)	OPERATING CURRENT(mA)	STANDBY CURRENT(uA)	Temperature	PACKAGE	Remark
MX25L4005AMC-12	85	12	10	0~70°C	8-SOP (150mil)	
MX25L4005AMC-12G	85	12	10	0~70°C	8-SOP (150mil)	Pb-free
MX25L4005AM2C-12	85	12	10	0~70°C	8-SOP (200mil)	
MX25L4005AM2C-12G	85	12	10	0~70°C	8-SOP (200mil)	Pb-free
MX25L4005APC-12G	85	12	10	0~70°C	8-PDIP (300mil)	Pb-free
MX25L4005AZMC-12G	85	12	10	0~70°C	8-land SON (6x5mm)	Pb-free
MX25L4005AMI-12	85	12	10	-40~85°C	8-SOP (150mil)	
MX25L4005AMI-12G	85	12	10	-40~85°C	8-SOP (150mil)	Pb-free
MX25L4005AM2I-12	85	12	10	-40~85°C	8-SOP (200mil)	
MX25L4005AM2I-12G	85	12	10	-40~85°C	8-SOP (200mil)	Pb-free
MX25L4005AZMI-12G	85	12	10	-40~85°C	8-land SON (6x5mm)	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for SOP 8L (150MIL)

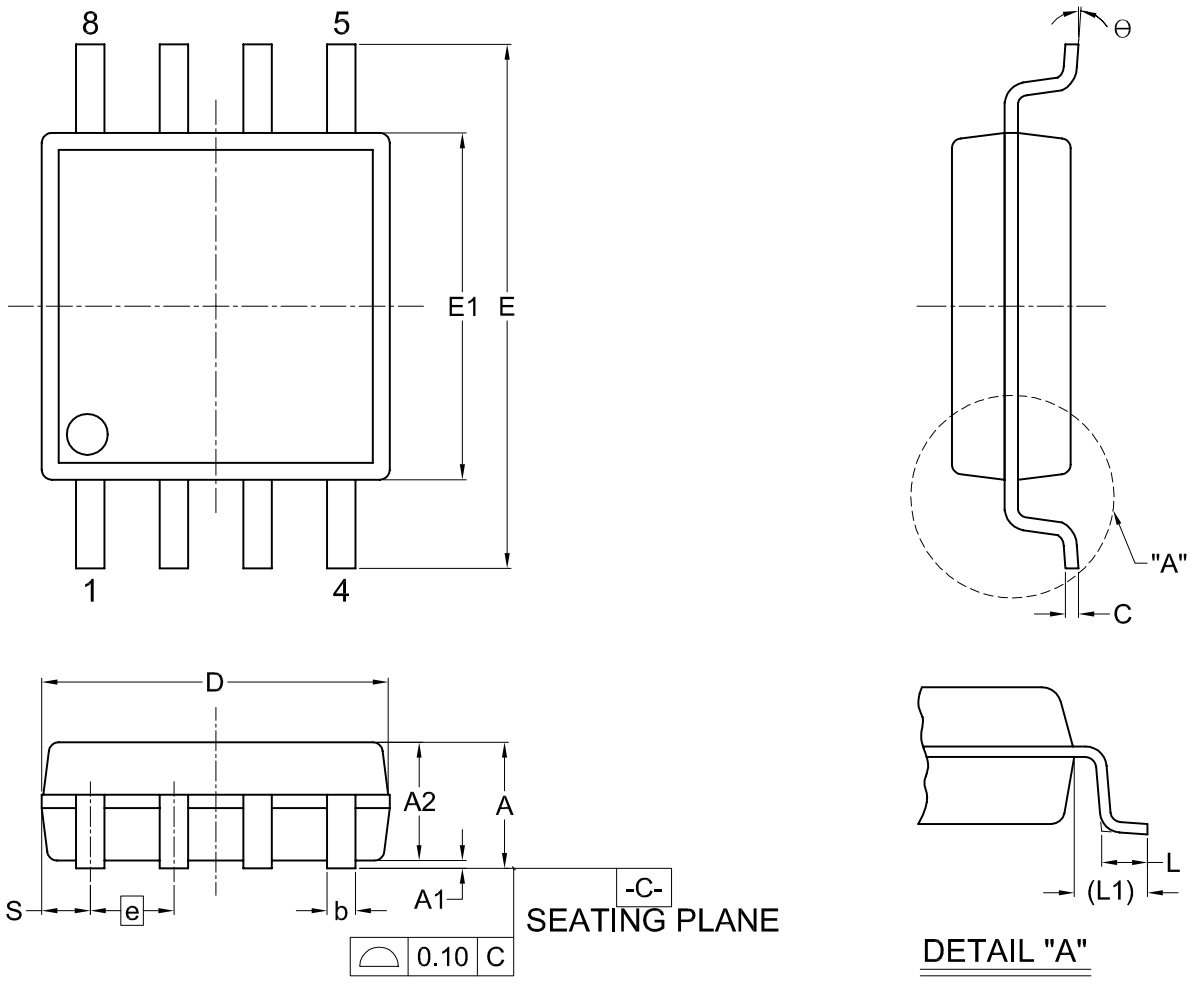


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80		0.46	0.85	0.41	0
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00		0.86	1.25	0.67	8
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150		0.018	0.033	0.016	0
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158		0.034	0.049	0.026	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1401	6	MS-012			11-26-'03

Title: **Package Outline for SOP 8L 200MIL (official name - 209MIL)**

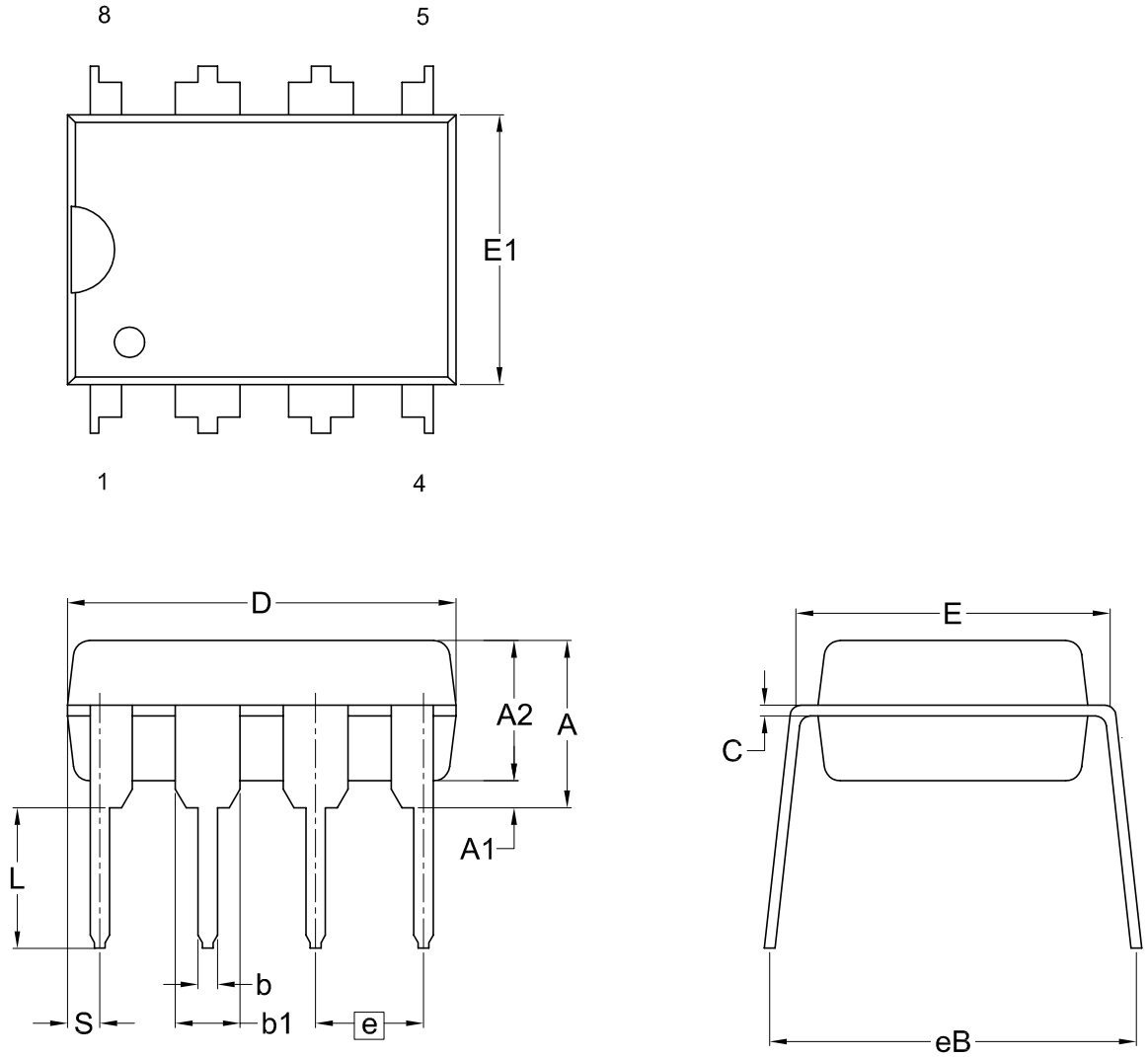


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18		0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204		0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.009	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.031	0.056	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1406	1				05-06-'05

Title: Package Outline for PDIP 8L (300MIL)

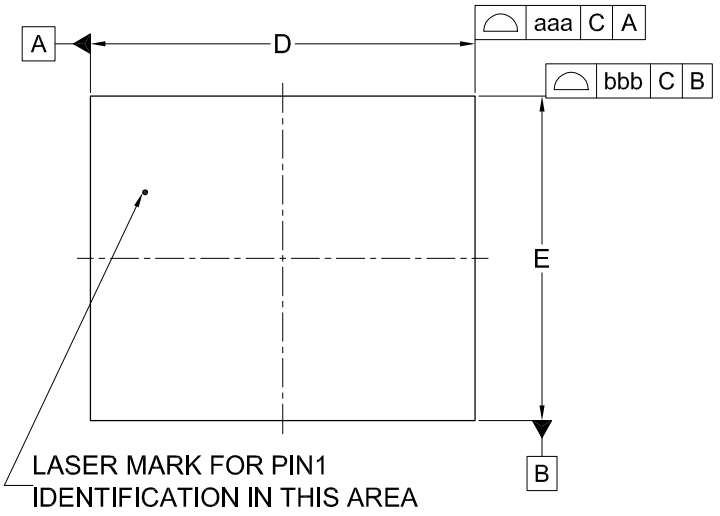


Dimensions (inch dimensions are derived from the original mm dimensions)

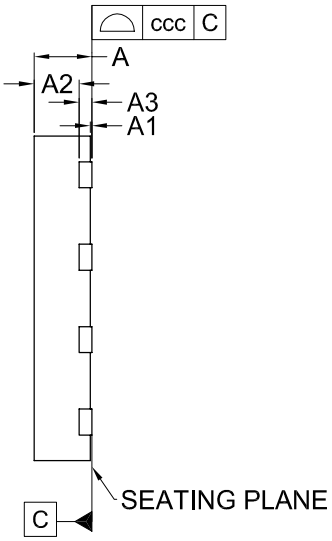
SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	--	0.38	3.18	0.36	1.14	0.20	9.02	7.62	6.22	—	7.87	2.92	0.76
	Nom.	--	--	3.30	0.46	1.52	0.25	9.27	7.87	6.35	2.54	8.89	3.30	1.14
	Max.	5.33	--	3.43	0.56	1.78	0.36	10.16	8.13	6.48	—	9.53	3.81	1.52
Inch	Min.	---	0.015	0.125	0.014	0.045	0.008	0.355	0.300	0.245	—	0.310	0.115	0.030
	Nom.	---	--	0.130	0.018	0.060	0.010	0.365	0.310	0.250	0.100	0.350	0.130	0.045
	Max.	0.210	--	0.135	0.022	0.070	0.014	0.400	0.320	0.255	—	0.375	0.150	0.060

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0201	6	MS-001			09-01-'06

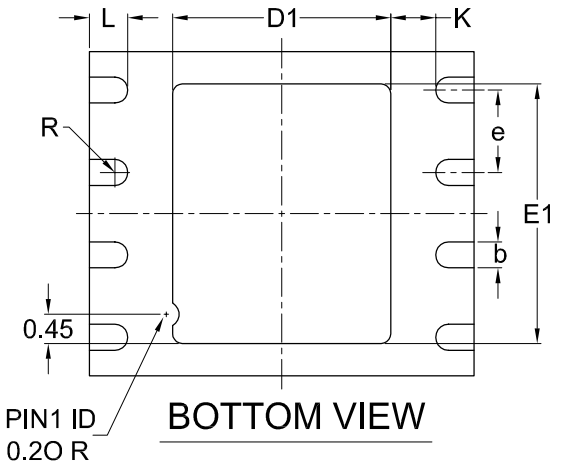
Title: Package Outline for SON 8L (6x5x1.0MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimensions (inch dimensions are derived from the original mm dimensions)

*1 : The exposed pad size must not violate the minimum metal separation requirement (K).

SYMBOL / UNIT		A	A1	A2	A3	b	D	D1	E	E1	L	e	R	K	aaa	bbb	ccc
mm	Min.	---	---	---	---	0.35	5.90	0.00	4.90	0.00	0.50	---	0.175	0.20	---	---	---
	Nom.	---	---	0.65	0.20	0.40	6.00	*1	5.00	*1	0.60	1.27	---	---	0.10	0.10	0.05
	Max.	1.00	0.05	0.70	---	0.48	6.10		5.10		0.75	---	---	---	---	---	---
Inch	Min.	---	---	---	---	0.013	0.232	0.000	0.193	0.000	0.020	---	0.007	0.008	---	---	---
	Nom.		---	0.026	0.008	0.016	0.236	*1	0.197	*1	0.024	0.05	---	---	0.004	0.004	0.002
	Max.	0.039	0.002	0.028	---	0.019	0.240		0.201		0.030	---	---	---	---	---	---

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3302	4	MO-220			05-30-'05

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Modified read current:6mA@85MHz/4mA@66MHz/2mA@33MHz --> 12mA@85MHz/8mA@66MHz/4mA@33MHz	P1,20,35	SEP/29/2005
	2. Modified tSE:90ms(typ)/270ms(max)-->60ms(typ)/120ms(max) ; tBE:3s(max)-->2s(max); tCE:4.5s(typ)/10s(max)-->3.5s(typ)/7.5s(max)	P1,21,34	
	3. Modified operating current max. from 2mA to 12mA	P33	
	4. Added description about Pb-free device is RoHS compliant	P1	
	5. Standby current is reduced from 25uA(max) to 10uA(max)	P1,2,20,35	
	6. Deep Power-down current from 5uA to 10uA	P20	
1.2	1. Format change	All	JUN/08/2006
	2. Supplemented the footnote for tW of protect/unprotect bits	P11	
1.3	1. Added 8-pin PDIP package option	P1,2,35,36,39	SEP/06/2006

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