MX23C4100

4M-BIT [512K x 8/256K x 16] MASK ROM

FEATURES

- Switchable organization
  - 512K x 8 (byte mode)
  - 256K x 16 (word mode)
- Single +5V power supply
- Fast access time:100/120/150ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package
  - 40 pin DIP (600 mil)
  - 40 pin SOP

GENERAL DESCRIPTION

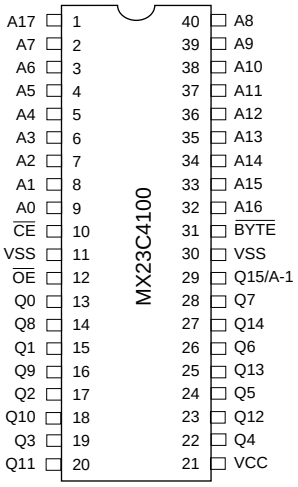
The MX23C4100 is a 5V only, 4M-bit, Read Only Memory. It is organized as 512Kx8 bits (byte mode) or as 256Kx16 bit (word mode) depending on $\overline{BYTE}$ (pin 31) voltage level. MX23C4100 has a static standby mode, and has an access time of 100/120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C4100 offers automatic power-down, with power-down controlled by the chip enable ($\overline{CE}$) input. When $\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ stays in the unselected mode.

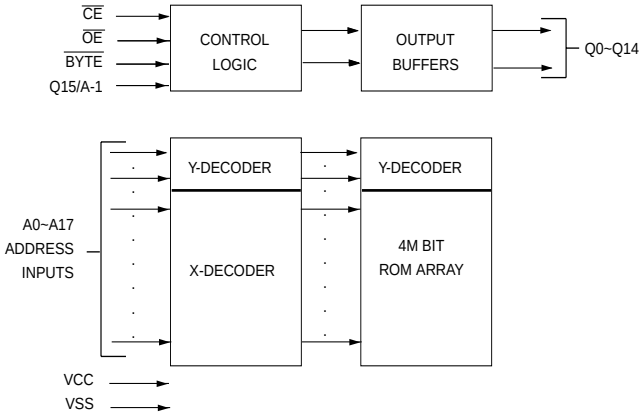
The $\overline{OE}$ input as well as $\overline{OE}$ input may be programmed active Low.

PIN CONFIGURATION

40 PDIP/SOP



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Input
Q0~Q14	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB address(Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE ($\overline{BYTE}$=VSS)

$\overline{CE}$	$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby (ICC2)	1
L	H	X	Non selected	High Z	Operating (ICC1)	1
L	L	A-1 input	Selected	DOUT	Operating (ICC1)	1

WORD MODE ($\overline{BYTE}$=VCC)

$\overline{CE}$	$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby (ICC2)	1
L	H	High Z	Non selected	High Z	Operating (ICC1)	1
L	L	DOUT	Selected	DOUT	Operating (ICC1)	1

NOTE1:X=H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0° C to 70° C
Storage Temperature	-65° C to 125° C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

*Note:
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS (Ta = 0° C ~ 70° C, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	VIN=0 to 5.5V
Output Leakage Current	ILO	-	10uA	VOUT=0 to 5.5V
Power-Down Supply Current	ICC3	-	100uA	$\overline{CE}$>VCC-0.2V
Standby Supply Current	ICC2	-	1.0mA	$\overline{CE}$ = VIH
Operating Supply Current	ICC1	-	60mA	Note 1

CAPACITANCE (Ta = 25° C, f=1.0MHz (Note 2))

Item	Symbol	MIN.	MAX.	UNIT	Conditions
Input Capacitance	CIN	-	10	pF	VIN=0V
Output Capacitance	COUT	-	10	pF	VOUT=0V

AC CHARACTERISTICS (Ta = 0° C ~ 70° C, VCC = 5V±10%)

Item	Symbol	23C4100-10		23C4100-12		23C4100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Cycle Time	tCYC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Output Hold Time After Address Change	tOH	0ns	-	0ns	-	0ns	-
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Select Access Time	tAOE	-	50ns	-	70ns	-	80ns
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

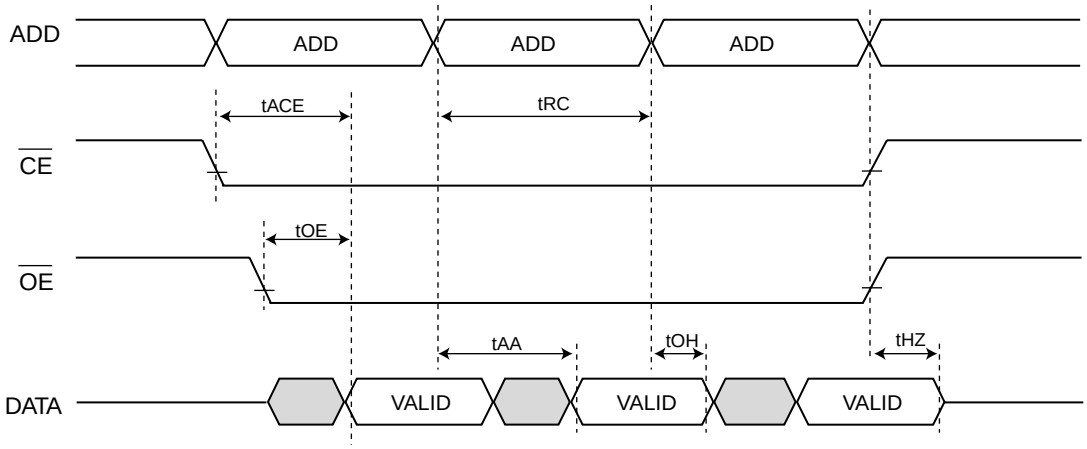
Note:
1. Measured with device selected at f=5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% teseted.

AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	1TLL+100pF

TIMING DIAGRAM

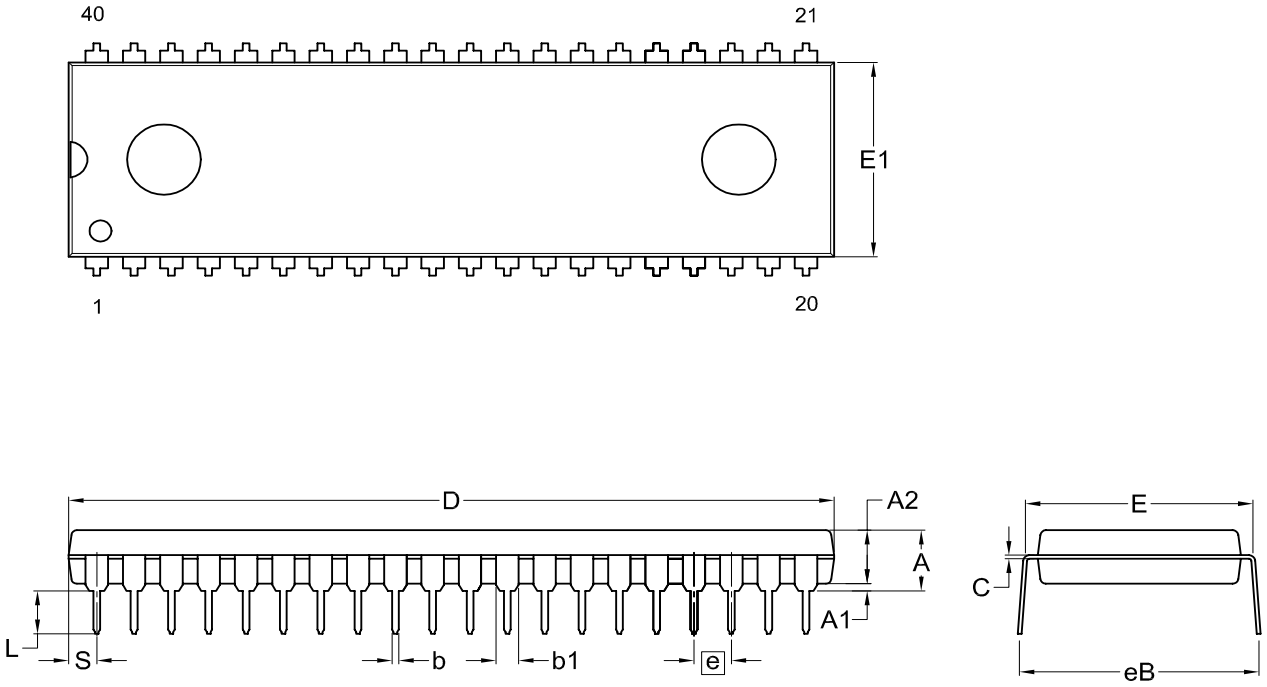
RANDOM READ



Note: $\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

Title: **Package Outline for PDIP 40L(600MIL)**

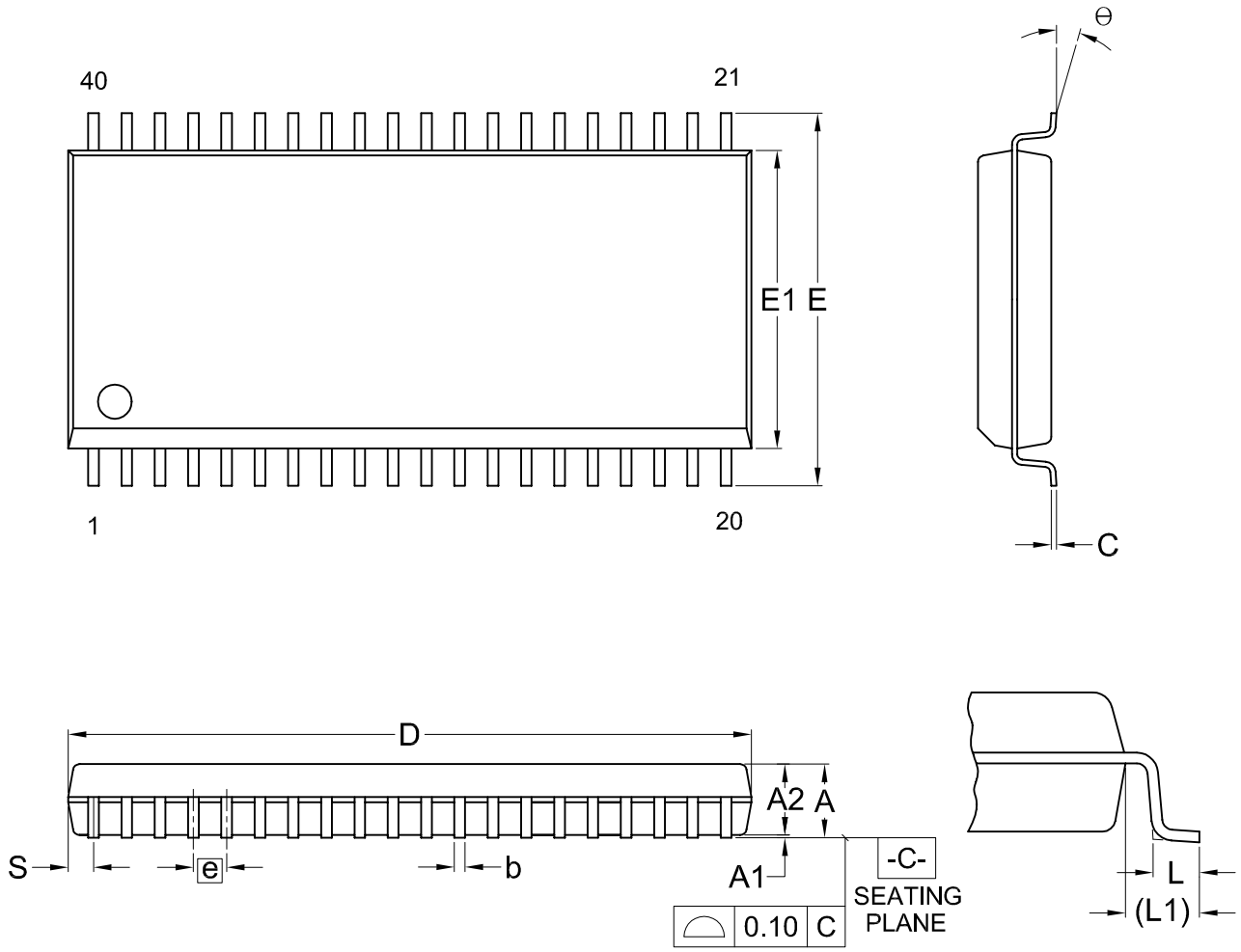


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.25	3.73	0.38	1.14	0.20	51.31	15.11	13.84		15.75	2.92	1.65
	Nom.	---	---	3.94	0.46	1.27	0.25	51.94	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.57	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.010	0.147	0.015	0.045	0.008	2.020	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	2.045	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.070	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.4	8				11-24-'03

Title: **Package Outline for SOP 40L (450MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	25.93	13.92	11.17		0.56	1.20	0.84	0
	Nom.	---	0.15	2.69	0.41	0.20	26.06	14.12	11.30	1.27	0.76	1.40	0.97	5
	Max.	3.00	0.20	2.80	0.51	0.25	26.19	14.32	11.43		0.96	1.60	1.10	8
Inch	Min.	---	0.004	0.102	0.014	0.006	1.021	0.548	0.440		0.022	0.047	0.033	0
	Nom.	---	0.006	0.106	0.016	0.008	1.026	0.556	0.445	0.050	0.030	0.055	0.038	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.031	0.564	0.450		0.038	0.063	0.043	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404.1	4	MO-099			11-26-'03

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
3.3	AC CHARACTERISTICS tOH 10ns-->0ns	P3	JAN/29/1999
3.4	Modify MX23C4100-10 AC Characteristics:tAOE:60ns-->50ns(max.)	P3	OCT/17/2000
	tHZ:70ns-->20ns(max.)	P3	
3.5	Delete Fast time:200ns	P1,3	JAN/19/2001
	Modify CE/$\overline{CE}$-->$\overline{CE}$; OE/$\overline{OE}$-->$\overline{OE}$	P1,2	
	Modify AC Characteristics	P3	
	Modify Timing Diagram	P4	
	Delete Order Information	P5	
3.6	Modify Package Information	P5,6	JUL/16/2001
3.7	Modify Package Information	P5,6	NOV/21/2002
3.8	Modify 40-PDIP Package Information	P5	JUN/19/2003

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com

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